COOPERATIVE RESEARCH

1987 Annual Report

The Semiconductor Rese

The Annual Report of the Semiconductor Research Corporation is published each June to summarize the directions and results of the SRC Research Program, present the formal financial report, and provide information on activities and events of the SRC industry/government/university community for the previous calendar year. The highlight material contained in the research section and most of the illustrations used in this publication are provided by the faculty and or graduate students conducting SRC-sponsored research. The remaining text is written by the technical staff of the SRC. Production is guided by the SRC's Editorial Coordinator, Marian Regan.

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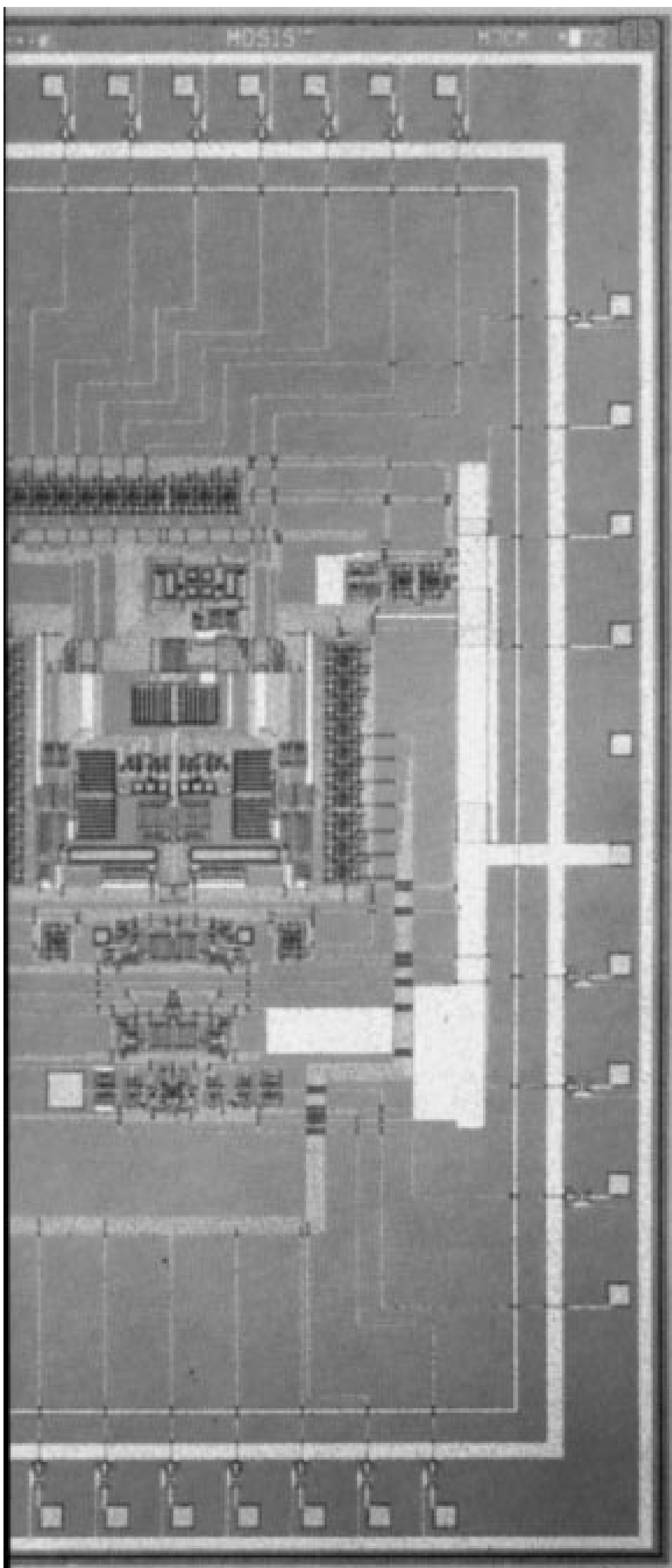


The Semiconductor Research Corporation (SRC) is a cooperative effort of U.S. companies, with government participation, to strengthen and maintain the vitality and competitive ability of the U.S. semiconductor industry. Semiconductors are the key material in integrated circuits, sometimes referred to as microelectronic devices. These are the basic building blocks of the computation, communication, information processing, and automation capabilities that are pervasive in the modern world and upon which the nation's defense and economy are becoming increasingly dependent.

The SRC plans and implements an integrated program of basic research conducted by faculty and graduate students in the university laboratories. The more-than-$80 million the SRC has committed to research programs over the last five years has funded a so/id majority of the silicon-related generic research conducted at U.S. universities. In 1987, SRC research investigations supported efforts of 276 faculty and 383 graduate students on 36 campuses.

SRC research is related to a set of long-range industry goals. Research projects are funded through formal contracts that are closely monitored by senior members of the 32-person corporate staff based at SRC headquarters in Research Triangle Park, North Carolina. Two special advisory groups complement the SRC Board of Directors in furnishing policy and program guidance: the Technical Advisory Board (TAB) and the University Advisory Committee (UAC).

In 1987, the SRC provided support to the SEMATECH cooperative effort in manufacturing technology and will continue to participate by managing the SEMATECH supporting research program.

The Semiconductor Research Corporation is a model of cooperation for the efficient use of domestic resources. Its success has set the stage within the industry, and between the industry and the government, for SEMATECH and other cooperative initiatives to strengthen the U.S. technology base and, as a result, our nation's ability to compete in microelectronics.

Die photograph of a pipelined, self-calibrating A/D converter implemented in CMOS technology at MIT (see research highlight on page 34).

Message from the Chairman of the Board and President

The SRC has been in operation for five years and is, by now, solidly established. Within our industry, the SRC is widely recognized for its accomplishments towards an integratedprogram of basic semiconductor research in university laboratories, and for encouraging the supply of suitably qualified scientists and engineers. On a wider front, people are excited by the symbolism of U.S. companies' cooperating on establishing a sound foundation for our work. It has been delightful to watch the steady decrease of suspicions, and the increasing ease of converse.

The most significant event of the last year has been the creation of SEMATECH. It represents a quantum leap in the cooperative activities of our industry. The SRC has been a major participant in the many activities that resulted in the creation of SEMATECH. That is very appropriate, since SEMATECH's mission is manufacturing technology, while a major part (a third) of the SRC's program is in the closely related area of manufacturing sciences. For that matter, there is also a close relation of manufacturing technology with microstructure sciences and design sciences, through design for manufacturability. The SRC will participate in SEMATECH by assuming responsibility for its supporting research program. The administration of this program will be similar in most respects to the existing SRC research efforts, and the results are expected to be available to all SRC members.

It has been a busy year. As has been thoroughly publicized in the press, the creation of SEMATECH was fraught with major difficulties, which added greatly to the load of the staff. A second issue was the need for the SRC to transition from growth to stable funding. This came about because of the '85-'86 downturn in industry revenues, the resultant effect on SRC income, and now the need to rebuild our reserves. The necessary adjustments to the research agenda have been made, and the research program remains one of high quality and productivity. Throughout these difficulties we have enjoyed constructive dialogue and good relations with our university partners.

Since the inception of the SRC research program at the end of 1982, each of five groups has received total funding in excess of five million dollars: the University of California at Berkeley, Carnegie-Mellon University, Cornell University, the Microelectronics Center of North Carolina, and Stanford University. The SRC support has had a major impact on each of these research institutions, strengthening their contributions to the new knowledge upon which our industry relies. We are currently reviewing the products of these major efforts in order to obtain better understanding of the research management process. A brief summary of the first of these reviews, on Cornell, is given in this report.

The SRC has assumed an important role in the semiconductor research activities in this country. I expect that over time the industry will find that more activities should be carried out together, rather than separately, and that the SRC will be asked to assume a broader responsibility for these cooperative activities. Its future successes will be determined by the quality of member participation, of its leadership, and of the research community with which we work.

My successor as Chairman of the Board of Directors is Robert J. McMillin of Genera/ Motors. I am confident that he will find his tenure as rewarding as I have found mine and that the SRC will benefit from his leadership.

Klaus Bowers

Klaus D. Bowers
Chairman, Board of Directors

Dr. Bowers has noted that this past year has seen significant additional activity related to SEMATECH on top of the increasingly busy schedule of the SRC. The SRC's ability to respond to this challenge is due to its highly capable staff. Essential to this staff are the residents assigned for varying lengths of time by member organizations. These individuals make significant contributions to semiconductor technology while at the SRC and, in the process, obtain invaluable experience. At present, industry resident managers comprise half of the ten-person research program staff.

As SEMATECH becomes a reality, we expect that direct technology transfer from SRC research to members will be augmented by transfer to SEMATECH. SEMATECH will become one of our biggest customers. The foundation for a close relationship between the SRC and SEMATECH has been established by the requirement that all SEMATECH members must also be members of the SRC.

The partnership between the U.S. government and the industry in semiconductor technology has grown much stronger. One effort in which the SRC has taken initiative is support of the concept of a National Advisory Committee on Semiconductors. The NACS would provide a means for acquisition of information on the technology and for the application of this information to increase the efficiency of the diverse, and sometimes redundant, semiconductor R&D efforts in the United States.

The SRC's primary research mission is the generation of new knowledge that enables members to advance their abilities to make competitive, high-performance products. An efficient means for communicating this knowledge is in the form of models for systems, circuits, devices, materials, processes, equipments, and fabrication sequences. Technology complexity makes these models difficult to construct and apply. During this past year, the SRC has seen important progress in modeling and the associated software environment. The need to link the technology models in a structure that extends from behavioral chip descriptions to final production is becoming accepted. Efforts to provide a full spectrum of the needed tools and software are paying off. Equipment modeling efforts are getting results, process and device models are being extended for submicron design rules, and linkages between CASM (computer-automated semiconductor manufacturing) and CAD tools are being established. The knowledge on which future semiconductor manufacturing will be based is emerging from SRC research.

Larry W. Sumney
President

Participants

Companies

AT&T
Advanced Micro Devices, Incorporated
Applied Materials, Incorporated
Control Data Corporation
Digital Equipment Corporation
E.I. du Pont de Nemours & Company
E-Systems, Incorporated
Eastman Kodak Company
Eaton Corporation
GTE Laboratories, Incorporated
General Electric Company
General Motors Corporation
Harris Corporation
Hewlett-Packard Company
Honeywell Incorporated
IBM Corporation
Intel Corporation
Loral Systems Group
Monolithic Memories, Incorporated *
Monsanto Company
Motorola, Incorporated
National Semiconductor Corporation
The Perkin-Elmer Corporation
Rockwell International Corporation
SEMI, Chapter **
Silicon Systems, Incorporated
Texas Instruments Incorporated
Union Carbide Corporation
Varian Associates, Incorporated
Westinghouse Electric Corporation
Xerox Corporation

*The commitment for individual participation in the SRC by Monolithic Memories in 1987 preceded corporate merger with Advanced Micro Devices.

Government

Department of Defense
National Bureau of Standards
National Science Foundation
National Security Agency

**The following companies are included in the Semiconductor Equipment and Materials Institute, Inc., CHAPTER:

AG Associates
American Technical Ceramics
Applied Electron Corporation
ASYST Technologies, Inc.
Coors Ceramics Company
Dynapert/Amedyne
Eagle-Picher Industries, Inc.
Emergent Technologies Corporation
FEP Analytic
FSI Corporation
Genus, Inc.
Gryphon Products
Hercules Specialty Chemicals Company
Ion Beam Technologies, Inc.
Ion Implant Services
Lehighton Electronics, Inc.
Logical Solutions Technology, inc.
MacDermid, Inc.
Machine Technology, Inc.
MG IndustrieslScientific Gases
Micrion Corporation
The Micromanipulator Comany, Inc.
Oneac Corporation
Optical Specialties, Inc.
PT Analytic, Inc.
Pacific Western Systems, Inc.
Peak Systems, Inc.
Sage Enterprises, Inc.
The SEMI Group, Inc.
Silsco, Inc.
SILVACO Data Systems
SOHIO Engineered Materials Company
Solid State Equipment Corporation
Technology Modeling Associates, Inc.
Thermco Systems, Inc.
UTI Instruments Company
VLSI Standards, Inc.
XMR, Inc.

Institutions

Arizona, University of
Auburn University
Brown University
California at Berkeley, University of
California at Los Angeles, University of
California at Santa Barbara, University of
California Institute of Technology
Carnegie-Mellon University
Case Western Reserve University
Clemson University
Columbia University
Cornell University
Duke University
Florida, University of
Florida State University
Georgia Institute of Technology
Illinois at Urbana/Champaign, University of
The Johns Hopkins University
Lehigh University
Massachusetts at Amherst, University of
Massachusetts Institute of Technology
Michigan, University of
Microelectronics Center of North Carolina
Minnesota, University of
Nebraska at Lincoln, University of
North Carolina at Chapel Hill, University of
North Carolina State University
Oregon Graduate Center
Purdue University
Rensselaer Polytechnic Institute
Research Triangle Institute
Rochester, University of
Rochester Institute of Technology
South Florida, University of
Southern California, University of
Stanford University
Texas at Austin, University of
Vermont, University of
Yale University

Malcolm L. White, Research Scientist at Lehigh University, uses a vacuum evaporator to deposit aluminum on glass substrates for semiconductor corrosion studies. *(This photograph and the one on page 26 appeared in the "Lehigh Research Perspective 1987" and are used with permission of journalist/photographer Kenneth A. Friedman, 3061 Powder Mill Circle, Bethlehem, PA 18017.)*

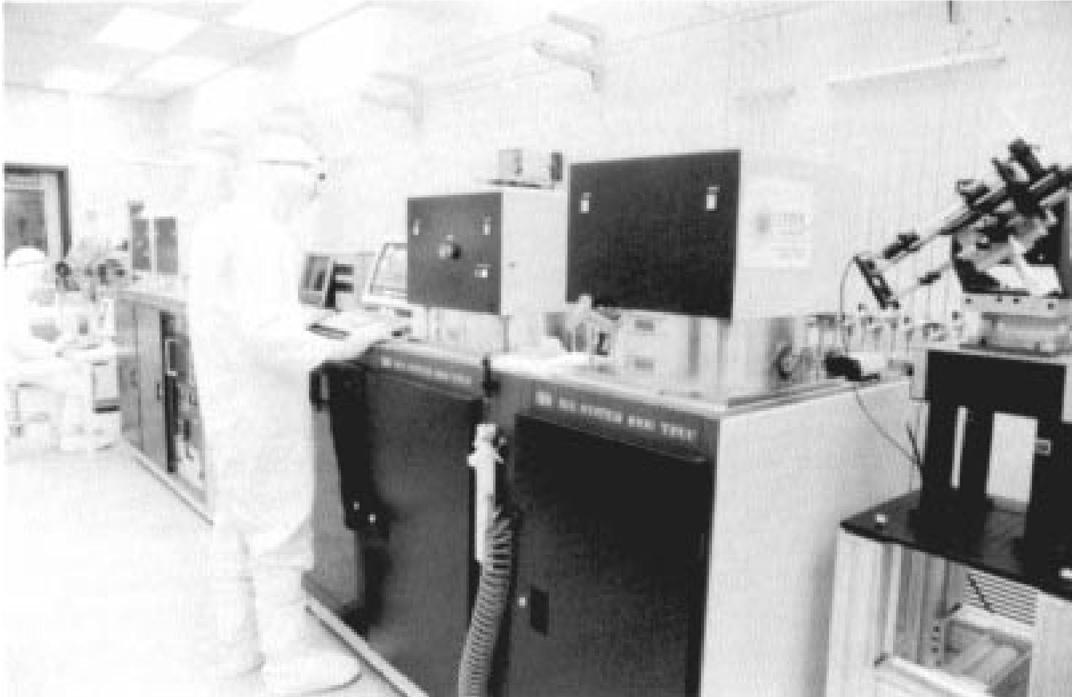
Cooperation

Cooperative Research Concept

High quality research follows from a well-planned program that uses the best information, concepts, and resources.

Characteristics of the SRC Research Program:

- *DEFINITION. From the outset, the SRC Research Program has responded to a set of goals defined by representatives from the SRC member companies. These goals provide a framework for selection of university-based research projects that are relevant to the needs of the industry and will result in a 20% acceleration in the pace of basic semiconductor technology by the year 1994.*
- *FOCUS and DIRECTION. Roadmaps have been developed by industry representatives to refine and interpret the overall SRC research goals for the selection of specific research thrust areas and projects. These roadmaps are living documents that allow for continuous fine-tuning to adjust to changes in strategy, funding, and the technology.*
- *CONTROL. SRC research funding is distributed through formal contracts calling for deliverables on an agreed-to schedule.*
- *ACCOUNTABILITY. Research funding is provided through a cost-reimbursement system that is keyed to recipients' meeting contract obligations.*
- *CREATIVITY. Topics under study in university laboratories are sufficiently flexible to accommodate innovation.*
- *BROADENING THE UNIVERSITY BASE. SRC research funding allows universities to hire additional faculty, and to update research equipment and facilities. SRC support also helps universities attract additional funding from other sources. The SRC, in 1987, initiated a program for development of interdisciplinary curricula for the education of microelectronics manufacturing engineers.*
- *ATTRACTING GRADUATE STUDENTS TO INDUSTRY-RELATED FIELDS. By enabling universities to conduct research that is relevant to the practical needs of the industry, the SRC has attracted more than 500 highly qualified graduate students to work on SRC projects that prepare them for the industry's manpower needs.*
- *DEPTH. The communication and interaction that are encouraged among academic/industry/government researchers of the SRC community not only serve to strengthen the SRC research program and to keep members informed of its progress, but also help to reduce research redundancy among industry/government/university participants.*



"The SRC played a key role in creating our current semiconductor program at Michigan. [The SRC's] direct investment is close to $2.3 million and that, plus [the SRC's] influence, has enabled us to attract State and Federal support in the amount of over $16 million in facilities and about $8 million in annual research."

— Professor K.D. Wise

UPDATE TO UNIVERSITY FACILITIES. Among the advantages universities gain from SRC research funding is the opportunity to update equipment and expand facilities for state-of-the-art research. Shown above is a Solid-State Fabrication Facility built, in part, with SRC funding to the University of Michigan Program in Automated Semiconductor Manufacturing. This project uses reactive ion etching as a process vehicle for examining key issues associated with automated sensing, control, and process integration (see research highlight on page 21).

- *QUALITY. SRC research is continuously monitored by the SRC technical staff and regularly reviewed and assessed by industry experts for quality assurance.*
- *RESULTS: TECHNOLOGY*

... a supermarket of research results has been made available by university researchers for transfer to industry members,

> *"... we found the VLSI design automation research extremely relevant to our industrial applications. The fact that it is followed in many cases by actual programs of high quality, makes it even more attractive . . . "*
> *— National Semiconductor*

... inventions and new or improved processes have been transferred to industry,

> *"If not for the availability of this valuable source of information, it would have taken us weeks or possibly months to get the technique working;"*
> *— Emergent Technologies.*

... a variety of software packages has been released to the mainstream.

> *"These programs have proven very useful and have had a major impact on our ability to design and analyze packages"* *— Honeywell.*

- *RESULTS: MANPOWER.*

... The SRC research program has tripled the population of graduate students who will make the seminal inventions of the next decade and will comprise the manpower base of the future industry.

... Over the last five years, more than 150 students who conducted research under SRC contracts have completed requirements for the Master's or Ph.D. degrees and have joined the U.S. work force. Most of these persons are now employed by SRC member companies or have joined the faculty of U.S. universities.

Cooperation

Technology Transfer in Action

Activities, events, and communication mechanisms are offered by the SRC to expedite the transfer of technology and to foster cooperative interaction among the industry engineers and scientists, university researchers, and government technologists who participate in the SRC Community.

Events

The following major SRC technology transfer events in 1987 provided opportunities for exchange of information among industry, government, and academic participants in the SRC community. A total of over 750 persons participated.

January 19: The workshop on **Technology Transfer** reviewed technology transfer practices currently in use at member companies and identified key technology transfer issues for industry. Three working sessions addressed (1) barriers and solutions. (2) measurement and reporting, and (3) information dissemination. An SRC technology transfer roadmap was developed.

February 23 and 24: A two-day **Technology Transfer** Course on **FABRICS** provided discussions and laboratory hands-on use of FABRICS, PROMETHEUS, PED, and PI/C. an Integrated suite of computer tools that provides synthesis support for the design of manufacturing processes that minimize the effects of random fluctuations and thus maximize yield.

March 17 and 18: The Topical Research Conference on **Reliability of VLSI Circuits** discussed future directions of reliability as related to oxides, electrostatic discharge, electromigration, packaging, equipment, and design.

April 21 and 22: The Topical Research Conference on **Advanced MOS Process and Device Modeling** assessed state-of-the-art process and device modeling research, postulated needed future research directions, and provided insight on the need for supercomputing in microelectronics technology CAD.

May 74: A workshop on **Semiconductor Fabrication Equipment: Vendor-User Synergisms** discussed the nature of vendor-user relationships and identified means for increasing benefits from these interactions in the U.S. semiconductor fabrication equipment industry.

May 28 and 29: At the **Bipolar Device Technology** conference, university and industry researchers who work at various levels of modeling/simulation discussed the full range of activities currently being pursued in bipolar devices and circuits.

June 3 and 4: At the DARPA/SRC Workshop on **Computer-Integrated Manufacturing (CIM)** researchers explored the advantages of CIM, flow languages, data models, scheduling, system architecture, equipment models, management tools, and information dissemination via networks.

June 16: The DEC/SRC Workshop on Technology Transfer in **Japan** covered corporate technology transfer processes in Japan and the U.S. Discussion areas included public policy, corporate philosophy, management strategy and industrial/interrelationships, societal factors, educational system, technology transfer mechanisms, internal technology acquisition, and measurements of success.

Photos: UPPER — Professor Michael Borrus, Deputy Director of the Berkeley Roundtable on International Economics, addressing forum audience; LOWER — Joseph L. Bower of the Harvard Business School, leader of forum panel.

June 29 to July 3: *The joint SRC/Institute for Theoretical Physics Workshop on **Quantum Domain Devices** discussed the interaction of quantum mechanical and (quasi-)classical phenomenological models, localization and interference effects, fluctuations, and the novel physics associated with small systems with a focus on "What can submicron technology do for information technology?"*

July 8 and 9: *A technology Transfer Course on **Technology CAD for BiCMOS Design** provided lecture sessions and hands-on lab experience using a one-dimensionaland a two-dimensional TCAD tool set for BiCMOS design. Future plans for tool development under SRC sponsorship were discussed.*

September 15 and 16: *The Topical Research Conference on **Design Verification** assessed the current state of the art and defined areas requiring further research. It was decided that design verification would still be a relevant system design process for the 1990s.*

November 5 and 6: *The Topical Research Conference on **Packaging Reliability Without Hermeticity** covered operating environments, mechanisms of failure, physical chemistry of moisture films, contamination thresholds, and ionic activity.*

November 13: *Participants in the Workshop on **Data Management for IC CAD** were introduced to the Berkeley OCT / VEM / RPC design environment through presentations and on-line demonstrations and provided with an industry view of data management requirements for IC design systems of the 1990s.*

November 20: *At thesecond DEC/SRC Workshop on **Technology Transfer in Japan,** findings from interviews and literature searches for a project to explore technology transfer mechanisms being practiced in Japan and the United States were presented.*

December 10 and 11: *A Topical Research Conference on **Submicron BiCMOS Technology for the 1990s** included discussions of significant advances in process integration, unit processes, and circuit design. Critical issues were identified in order to define future research directions and to provide recommendations on how to cost-effectively marry CMOS and bipolar technologies to achieve a submicron BiCMOS technology.*

Competitiveness Forum

The SRC arranged a forum on "U.S. Competitiveness — Analysis and Remedies," by a panel of four distinguished scholars from the Harvard Business School and the Berkeley Roundtable on International Economics for a joint meeting of the SIA/SEMATECH/ SRC boards in September. The panelists analyzed the relationship of national culture, manufacturing systems, and marketing approaches to a country's economic success in the international marketplace. Improvements were suggested for U.S. business, industry, and education that would strengthen this nation's competitive capability. Representatives from the U.S. semiconductor industry comprised the audience of more than 100 persons.

Technology Transfer in Action (continued)

SRC fellowship recipients Michael Neacsu (left), graduate student at the University of North Carolina at Chapel Hill, and Thomas Cobourn, graduate student at Carnegie-Mellon University.

Fellowship Banquet

The SRC honored the 29 students who have been supported by SRC Fellowships with a banquet on October 19 at the Governors Inn at Research Triangle Park, NC. Sharing dinner were members of the SRC technical staff and the newly appointed Fellowship Program Industry Advisors. On October 20, the students conducted a 'poster session" to familiarize the industry Advisors with research being done in respective graduate programs. The advisors are staff from SRC member companies who have volunteered to establish a one-on-one relationship with a Fellowship recipient throughout his or her doctoral studies. This meeting generated enthusiastic interactions not only between advisors and students, but also among students who discovered areas of similar research interest.

Government Participation

Recognizing that the stakes are high and the risks real for the U.S. economy and national security if this country does not have a world-class and competitive semiconductor industry, three agencies of the federal government agreed in September, 1986, to participate in the SRC. In 1987, a fourth agency became a participant — the National Bureau of Standards.

Agency scientists and engineers contribute technical expertise to the research program and share in all phases of SRC activity with members of the university and industry community. The Government Coordinating Committee (GCC) of the SRC has the responsibility to provide the technical link between the various participating government agencies and the SRC Research Program. Mr. K. Speierman of the National Security Agency has served as the GCC Chairman since its inception. Other members of the committee include.. Mr. E.D. "Sonny" Maynard (Department of Defense), Dr. Alan Stubberud (National Science Foundation), Mr. C.E. Holland, Jr. (SRC Resident Program Manager assigned by DoD), and Mr. Frank F. Oettinger (National Bureau of Standards). The GCC actively developed plans in the latter part of this year to significantly increase government agency and personnel participation.

Evaluation

The first in a series of evaluations of SRC research at universities with major cumulative investments was conducted in 1987. An evaluation team examined SRC research at Cornell University, which has received over $7 million in funding since 1982 for investigations directed to long-range objectives in process and device technology, and, more recently, in packaging.

The evaluation team concluded that Cornell's multidisciplinary research effort, involving 28 faculty members and 47 graduate students in 1987, was effectively addressing SRC goals and objectives.

Recommendations were made to the SRC to strengthen Cornell's sensitivity to patents and to guard against excessive focus at the expense of creativity. Cornell's role in the SRC research agenda is to provide a scientifically strong effort directed toward submicron process and device technology with a focus on one-quarter micron CMOS; and, in packaging, to concepts, materials, and base technologies.

Resident Managers

Resident Managers are employees of member companies or government agencies who are assigned to SRC headquarters as technical staff for periods of one or more years. As members of the staff, the residents contribute the benefit of their experience to the SRC research program and share in monitoring the research contracts. Having an employee on site for continuous access to the research is an excellent mechanism for maximizing technology transfer. Listed in the fable below are the Resident Managers who have reinforced the corporate staff since the SRC's inception.

The response of member companies and government agencies in providing a growing number of Residents as staff assignees significantly enhances the efficient and effective management of SRC research.

Publications

In 1987, the SRC distributed over 12,500 copies of publications generated from university research and by the SRC staff. The SRC library catalogued 954 new research documents from January through December, and, by the end of the year, its inventory contained more than 2,800 SRC publications.

The SRC Newsletter

The monthly SRC Newsletter provides information for and about the SRC community. The newsletter is available free of charge to the staff of member companies, participating government agencies, and U.S. universities. Circulation increased by 20% during 1987, reaching 5,000 copies by year's end. Seventy-five percent of the subscribers are member company personnel.

Information Central

Use of information Central, the SRC's on-line telephone database and mail facility, continues to provide 24-hour-a-day benefits for the staff of industry/government members and university contractors. Off-site users logged over 840 hours of connect time in 1987 to obtain information about SRC research and related activities. In addition to dialup usage of information Central, electronic communications among member companies, universities, and the SRC via CSNET-Internet increased substantially.

Resident Managers *

Name	Assigned From	Period of Residence	Area of Responsibility
Benjamin J. Agusta	IBM	1983-1984	Microstructure Sciences
Richard A. Lucic	HP	1983-1984	Manufacturing Sciences
James R. Key	CDC	1983-1985	Technology Transfer
John J. Cox	DuPont	1984-1985	Packaging
Patrick W. Wallace	DuPont	1984	Packaging
Jeffrey A. Coriale	Harris	1984-1987	CMOS-BiCMOS
Shakir A. Abbas	IBM	1985-1987	Bipolar Technology/Reliability
Phillip A. Lutz	GM-Delco	1986-	Packaging
Norman F. Foster	ATT	1987-	Manufacturing Science/Reliability
C. Edward Holland, Jr.	DoD	1987-	Government Interface
Kenneth L. Pocek	Intel	1988-	Design Sciences
Jeffrey L. Hilbert	Motorola	1988-	Design Sciences
Vincent Lyons	IBM	1988-	TECHCON 88

*Additional staff from member companies have served as Ad Hoc Assignees to assist in implementing Topical Research Conferences and Workshops or for short-term management of other activities.

The SRC and Cooperative Initiatives

The success of the SRC in demonstrating the effectiveness of cooperation has led to its being called upon to participate in other efforts aimed at responding to competitiveness issues for the U.S. semiconductor industry. Primary among the SRC's contributions to other efforts is a unique understanding of the status and future directions of semiconductor technology that has been gained while defining and implementing its own generic research program with the industry.

SEMATECH

SEMATECH is the most prominent and highest impact initiative that involved the efforts of the SRC staff during 1987. This is an industry/government cooperative endeavor that reached an advanced planning phase by the beginning of 1988 and that will be located in Austin, Texas. The aim of SEMATECH is to ensure a domestic, world-class semiconductor manufacturing capability by 1993 through focused development and application of modern manufacturing technology.

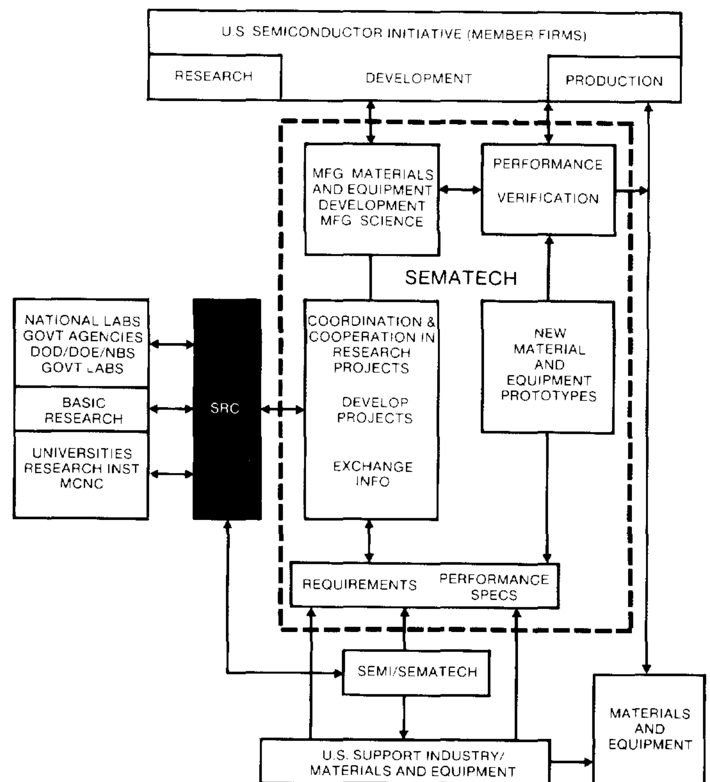
The SRC has participated from the outset in defining the need for, the thrust of, and gaining support for SEMATECH. The SRC's president, Larry W. Sumney, has had a key role as Managing Director for SEMATECH in its startup phase, and the SRC's research staff have contributed to the planning process. SEMATECH has identified the SRC as its agent for implementing and administering a supportive research program. The operational concept for SEMATECH is shown in the diagram.

The university-based program already established by the SRC provides a strong foundation on which to build a research agenda for SEMATECH. Priority research needs of SEMATECH have been identified in such areas as optical lithography, metrology, manufacturing systems, etching, multilevel interconnection systems, and packaging.

The SRC will carry out a research program in support of SEMATECH in much the same mode as it has planned and implemented its existing research program since 1982, although funding for the two programs will be distinct. Most of the results of both programs will be available to all SRC participants, and SRC research results will be fully accessible by SEMATECH.

Charles E. Sporck (left), Chairman of the SEMATECH Board of Directors, with Larry W. Sumney, President of the SRC.

SEMATECH Concept



Formulation of a research plan for SEMATECH was begun in the latter part of 1987, and the first step in setting up the program was taken at the beginning of 1988 when a Centers-of-Excellence program was initiated. These centers will not only conduct research, but will also provide knowledge resources for SEMATECH's use during its aggressive development efforts.

Additional SEMATECH research initiatives may extend beyond academic laboratories to other institutional participants in semiconductor research. However, plans for these activities were still in the early stages by the end of this calendar year.

National Advisory Committee on Semiconductors (NACS)

Legislation was introduced in 1987 in the United States Congress for the establishment of a prestigious advisory body on domestic semiconductor R&D activities. The motivation for a National Advisory Committee on Semiconductors is to improve the competitive strength of the U.S. industry by increasing the efficiency of its diverse R&D efforts. One approach that could be taken by an NACS would be to provide an overview of the programmatic and technical components of the nation's semiconductor research activities, and to conduct a coherent analysis of its competitive status and needs.

The SRC has participated in defining the NACS concept and has consulted with the Congress and others in bringing this proposal to its present stage. It is anticipated that if this proposal is enacted, the SRC will continue to cooperate in making it a success.

0ther Cooperative Activities

Other activities of the government and industry related to cooperatively addressing semiconductor issues in which SRC staff have been engaged include participation on advisory committees of the National Science Foundation, the Department of Defense, and the National Academy of Sciences. The SRC is also represented in ongoing Semiconductor Industry Association (SIA) activities that focus on industry concerns. At the SIA/SRC Joint Conference in September, a forum was organized and conducted by noted academicians to analyze broad issues regarding U.S. competitiveness.

The above photograph taken at the Sandia National Laboratories includes the following workshop participants (left to right): Dr. W. Dale Compton, Senior Fellow, National Academy of Engineering; Dr. William C. Holton, SRC Director for Microstructure Sciences; Dr. Louis C. Ianniello, DOE Deputy Associate Director for Basic Energy Sciences and leader of the DOE National Laboratory Task Force Group; and Dr. Venky Narayanamurti, Vice President of Research, Sandia National Laboratories.

The Semiconductor Industry and the National Laboratories

The SRC has been active in representing the U.S. semiconductor industry at meetings to plan government/ industry initiatives toward developing a national strategy for the efficient use of domestic resources. One of these initiatives, under the auspices of the National Academy of Sciences, is aimed at implementing a cooperative effort between the research resources of the US. semiconductor industry and the facilities and expertise available at the U.S. Department of Energy's National Laboratories, A Workshop held at the Sandia National Laboratories on May 26 to 28, 1987, was the first in a series of technical-level planning meetings for this effort.

In November, a follow-on meeting to the Sandia Workshop was held at Oak Ridge National Laboratory. This series of meetings will continue at other National Laboratory sites to articulate specific areas of the industry's generic research needs that conform to the capabilities of the National Labs and to allow the National Laboratories to determine how they could mobilize their resources to address those research needs.

Research

The SRC's Research Program is based upon a vision of the future derived by working with the industry on goals.

This vision allows one to forecast trends in semiconductors over the next several years with considerable confidence and to create a research agenda that accelerates U.S. technology development while retaining flexibility for response to new ideas and findings.

SRC Research Goals

The SRC Research Program addresses industry needs for improved performance and higher density integrated circuits. In brief, the overall goals are to make possible in 1994 the prototype production of chips with:

- *complexity 250 times greater than those of 1984 (equivalent to a 256 Mbit DRAM),*
- *functional throughput rates of 5 x 10^{15} gate-hertz per square centimeter,*
- *reliability such that less than 10 failures occur in 1 billion operating hours,*
- *cost per functional element reduced by 500 times from 1984 costs.*

In 1988, the SRC is planning to update and extend these goals to the year 2001.

Research Directions

Although limited to topics associated with mainstream silicon semiconductor technology, the SRC's research agenda covers a broad spectrum. Major identifiable thrusts encompass a majority of the program. The following subjects represent most of the major thrusts, some results from which are presented as research highlights on the next twenty-four pages:

- *0.25 micron CMOS/&CMOS*
- *process and device modeling*
- *computer-automated semiconductor manufacturing (CASM)*
- *VLSI architectures*
- *high performance bipolar technology*
- *high performance packaging*
- *design synthesis*
- *single wafer processing*
- *reliability and yield enhancement*
- *analog ICs*
- *advanced process technology*
- *design for test*
- *curricula development for microelectronic manufacturing engineering education.*

In addition, efforts are underway in other areas, such as quantum domain devices, metrology and robotics.

Each of the thrusts identifies a research area that is a part of the SRC agenda and serves as a focus for defining future directions. This analytical process identifies high-impact microelectronic technologies for the nineties and beyond.

At present, little evidence appears to justify going beyond the 1/3-1/4 micron design rule capability in integrated circuits. Greater impact will be obtained through investment in design systems, development of improved system architectures, integrated manufacturing systems, and the hierarchical software and simulation environments that connect these.

Simulation of submicron semiconductor device production requires process and equipment models. The latter, in particular, do not exist and are proving difficult to obtain. Limits on equipment models may delay achievement of the sought-after ability to bridge simulations of system performance and design to those for production in order to achieve the economies necessary to compete successfully. In-situ and single wafer processing technologies are replacing batch processes of the past.

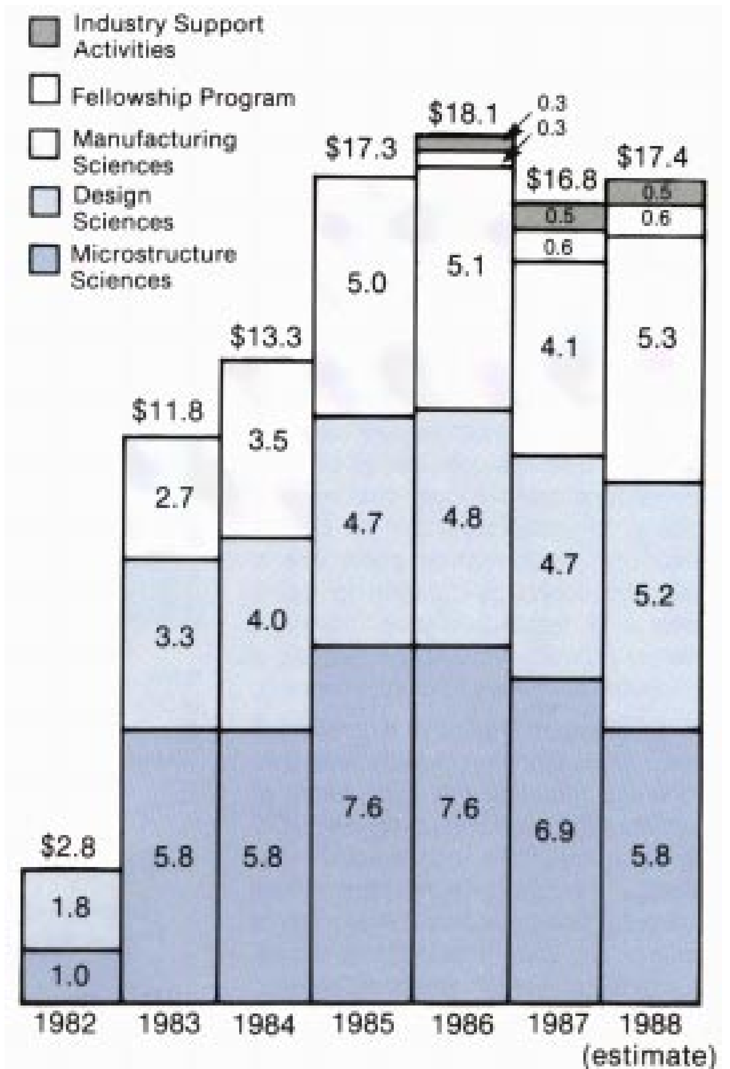
Metrology capabilities for submicron IC fabrication are very limited. In-process controls, pattern transfer, failure analysis, and structural control are pushing the limits of measurement and monitoring capabilities. The winner in the race to produce the next generation may be the possessor of the best measurement capabilities.

The increasing focus on system-level design, coupled with the complexity of submicron ICs, will present enormous challenges to design systems and methods. Future designs will require hierarchical methods, formal verification tools, and integrated design environments supporting system-level partitioning, extensive use of synthesis, and early evaluation of design tradeoffs — including performance, testability, reliability, yield, and cost.

Design systems will be extended to cover the design process from architectural-level system design through modeling of physical phenomena; device, materials, process, and equipment design; and mechanical and thermal considerations. Concurrent use of multiple technologies, large data volumes, and supercomputer systems and distributed heterogeneous networks will require integrated design data and process management.

CAD will extend to detailed thermal, electrical, and mechanical features of multichip subsystem packages.

Research Program Commitments
($ in Millions)



Trends in funding levels for SRC research are shown above. The growth of total funding through 1986 ended as the pool of potential new members decreased and fees from the present membership were affected by the industry recession. A reversal of this trend is occurring for 1988. Not shown, because key decisions are still being made, is the large impact that SEMATECH funding will have on SRC research activity. The SRC has been evaluating proposals for the SEMATECH Centers-of-Excellence initiative that will be managed through the SRC. This may result in a 25 percent increase in funding for research during the next calendar year.

The distribution of funding among the research areas is being brought into approximate balance according to plan. The apparent decrease in program expenditures for Manufacturing Sciences from 1986 to 1987 is, in part, an artifact resulting from the timing of year-end contract awards. It must be noted that the three major program areas are thoroughly integrated and such boundaries as may exist between them are not distinct.

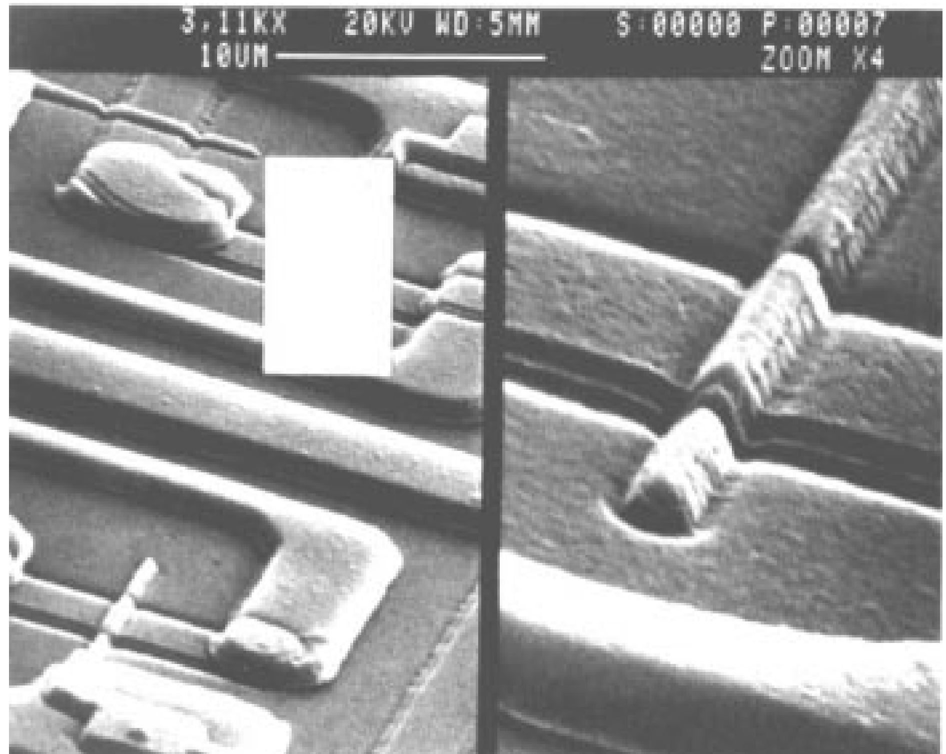
CMOS and BiCMOS Technology

As integrated circuit technology approaches thephysical limits of classicaldevice technology at approximately 0.1 micron minimum feature size, single chip designs will serve for many system applications; and, advanced packaging, employing "silicon backplanes," will provide for enhanced-capability multichip interconnected systems.

SRC CMOS circuit technology performance goals for 1994 are a 0.25 micron minimum feature size that will lead to device densities of 40 x 10^6 transistors/cm^2 for logic designs and 200 x 10^6 transistors/cm^2 for DRAM memory. Performance goals are a 50 picosecond pair switching delay with a 5 femtojoule/gate (power x delay) product. Circuits will require a minimum of four levels of interconnect.

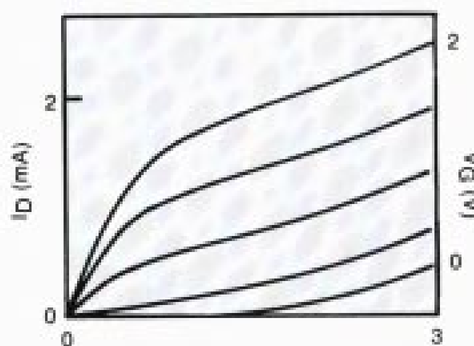
As minimum feature size is reduced and manufacturing yields improve (thereby reducing the cost adder of additional process complexity) BiCMOS is emerging as the leading edge technology for high-performance mixed linear/digital applications, digitalsignal processing, data acquisition systems, and, ultimately, high-speed digital logic and memory. SRC research is oriented to support this strategy, and technology roadmaps for both CMOS and BiCMOS are being prepared to provide guidance for the research.

Complementary BiCMOS technology thrusts in support of the SRC strategy have been initiated at MIT, Stanford, and the University of California at Berkeley. A key aspect of the technology involves the development of a design and a fabrication process that will permit decoupling of the performance parameters of the bipolar and CMOS components — allowing optimal tuning of the bipolar device to maximum speed or higher voltage as required by the circuit application, without compromising the performance of the CMOS elements.



SEM view of 0.25 μm n-channel MOS devices. Zoom window shows active region of MOSFET with effective channel length of 130 nm and effective gate width of 2.5 μm. Source-drain regions are silicided from the sidewall spacer outwards. Cornell University.

Device/ Process Integration for 0.25 Micron CMOS



Drain current-voltage characteristic of n-channel MOSFET with effective channel length of 90 nm and gate width of 2.5 μm at a temperature of 77 K.

Researchers at the SRCICornell Center for Microscience and Technology are investigating device structures, related unit processes, and process integration of 0.25 pm CMOS devices via design, fabrication, characterization, and analysis. Compatible E-mode 0.25 μm n-channel devices have been investigated in an E/D mode NMOS environment. The 0.25 μm NMOS process has been employed during 1987 for process and device experiments in order to complete the characterization of n-channel devices down to channel lengths of 100 nm.

Professor J. Peter Krusius
Cornell University

MIT BiCMOS Technology

The MIT BiCMOS process is oriented toward mixed analog/digital applications and is serving as the development vehicle for a 16-bit analog to digital converter. The process uses epi wafers and offers fully optimized NMOS, PMOS, and semi-oxide isolated vertical n-p-n bipolartransistors. In addition, MOS capacitors with n+ bottom plates, and non-optimized vertical p-n-p bipolar transistors are available.

The cross section of devices available is shown in the large figure above that was prepared by Kenneth O, an SRC-supported graduate student. The device characteristics for the MOS and n-p-n bipolar devices are shown in the three smaller figures below.

Professors L. Rafael Reif and Hae-Seung Lee
Massachusetts Institute of Technology

NMOS Device: gate width 20 μm, gate length 2 μm, Threshold V_t = +0.75 V, V_{SB} = 0, ΔV_{GS} = 1 volt steps.

PMOS Device: gate width 20 μm, gate length 2 μm, Threshold V_t = -0.85 V, V_{SB} = 0, ΔV_{GS} = -1 volt steps.

Vertical n-p-n Bipolar Device:
Emitter length 6.0 μm,
Emitter width 6.0 μm.

Accurate Simulation of Shallow Boron Implantation

Shallow boron profiles are required in submicron CMOS circuits and are produced by low energy implants of B+ or BF_2+ ions. Because Boron can channel so easily into silicon, the simulation of as-implanted boron profiles has been quite difficult. LSS theory fails to predict these profiles because if is strictly valid for implantation info amorphous materials for which there is no channeling. The use of a Pearson distribution offers only limited improvement. A new simulation approach has been successfuly applied for both B+ and BF_2+ implants. This physically based approach uses the sum of two Pearson functions that accounts for the channeling and nonchanneling events, respectively. The ratio of the two functions varies smoothly with the logarithm of the dose. A simulated profile based on this new approach is illustrated for B+ implants. The new approach provides accurate simulation of the entire profile for all energies and doses.

Professor A.F. Tasch
University of Texas at Austin

Process and Device Modeling

Accurate models are required for the design of processes and devices in the submicron regime. In turn, successful integrated circuit design depends on the availability of good circuit-level models for the circuit components. Several projects in the SRC research portfolio address the development of improved models and simulators for processes and devices. Work has continued on the extension and refinement of the leading-edge SUPREM 4 and PISCES 2 process and device modeling programs (see research highlight on following page). A class of difficult process modeling problems involves the representation of creep-flow phenomena that arise in IC processing. SRC research at Berkeley has resulted in a prototype simulator, CREEP, for this class of problems (highlight below).

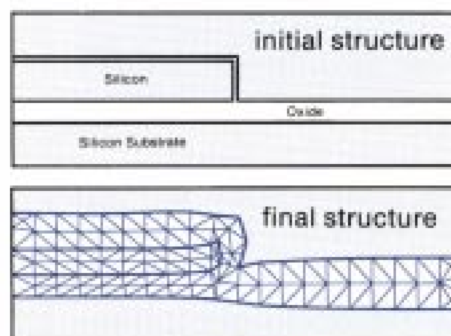
Several efforts are underway to devise improved circuit-level device models. At the California Institute of Technology, an accurate, physically-based charge model has been developed that expresses intrinsic charge in a MOS device as a single continuous analytic expression that is equally applicable in the saturation and ohmic regions of operation. Accurate and efficient table look-up models are being developed at the Georgia institute of Technology for analog applications. The BSIM modeling and characterization system for MOS devices from Berkeley is being extended to provide accurate models for 0.25 micron channellength devices, Work is focusing on representation of temperature effects, hot electron effects, and non-quasistatic charge effects.

SIMPL is a tool for simulating and viewing the cross-sectional structure of VLSI wafers, given mask and process data. An interactive workstation interface has been developed for SIMPL, and a capability for identifying potential topography problems has been added. SIMPL is now being linked to more detailed process simulators such as CREEP and SAMPLE via the PIF data format.

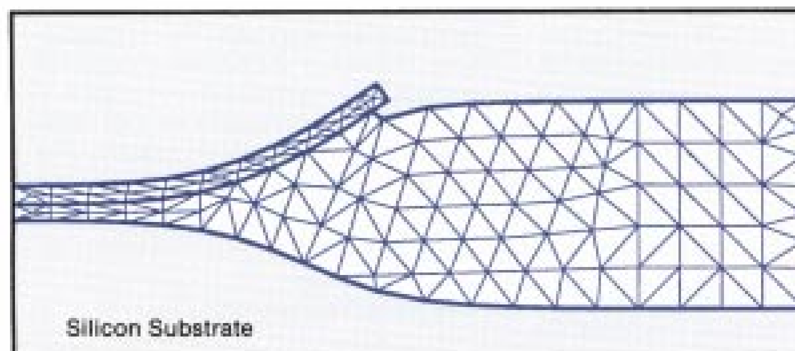
CODECS is a mixed-level circuit and device simulator that supports the inclusion of one and two-dimensional numerical models along with circuit models. This mixed-level simulation capability allows the user to explore the effect of process-related parameters, such as doping profiles, on circuit performance.

CREEP

CREEP is a two-dimensional process simulator designed to solve certain creep-flow problems encountered in IC fabrication technology. Its most important capability is the prediction of general 20 silicon oxidation. It also performs glass-reflow or film-shrinkage simulation as subset problems of silicon oxidation. CREEP incorporates stress-dependent silicon oxidation models which have been shown to accurately predict the retardation of oxidation on cylindrical silicon surfaces. CREEP is equipped with a flexible and robust data structure for handling geometrical information. All geometrical structures are represented using nodes and segments. Hence, fairly general geometrical structures can be handled. An automatic finite element mesh generator has also been built into the CREEP program. The figures show simulations of a silicon gate and a LOCOS structure to illustrate the capability of the mesh generator. In both cases, the user specifies only a mesh-density parameter (about 10 µm in the examples shown). The mesh is then generated automatically by CREEP at every time-step of the computation.



Gate Oxidation



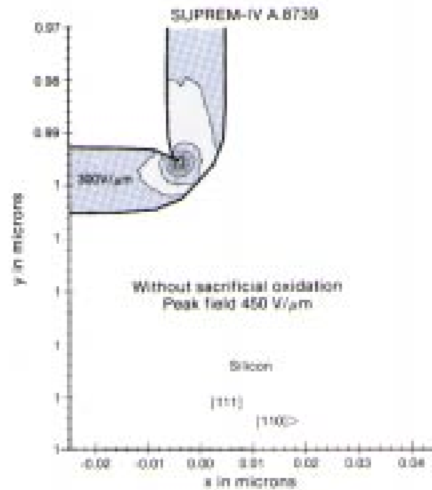
LOCOS

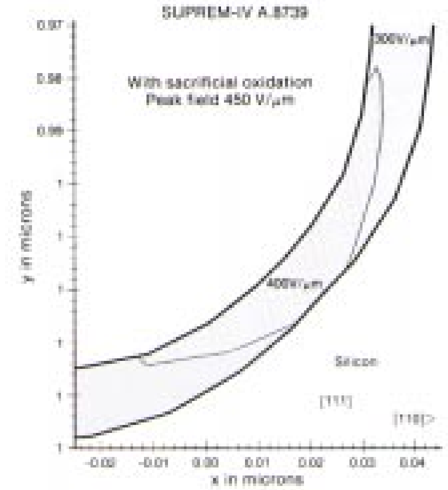
Professor William G. Oldham
University of California at Berkeley

Integrated Technology Computer-Aided Design (TCAD)

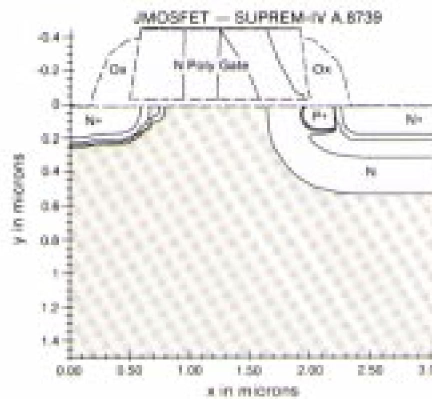
SUPREM 4 contains advanced kinetic models for processes such as nonplanar (trench) oxides and source/drain diffusions engineered to reduce hoi carrier effects. The figures show typical structures with SUPREM 4 coupled directly to PISCES 2 to extract pertinent electrical parameters. The upper figure compares the critical electric field strength for a corner after a single 900°C dry oxidation and a smoother corner which has been oxidized, stripped, and reoxidized. The contour lines and peak electric field values indicate the importance of having accurate models for stress-dependent local oxidation. These results can help improve fabrication of more reliable oxides for DRAMS and isolation. The second figure shows the process and device simulation of a novel MOS device with local ion implantation used to reduce hot carrier effects at the drain. Based on accurate 2D profiles from SUPREM, the electrical characteristics obtained with PISCES 2 are shown. Previous ID profiles used for quasi-2D analysis were inadequate to match experiment. The PISCES code now includes new mobility data and an accurate avalanche generation model. Excellent substrate current predictions can now be obtained for 0.5 µm channel length devices — both conventional and LDD configurations.

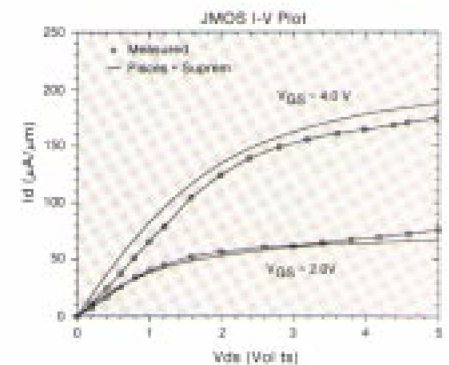
Professors Robert W. Dutton and
James D. Plummer
Stanford University





SUPREM 4 simulations of local oxidation with contours of electric field computed using PISCES 2.
(Left) single-step oxidation showing 1450 V/µm peak electric field.
(Right) two-step oxidation showing 450 V/µm.





Process and device simulations of the JMOS device designed to reduce hot carrier effects at the drain by creating a local buried JFET.
(Left) SUPREM 4 cross section showing p+ island to drive the current subsurface into the JFET.
(Right) Comparison of experimental results and PISCES 2 output using SUPREM 4 impurity profiles.

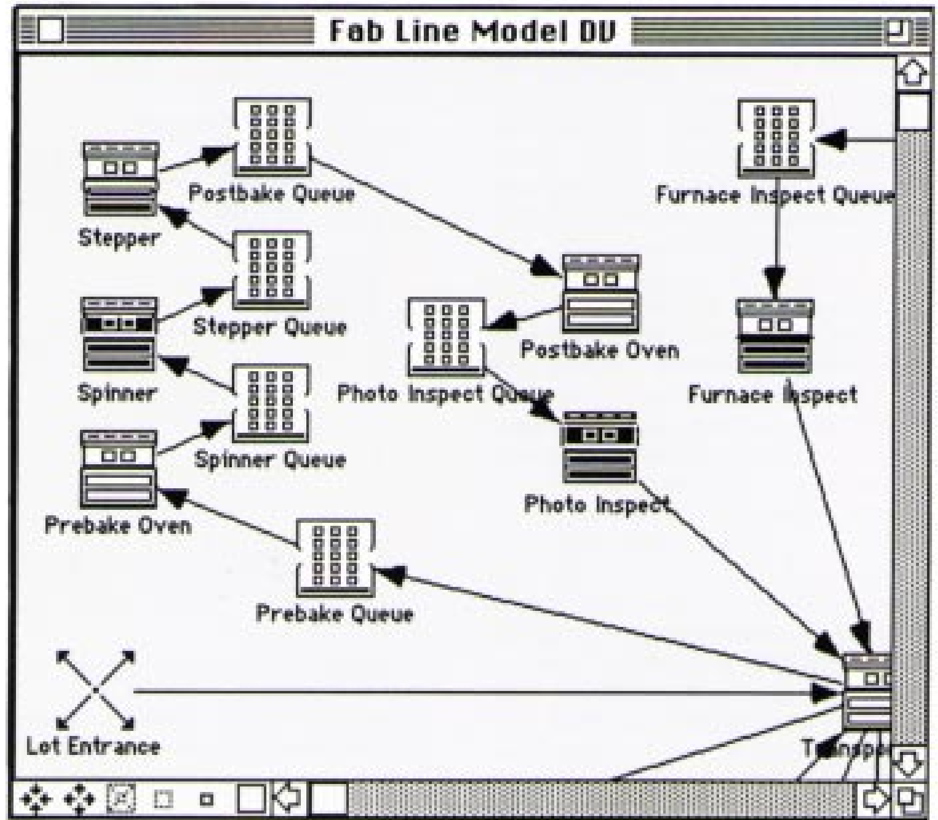
CASM

Computer-Automated Semiconductor Manufacturing (CASM) is a significant new research thrust that includes programs aimed at developing the tools needed to automate the IC manufacturing process.

Substantial automation of both wafer processing and factory management will be needed to obtain the degree of manufacturingprocess control required to meet the goals of the industry for the 1990s. The differing approaches taken by university investigators for SRC CASM research have resulted in a matrix of complementary programs to develop some of the building blocks for establishing such automation. The process/circuit modeling activities that have long been the strengths of the programs at Stanford and UC/ Berkeley are now being extendedinto the critical process/equipment modeling required for real-time, closed-loop control and integration of fabrication. A completely integrated and automated semiconductor fabrication facility is being modeled, based on a fundamental understanding of the unit processes and the development of an associated factory simulation (virtual factory) that will allow the testing of the manufacturability of a design before committing it to silicon.

At the University of Michigan, research is more sharply focused on equipment/process modeling and, in particular, on the development of sensors for in-situ monitoring of the parameters needed for real-time process control.

The contribution to CASM by Carnegie-Mellon addresses the techniques needed to analyze masses of data generated by the many testing/ characterization facets of the wafer fabrication process. The focus is on sophisticated statistical tools for establishing correlations between sets of parameters, such as wafer test results and process conditions.



MODES Representation of a Portion of a Fabrication Line.

Programmable and Virtual Factory

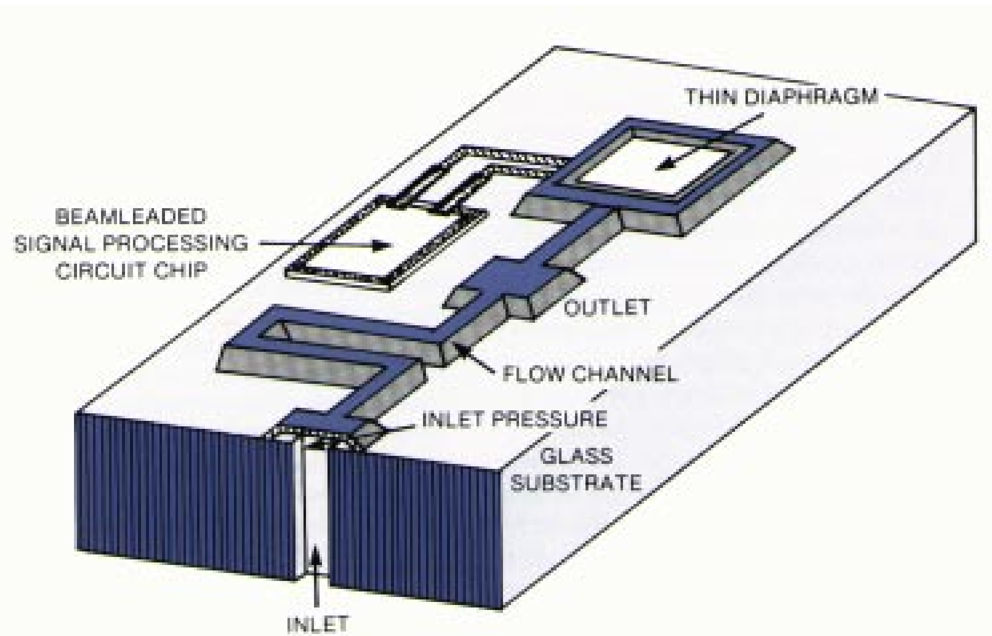
The objective of this program is the development of tools and methodologies that will enable reproducible, high-yield, low-cost, flexible manufacturing of VLSI circuits. The approach being used is to simulate and, then, to control a computer-integrated manufacturing (CIM) line. The benefit of this research will be the prediction and control of process, device, and circuit parameter distribution resulting from normal manufacturing variations. Two representations of a VLSI fabrication facility will be created: the programmable factory and the virtual factory. The programmable factory is an integrated system of manufacturing equipment, sensors, and computer hardware and software in an actual fabrication environment. The virtual factory represents a factory that can be run in simulation on a computer workstation. A wafer fabrication factory simulator, MODES (Modeling Discrete Events Simulations), has been developed. MODES is a CAD tool for wafer fab design, optimization, and operation that will also double as a prototyping vehicle for the CIM interface to the Programmable Wafer Fabrication Line. It is being developed as a demonstration platform for exploring representations and techniques for semiconductor manufacturing modeling and simulation. This software uses a mixture of graphical and procedural specification to represent the manufacturing line and its behavior.

Professor Krishna C. Saraswat
Stanford University

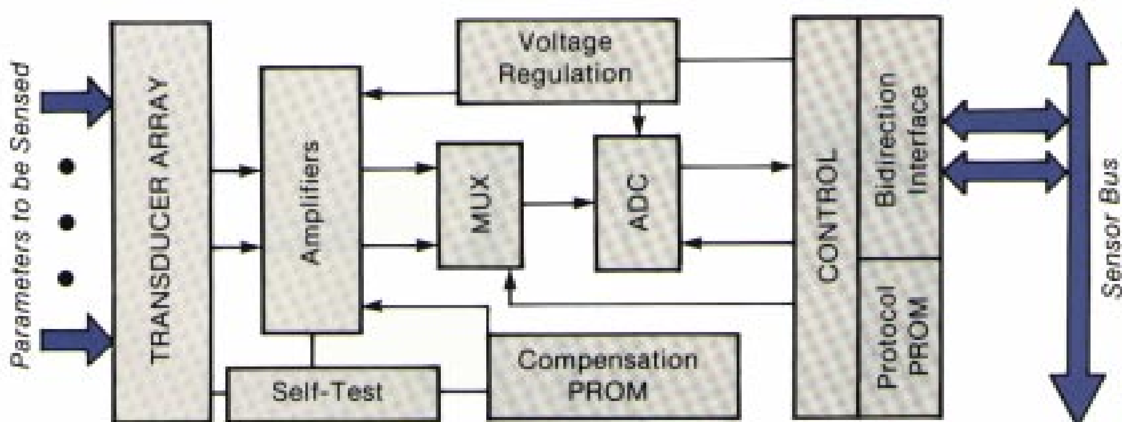
Sensors for Process Automation

Achievement of the real-time process control needed to meet the stringent requirements of automated submicron manufacturing will require in-situ measurement of many process parameters. The Automation in Semiconductor Manufacturing Program at the University of Michigan is developing silicon-based integrated sensors to meet this need, with emphasis on the reactive ion etching (RIE) process. First prototypes of monolithic integrated sensors for gas pressure, flow, and composition have been completed for use in reduced-pressure etch systems. A standardized sensor interface has also been defined for these devices and is being integrated. The bidirectional interface transforms the sensor chip into a smart peripheral, which features self-testing, flexibility in features, rapid response, and high precision, using PROM-based digital compensation. Expert-system software has been developed to allow control decisions based on data from sensors, from in-situ wafer monitoring, and from downstream cells employing machine vision.

Professor Ken D. Wise
University of Michigan



An Integrated Pressure-Based Microflow Sensor for Semiconductor Process Gases.



Block Diagram of an Integrated VLSI Sensor for Use in Automated Manufacturing.

VLSI Architectures

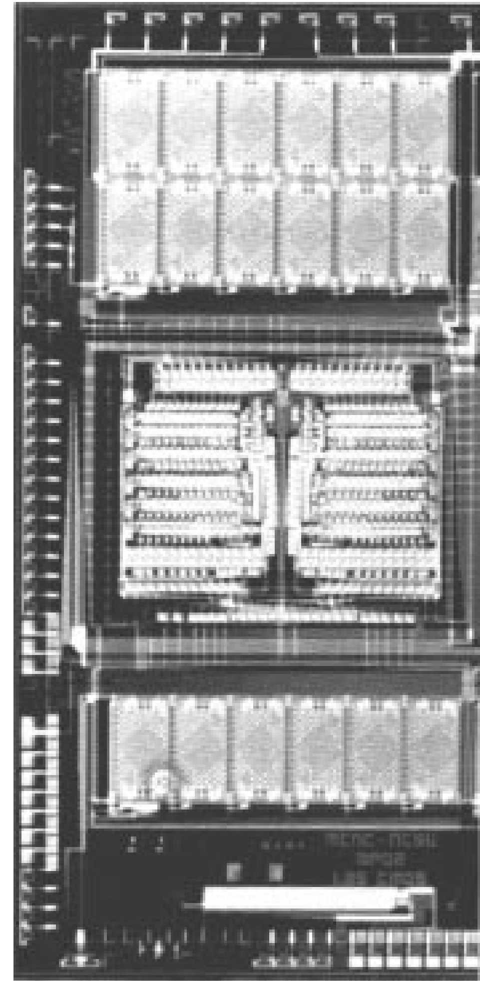
Research in VLSI architectures is intended to explore high risk/high payoff opportunities where novel structures can exploit the inherent complexity of VLSI systems to achieve new functionality and/or enhanced performance. As an example, connectionist architectures may offer new computational paradigms, but they also provide a challenge to VLSI design because of their high connectivity requirements (see research highlight from Professor Hammerstrom). VLSI architectures are also driven by data input/output constraints In many image processing problems, data are naturally available in scan-line order; and, thus, the architecture must be matched to this constraint in order to obtain optimum performance (see research highlight from Professor Liu). Special computational procedures are often so widely used that consideration of special architectures to expedite execution is warranted. An example is the general area of finite element computation that requires a significant commitment of computing resources for many applications. A new architecture that appears to be nearly optimum for the operations required in the solution of finite element problems has been devised and is described in the highlight from Professor Preparata.

It often turns out that the synthesis of an effective VLSI design requires the conduct of interactive architectural tradeoffs from the system level down to the bit level. In the design of a chip to be used in an adaptive sidelobe canceler system having many applications in communications, it was found at the University of Southern California that a novel arithmetic scheme, which allows only two nonzero bits in the binary word, provides a very efficient and effective VLSI realization.

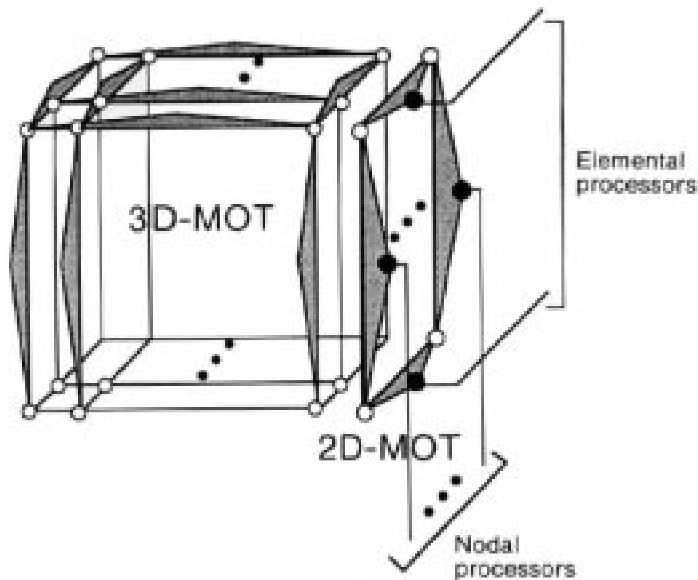
An Architecture to Solve Partial Differential Equations

The numerical solution of partial differential equations is the essence of many of the problems in applied engineering and physics. The pervasive application for finite element analysis as a numerical method for an important class of such problems motivates the identification of a computing structure naturally suited to the task. SRC researchers have proposed an architecture appropriate for a dedicated, highly parallel finite element machine that is efficient for diverse tasks. The architecture is a 3D mesh of trees augmented with an additional plane of processors (organized as a 2D mesh of trees), some additional connections, and a few matrix registers. This architecture (with nodal processors and elemental processors located at the roots of the trees in the additional plane) can be used to compute the elemental stiffness matrices and load vectors, and to assemble the global stiffness matrix and load vector from their elemental constituents. The same architecture can be used to solve the resulting linear system of equations by Newton's method and can also be hybridized with a systolic array to achieve a processor/time (or area/time) tradeoff.

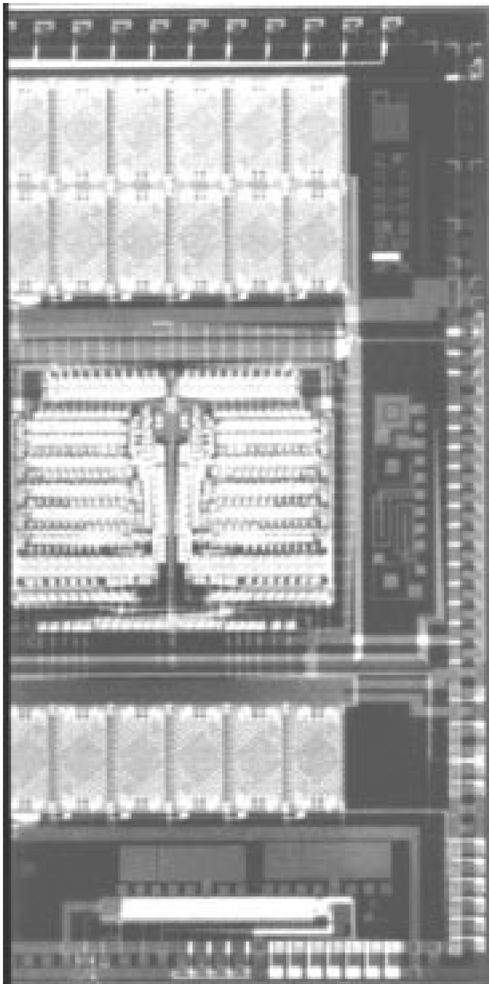
Professor Franco P. Preparata
University of Illinois



VLSI Design for rasterized 2D FET



Architecture proposed by researchers at Illinois for Solving Partial Differential Equations.



rom North Carolina State University

VLSI Architectures for Multidimensional Problems

Computational architectures for multidimensional problems are often driven by the need to handle scan-line input data, and these architectures must often perform operations on global data. Example applications include problems in image processing, computer vision, linear algebra, and signal processing. This research is providing a basis for translating multidimensional computational problems, constrained to utilize scan-tine data in real time into equivalent one-dimensional computational problems. Multidimensional Shuffle Exchange networks (and dual Butterfly networks) can be shown to provide asymptotically optimum performance for many problems, and these networks are serving as a basis for this research. Necessary and sufficient conditions for rasterization for problems involving general data permutations on multidimensional Shuffle Exchange Networks have been developed, and a sufficient condition for rasterization of general computation is available. One of the benefits of the theory is that matrix transposition associated with the two-dimensional FFT is no longer required.

A VLSI design for rasterized 2D FFT computation has been completed and is in fabrication (see microphotograph at left). The chip contains approximately 152K transistors and is being fabricated in 1.25 μm CMOS technology at the Microelectronics Center of North Carolina. It is projected that an interconnected set of these chips can perform two 256 x 256 FFT transformations in real time (30 frames per second).

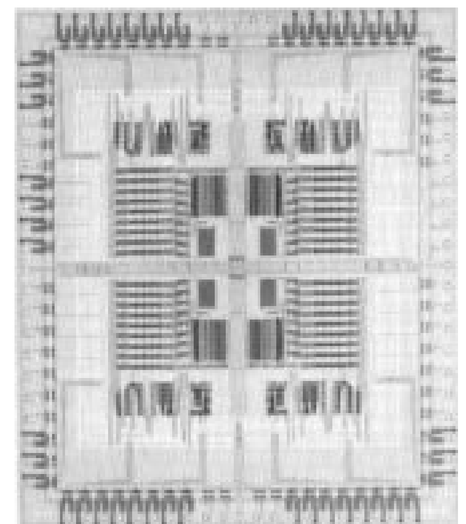
A second VLSI design based on the general theory will provide a novel bit-level rasterization for some of the geometric feature extraction calculations required in computer vision. The new architecture utilizes a binary tree rather than the conventional quad tree and takes advantage of information expansion associated with feature extraction. Other benefits include the achievement of bit-level concurrency, removal of the requirement for a frame buffer, and a pipeline structure suitable for VLSI implementation. It appears that a single chip implemented in 1.25 micron CMOS will perform feature extraction for a 512 x 512 image in real time.

Professor Wentai Liu
North Carolina State University

Interconnection Structures for VLSI-Based Connectionist/Neural Networks

Important practical problems are often incompletely specified and characterized by many weak constraints, requiring large solution spaces. Visual processing and speech recognition are problems of this kind. Processing such large data spaces significantly overwhelms traditional sequential, or low-level parallel computation. Recently a new style of massively parallel computation has been receiving attention as a candidate for processing these large dimensional spaces. Massively parallel networks — often called connectionist or neural network models — are characterized by a number of highly connected, simple processors and are loosely based on biological information processing systems. Fundamental computational limitations are being reached in the size of networks that can be emulated. This computational wall is due to the extreme connectivity of these networks (generally every node, in even a moderate-sized network, has hundreds of input and output connections). SRC researchers are examining radically new silicon-based computing structures. A set of interconnection architectures and hybrid analog/digital computation techniques have been developed that are optimized for connectionist/neural network emulation in VLSI. An Intel iPSC Hypercube-based simulation environment has been created that allows simulation of these architectures, both for correct function and for performance in the presence of typical silicon defects.

Professor Dan Hammerstrom
Oregon Graduate Center

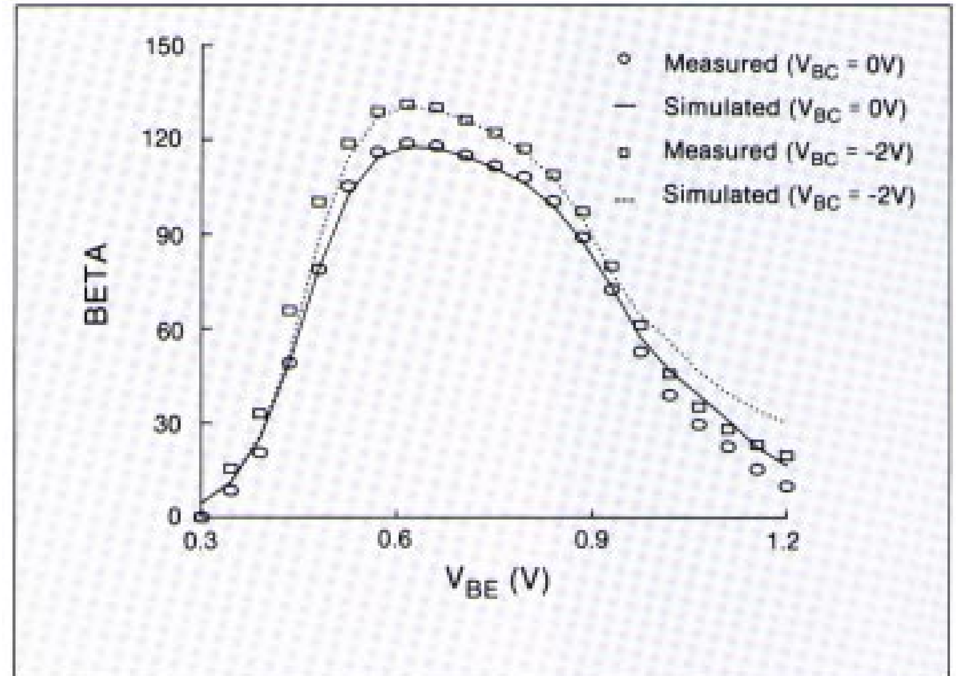


Chip showing "APN" Silicon Connection Processing Nodes from research at the Oregon Graduate Center. (see inside Back Cover)

Bipolar Technology

Bipolar integrated circuits have recently benefited from the continuing shrink in minimum feature size and oxide isolation technology, together with fundamental advances made in cooling technology for high-level packaging; therefore, bipolar integrated circuits will continue to provide the highest speed performance of existing silicon IC technologies. The thrust of advanced bipolar technology is the use of dielectric isolation to reduce parasitic resistance and heterostructures to improve emitter performance. The use of these advanced structures has created the need for new bipolar transistor models with more sophistication than existing ones. The SRC has reinitiated research efforts to produce models capable of adequately predicting the large signal behavior of the new submicron bipolar devices.

The 1994 performance goals lead to a density of $1 x 10^6$ transistors/cm^2 with a 25 picosecond pair delay, a 1 kilowatt/cm^2 power dissipation with a power-delay product of 10 femtojoules per gate. This will require the use of the 0.25 micron minimum-feature-size devices.



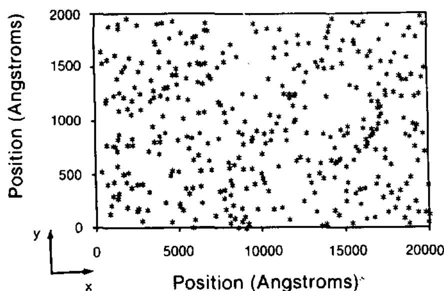
Mixed-Mode Bipolar Device/Circuit Simulation

It is now apparent that reliable technology CAD for VLSI must include mixed-mode device/circuit simulation to predict IC reliability and yield as well as performance. The University of Florida Program, which has stressed physics-based transistor (BJT) modeling for bipolar circuit simulation, has begun the development of a novel seminumerical mixed-mode simulator, MMSP ICE, for advanced bipolar technologies and, ultimately, for BiCMOS. A preliminary version of MMSPICE, in which a physical charge-based BJT model is written directly into SPICE2G, will be available in 1988. The model is implicitly defined by a system of analytic equations derived from regional carrier transport analyses. The system of model equations is solved simultaneously with the circuit nodal equations by MMSPICE to effect the mixed-mode simulation. The simulator is orders of magnitude more computationally efficient than the more conventional device simulators in which the carrier transport equations are solved totally numerically, yet is largely predictive — subject to the uncertainties in the actual IC structure. The accuracy of the analytic BJT model is commensurate with these uncertainties. In the above figure, measured and predicted (with only minimal parameter extraction associated with the uncertainties) current gains are plotted for a representative advanced-technology BJT. The accuracy of the simulation is excellent and demonstrates the potential of MMSPICE. MMSPICE will be evolved to render it useful for BiCMOS TCAD. Accurate analytical modeling of integrated interconnect signal transmission has been done based on 2D numerical simulations, and seminumerical interconnect models are being readied for implementation in MMSPICE. Accounting for interconnect delay in fast VLSI circuits is now essential for predictive simulation. In the future, other parasitic effects (e.g., latch-up) and reliability physics (e.g., hot-carrier effects) will be modeled and implemented in MMSPICE. MOS and bipolar transistors will be modeled physically but seminumerically, allowing the simulator to be used for predictions for IC yield as well as for performance and reliability.

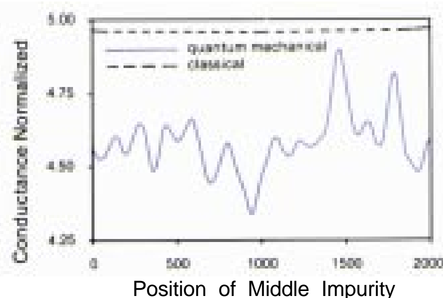
Professor J.G. Fossum
University of Florida

Quantum Effects in Submicron Structures

As the down-scaling of devices continues, quantum mechanical effects are beginning to emerge. One consequence is that devices maybe influenced by statistical effects such as the precise number of dopant atoms that happen to reside within the device, e.g., the base region of a bipolar transistor. Device performance may even depend on the exact placement of dopant atoms.



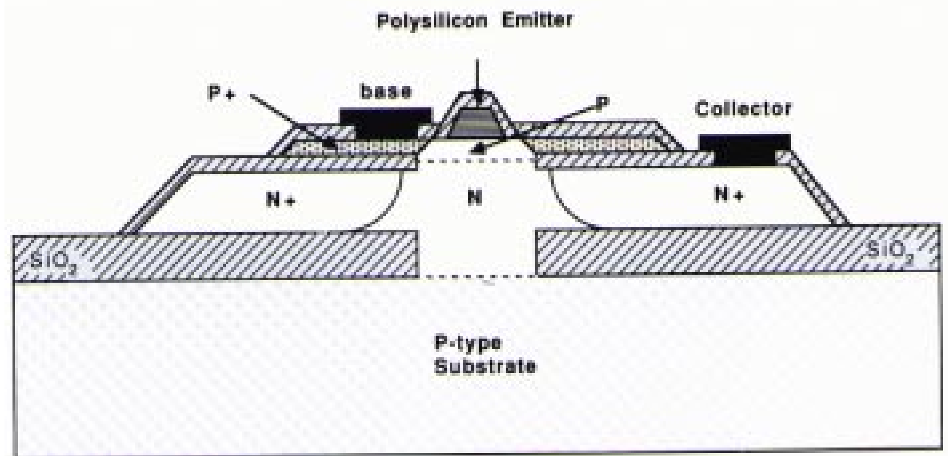
For example, one random configuration is shown above of dopants in an ultrasmall, 0.2 x 2.0 µm resistor. The low-temperature resistance, computed by a quantum device model developed at Purdue, is about 5 kΩ, which is about 10% lower than the classical value.



Position of Middle Impurity

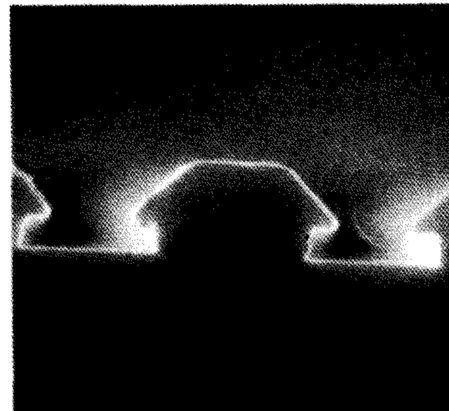
Even more striking is the ± 20% variation in resistance (see illustration) that occurs as a single dopant atom is moved. As device dimensions continue to shrink, these quantum effects will begin to limit device performance, but they offer opportunities to devise a new class of devices that exploit the wave nature of electrons.

Professors M.S. Lundstrom and S. Datta
Purdue University



A Minimum Parasitic ELO Bipolar Transistor

State-of-the-art bipolar junction transistor (BJT) switching speed and unity gain frequency are limited by the transit times of carriers through the device and by the parasitic capacitances and resistances associated with the fabrication technology. The Epitaxial Lateral Overgrowth BJT (ELO/BJT) structure reduces parasitic capacitances by dielectrically isolating the low-resistance collector region from the substrate and the base region. This obviates the need for a traditional buried layer, with ifs attendant parasitic collector substrate capacitance, yet the device is fully self-isolated with no trenches or diffusions required. Parasitic resistances are reduced by keeping currentpaths short, andplacing the highly-doped extrinsic collector and extrinsic base regions in close proximity to the active device regions. The oxide layer covering the lateral portions of the overgrowth provides the dielectric isolation, and the field oxide provides interdevice isolation. The stacked nature of the two overgrowths allow collector, base, and emitter contacts to be spaced as closely as lithography allows, facilitating a small geometry device. Working BJTs were obtained at Purdue with near bulk-quality characteristic in double ELO silicon. In addition, the double ELO technique is adaptable to a wide variety of applications in SOI, sensor construction, buried interconnects, BiCMOS, and dielectric isolation.

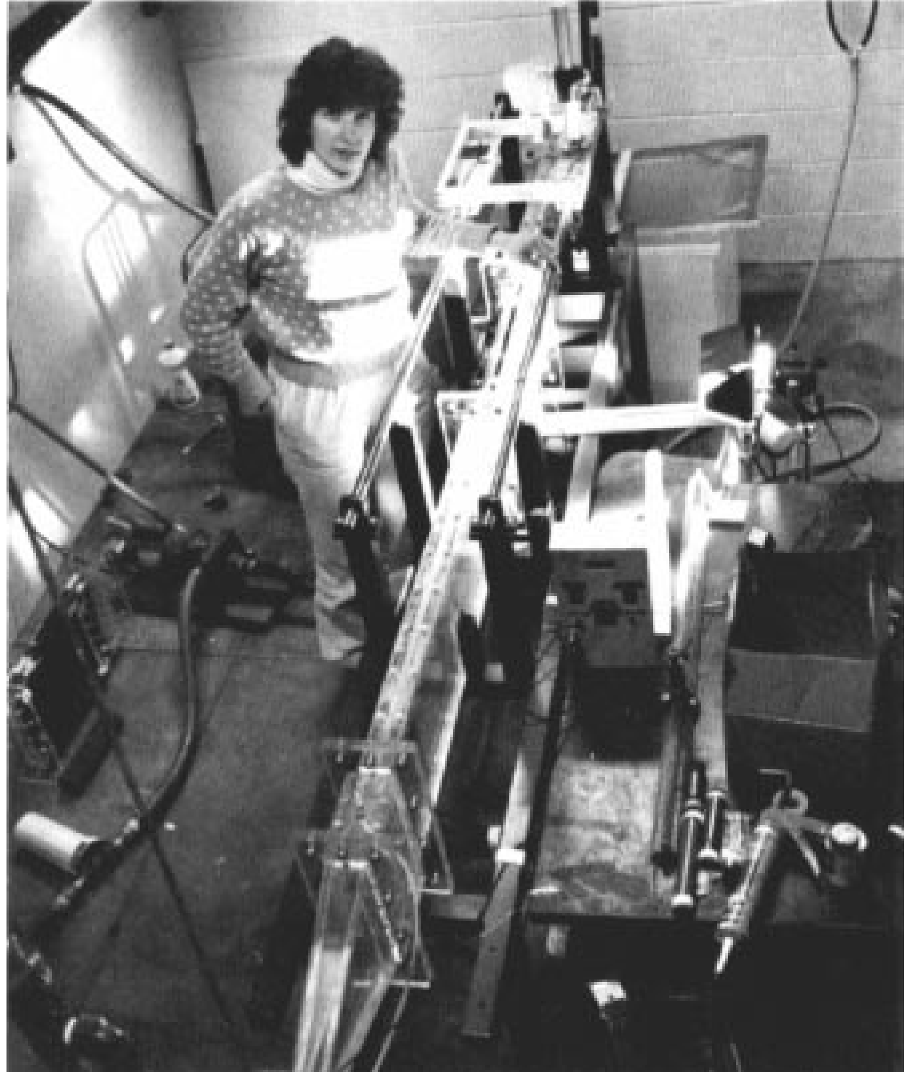


Professor G. W. Neudeck
Purdue University

Packaging

Integrated circuits require packages that interface chips to the outside world. As chips become more complex and performance demands increase, parallel developments are required in packaging technology. In recognition of this need, packaging is the second largest thrust in Manufacturing Sciences. It includes six university groups at Auburn, Stanford, Lehigh, Cornell, Purdue, and Arizona, with research programs ranging from materials characterization to the development of CAD tools for package design.

Research at Stanford has focused on using silicon substrates for high performance interconnections. Auburn is developing a methodology for evaluating package reliability. Lehigh and Cornell are covering both materials and performance aspects of densely packed designs. The Arizona research is bringing package design capability more in line with techniques that have been developed for the integrated circuit chip. At Purdue, emphasis is on building an accurate database of important materials used in packaging.



(Photo courtesy of Kenneth A. Friedman — See photo on page 5.)

Professor Kyra Stephanoff With Test Apparatus

Cooling With Pulsatile Flow

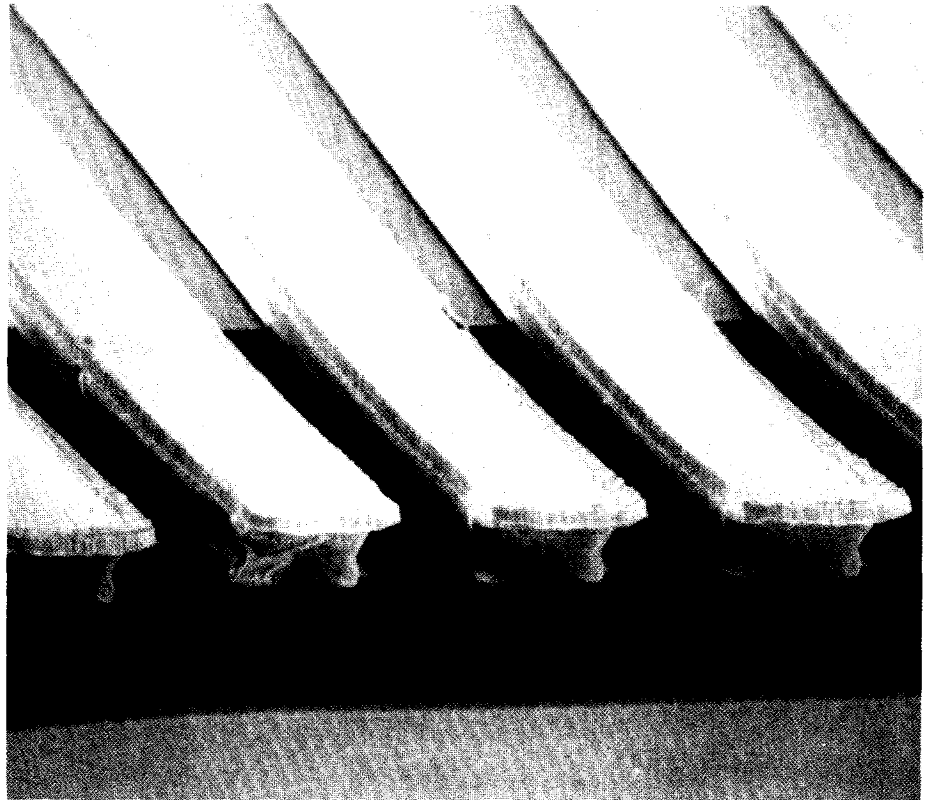
The heat generated by colonies of integrated circuit chips can adversely affect the performance and lifespan of semiconductor devices. Methods currently being used to dissipate such heat have disadvantages and limitations. For example, use of a steady flow of air across multilayer boards to transfer heat away from the circuitry by natural convection will create local hoi spots due to attached recirculatory flows at the leading and trailing edges of the chip carriers. At Lehigh, attempts are being made to improve cooling techniques for low-cost, moderate performance applications; and one method under investigation is a heat transfer process that uses pulsating, rather than steady, air flow. This project is based on the concept that the changes in pressure which occur with periodic air flow reversals can cause the eddies of hot air that collect around chip carriers to be ejected into the mainstream and, hence, swept away from the board. Such air flow reversals prevent stable thermallayers from forming adjacent to the chip carrier surfaces and, consequently, increase the local heat transfer away from the chip. Toward the goal of developing a viable technique for cooling with pulsatile flow, background information was gathered during 1987 from visualization experiments, linear analysis of phenomena, and long-wavelength analysis. A test apparatus was constructed and outfitted with instruments to perform heat transfer experiments.

Professors Kyra D. Stephanoff
and Phillip A. Blythe
Lehigh University

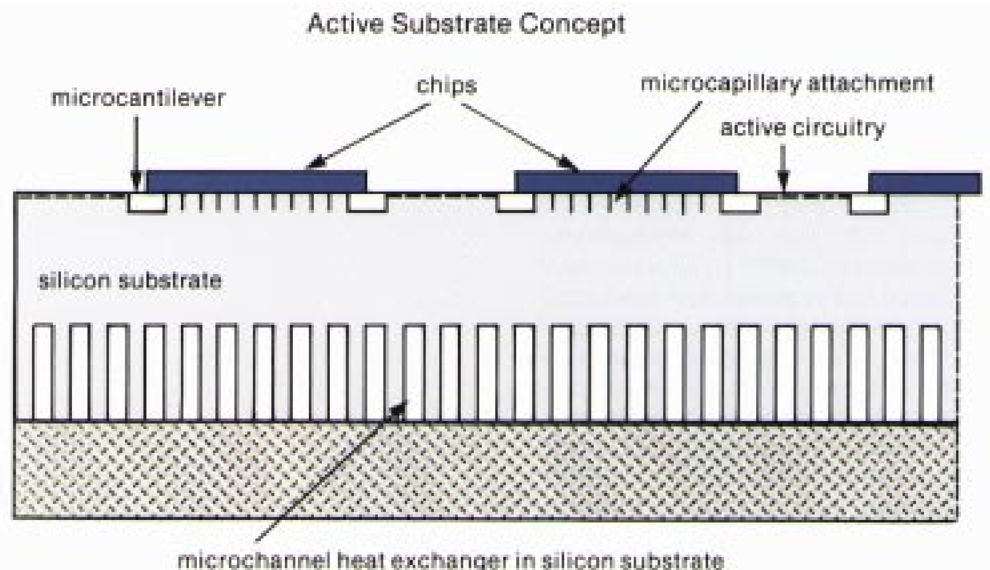
Active Substrate Interconnection Investigations

The Active Substrate approach to system integration employs a silicon wafer as a stand-alone, active, interconnect system where chips are bonded directly to the wafer. For attainment of SRC goals that are pointed toward an interconnect concept allowing 1,000 pin-outs around a 10 mm x 10 mm chip, the Stanford research team of Pease, Hong, and Bravman have been using an Active Substrate configuration to uncover the problems of high-density, multi-chip packaging. This team has originated a concept whereby chips are held down by microcapillary attachment to the active substrate, which can be cooled by the microchannel heat exchangers previously developed in this research project. Chip-to-substrate electrical connections are handled by microscopic cantilever beams distributed around the chip edges; power connections might be made through the microcapillary attachment. Some advantages of the Active Substrate approach are: system interconnects are transferred to a microelectronic environment, chip technology can be optimized for performance and functionality, chip and substrate technologies can be mixed to optimize system performance, and yield problems of full wafer-scale integration are avoided.

Professors John C. Bravman
and R. Fabian W. Pease
Stanford University



Photomicrograph of micromachined cantilevers for chip-to-substrate contacts in an experimental high-density packaging structure. These cantilevers are fabricated by using orientation-dependent etching and controlled-stress metallization and may be able to provide a reversible, compliant contact array that would allow 1,000 pin-outs around a 10 mm x 10 mm chip.



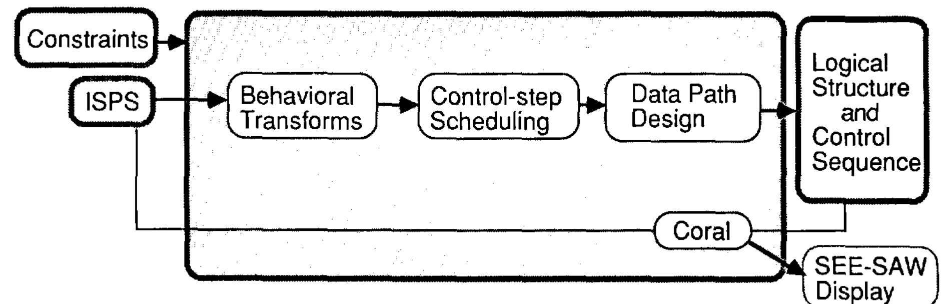
Design Synthesis

Synthesis tools and systems for use in the design process are fundamental to reducing time-to-market and design costs, promoting re-use of design data and knowledge, and supporting efficient evaluation of design alternatives. SRC-sponsored research in design synthesis includes system-level synthesis tools, logic-level synthesis, layout synthesis, array compilation, and synthesis for digital signal processing applications.

Digital System Synthesis

The System Architect's Workbench (SAW) is the result of an ongoing project that is developing a synthesis methodology and a set of supporting CAD tools to bring automation to the system levels of IC design. The methodology begins with a program-like behavioral description of the digital system to be designed and produces a datapath that is specified in terms of registers, arithmetic logic units and busing, and a control sequence. As shown in the figure, the workbench currently provides three main steps for the synthesis process. First, the behavior is transformed by the user. This may involve, for instance, splitting the behavior into several smaller concurrent state machines in response to physical area constraints. Next, the control sequence is automatically designed by scheduling the behavioral operations into control states in response to timing and resource constraints. finally, the datapath (including the registers, arithmetic logic units and busing structures) is automatically designed. The Coral and SEE-SAW programs allow the user to interrogate the automatically produced design through graphical depiction of correspondences between different views of the design. SAW will be used to drive a second component (LASSIE) of the CMU design system that synthesizes a layout from a structural description of a datapath. The SAW software is currently in use and under evaluation in the research labs of several SRC member companies.

Professor Donald E. Thomas
Carnegie-Mellon University



System Architect's Workbench

COSMOS

COSMOS (COmpiled Simulator for MOS), being developed by SRC-sponsored research at Carnegie-Mellon, is a unit delay switch-level simulator that represents a MOS transistor circuit as a network of discrete switches. COSMOS achieves high performance by preprocessing a MOS transistor network into a Boolean description. From this description, a set of procedures is generated to compute the behavior of each channel-connected subnetwork. COSMOS compiles these subnetwork procedures, together with kernel and user interface code, to generate an executable simulation program. The resulting simulator operates an order of magnitude faster than its predecessor MOSSIM II, thus achieving performance that rivals a logic-level simulator while preserving the generality and power of a switch-level simulator.

During 1987, four major improvements were made to COSMOS: (1) addition of fault simulation that combines both concurrent and parallel simulation techniques;(2) implementation of an inferface to allow user-written simulator drivers; (3) addition of a symbolic verification capability; and (4) addition of a test pattern generator that is based on symbolic fault simulation. Fifty copies of the simulator were distributed to university and member company sites for evaluation.

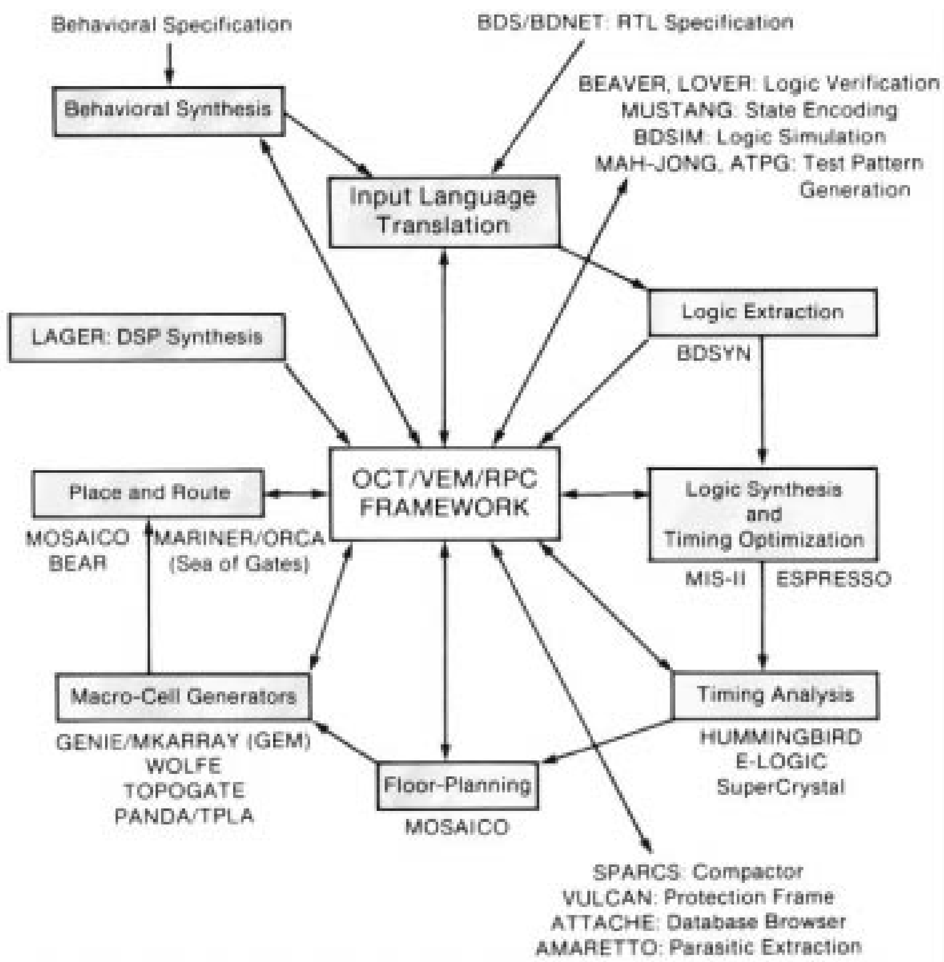
Professor Randal E. Bryant
Carnegie-Mellon University

Berkeley Synthesis System

The Berkeley Synthesis System (BSS) is an integrated design system centered on a framework composed of an object-oriented data manager (OCT), a view editor that provides a unified view interface to tools (VEM), and a remote procedure call capability for distributed computing environments (RPC). As shown in the figure, synthesis starts with a specification in a hardware description language and continues clockwise around the periphery. Individual tools successively refine the description until mask images for a completely synthesized system are obtained. Refinement can be performed interactively, allowing the user *to change design constraints and tool sequencing. Tools read and write the same database, creating new OCT views of a design or annotating old ones. The OCT/VEM/RPC framework allows tools to efficiently access and exchange information.*

During 1987, MOSAICO, the macrocell placement and routing system was integrated info the OCT/VEM/RPC environment, and a parallelimplementation for the simulated annealing floorplanner, PUPPY, was developed. This implementation yields a speedup that is almost linear in the number of processors. Development of the ORCA placement and routing system for sea-of-gates architectures continued, and demonstration of a prototype system is anticipated in 1988. Research in verification resulted in an accurate switch-level timing verifier for synchronous circuits (E-TV) that utilizes a dynamic path evaluation technique. Development of a new building block layout system, BEAR, is underway. BEAR utilizes L-shaped routing channels to guarantee routing completion, and includes 2- and 3-layer gridless channel routers and direct consideration of timing constraints to optimize performance. Additional synthesis research resulted in the development of a deterministic algorithm for synthesizing optimum asynchronous circuits for digital signal processing.

Center of Excellence for IC CAD
University of California at Berkeley



The Berkeley Synthesis System

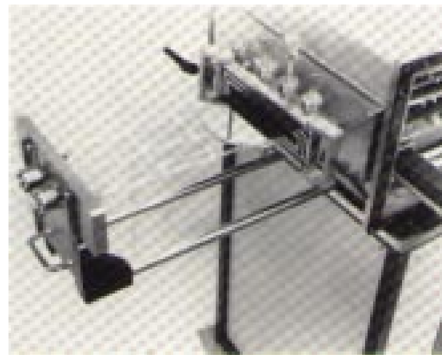
Single Wafer Processing

The strategic direction of integrated circuit fabrication is toward continuous flow single wafer processing with multiple process steps accomplished within the same process tool, i.e., in-situ. To obtain the benefits of this manufacturing method, each process tool will be equipped with sensors and microprocessor control linked to the factory computer to effect real-time control of the process. In the latter stages of fabrication, low thermal budget processes will become increasingly necessary to retain the precise doping concentrations and profiles, and to obtain the performance and reliability of thin layers of dielectric and metal films employed, e.g., for gate oxide, barrier metallization and interconnect.

The benefit of this IC fabrication method is a reduction in the theoretical manufacturing cycle time, further reduction of particulate defects, and active control of production parameters. In addition, the manufacturing line is amenable to technology tuning to accommodate multiple process flows for a limited variety of products. These benefits translate to lower manufacturing cost, dramatically higher throughput, i.e., reduction in actual manufacturing cycle time, and the ability to fabricate a variety of product within the same manufacturing space.

Multiple Process Technology

Side view of RTE CVD reactor, showing' lamp arrays.



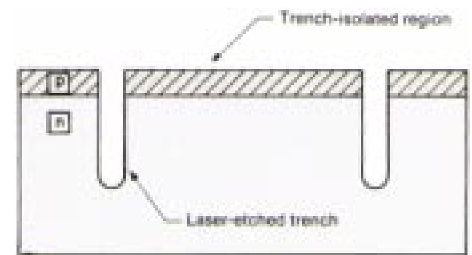
Loading door and cantilever wafer holder.

In-Situ Processing, i.e., the accomplishment of multiple process steps within the same process tool without movement of the wafer, is under investigation at NC State where a rapid thermal processing reactor is being employed for clean, epitaxial silicon or germanium growth, oxidation and nitridation in the same chamber without removal of the wafer between process steps. The RTP reactor is microprocessor controlled, and is currently being instrumented with sensors and actuators for real-time control of the programmed process. Both inner and outer chambers have been designed to operate at vacuum levels for low pressure CVD and clean. Heating is by fifteen one-half kilowatt lamps placed above and below the wafer; the system is designed to handle six-inch wafers,

Professor J.J. Wortman
North Carolina State University

Laser Processing

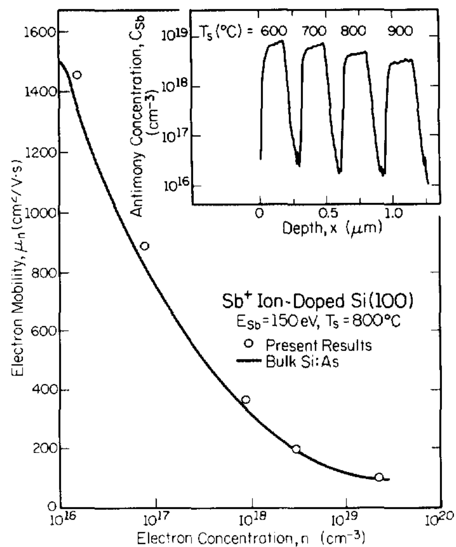
As ICs grow in functional complexity and die size, it becomes more important to develop processing techniques that affect only a limited region of the die and/or wafer; i.e., limited area processing (LAP). LAP is important for operations requiring extreme degrees of processing, such as through-wafer vias, or alteration of a nearly finished product where a low thermal budget is required (such as custom isolation, cutting silicon lines, and custom metallization). Laser direct writing — a rapid, maskless, gas-phase process with micron scale patterning capability — is being investigated at Columbia as a suitable tool for LAP. One successful process is the direct deposition of custom aluminum interconnect from the pyrolytic surface reaction, employing dimethyl aluminum hydride. A second process under investigation is custom trench isolation for active devices. This has been examined by etching trenches in a diffused p-n junction to from an isolated region.



The I-V characteristic of a typical trench-isolated diode indicates good isolation. Electrical characterization of MOS capacitors and Schottky barrier diodes fabricated on top of laser-etched silicon shows that little damage occurs when the power is moderate, indicating that laser-etched material is usable for IC fabrication.

Professor R.M. Osgood
Columbia University in the City of New York

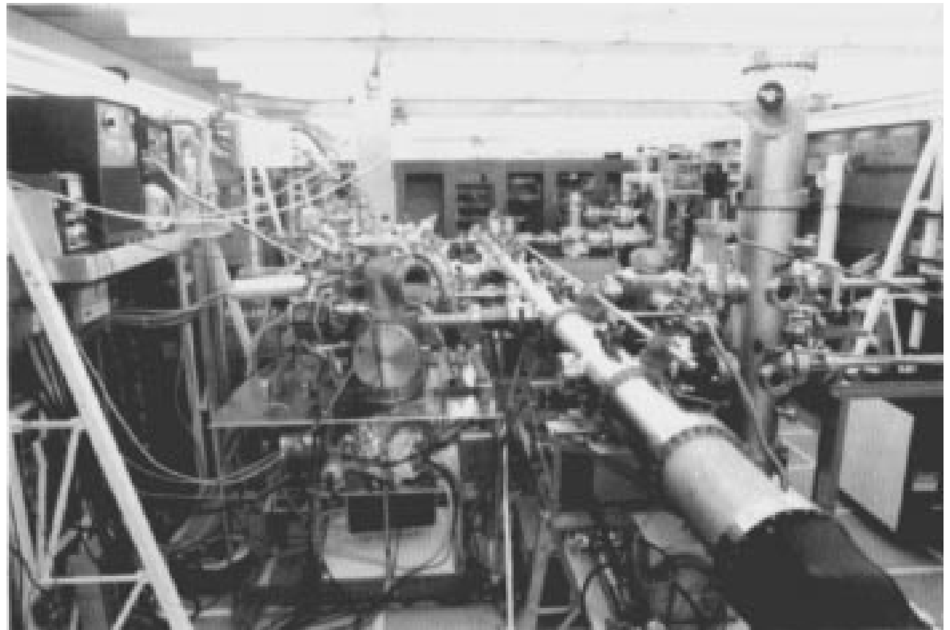
In-Situ Growth Parameters



Mobility of antimony versus concentration, and the use of pulse doping *to* illustrate dopant stability.

Fabrication of submicron microelectronic devices requires precise control of dopant concentration and depth distributions, employing low thermal budget processing. However, most of the common dopants used in IC fabrication present serious problems during film growth due to low incorporation probability and/or pronounced surface segregation, giving rise to uncontrolled profile broadening. The Thin Film Physics Group at Illinois has been investigating the use of low-energy (50-500 eV) accelerated-ion doping during MBE silicon growth to overcome these effects. The experiments are carried out using a new ultrahigh-vacuum-compatible, low-energy ion source developed as a part of the research. Accelerated-ion antimony may be made to incorporate with unity probability into substitutional, electrically active, sites at concentrations up to 3 x 1 0^{19}. The films are essentially dislocation free with no indication of residual ion-induced damage.

Professor J.E. Greene
University of Illinois



Five station Integrated Processing Facility for development of single wafer integrated processing technologies at Research Triangle Institute.

Low Temperature Silicon Oxynitride Technology

Single wafer low temperature processing with multiple process steps performed in the same tool will be the hallmark of future integrated circuit fabrication. The next generation ICs will require the use of smaller features and thin films with improved reliability. Research conducted jointly at RTI and NC State is directed toward development of high-reliability, low-temperature silicon oxynitride films in a tool that ultimately is capable of performing additional process steps. By the use of remote plasma-enhanced CVD, high quality gate dielectrics have been formed on silicon at temperatures as low as 300°C. The process can be used lo clean and deposit films (oxide, nitride, and controlled-composition stoichiometric oxynitride) in a clean ultrahigh vacuum compatible environment, and then transport the wafer in vacuum to an analysis station. The deposition station accommodates in-situ, plasma-enhanced surface cleaning together with in-situ surface characterization via reflecting high-energy electron diffraction (RHEED). These features will ultimately make direct, immediate feedbackpossible for real-time process control.

Dr. James A Hutchby
Research Triangle Institute

Professor Gerald Lucovsky
North Carolina State University

Reliability and Yield Enhancement

The Clemson contract was one of the first Manufacturing Sciences programs responding to the high priority placed on IC reliability research. It has focused on three reliability issues: aluminum electromigration, charge injection into dielectrics, and electrostatic discharge. Most recently the emphasis has extended to reliability models for use in the design process to predict device reliability before wafer fabrication. Work has been started on developing such a model for the electromigration mechanism at Clemson and at Cornell.

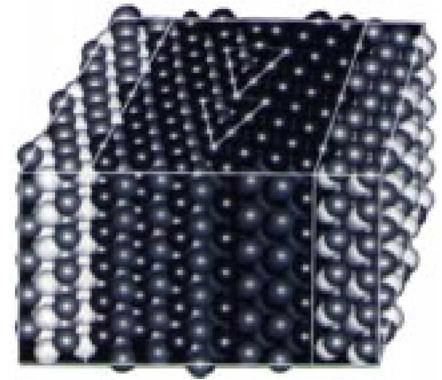
Yield enhancement research at Research Triangle institute and the Microelectronics Center of North Carolina has been largely concerned with the study of particulate contamination, both in the clean room environment and as a more fundamental study of the behavior of submicron particles in liquids and gases.

Yield Enhancement research at the University of Illinois has concentrated on optimization of reconfiguration design methods.

Simulated Electromigration

Diffusion along grain boundaries is an important mass transport process in many integrated circuit phenomena. In particular, the migration of impurity and metal atoms in metallization levels is a precursor to electromigration failure. This is a common failure mechanism for interconnects that are stressed at high current densities for extended periods of time. A simulation, using the techniques of molecular dynamics to study the diffusive properties of grain boundaries at an atomic level, is being used at Cornell to investigate parameters that affect the diffusion rates and activation energies in different kinds of grain boundaries. A metal grain boundary is simulated on the computer (CNSF IBM 3090-600E) by placing several hundred atoms on the lattice sites of a chosen geometry and then relaxing them to minimum energy positions. This gives the static structure of the boundary (see accompanying figure). Random velocities are then assigned to the atoms, and the trajectory of each atom can be followed in time as it is repulsed and attracted by its neighbors. At temperatures greater than one-half T_{melt}, atoms in the grain boundary region become quite mobile, forming Frenkel pairs as vacancies are created and hopping from lattice site to site within the boundary. By calculating the distances that different atoms migrate at different temperatures, a diffusion coefficient and activation energy for the system can be determined.

Professor Edward D. Wolf
Cornell University



A high angle tilt boundary in a body-centered cubic (bcc) lattice. Each sphere represents an atom sitting on its lattice site. The kite-like structures in the middle mark the boundary region where the two crystals come together. The atoms in the central portion are free to move in the dynamic part of the simulation; the walls of atoms on the left and right are held fixed and serve to contain the motion.

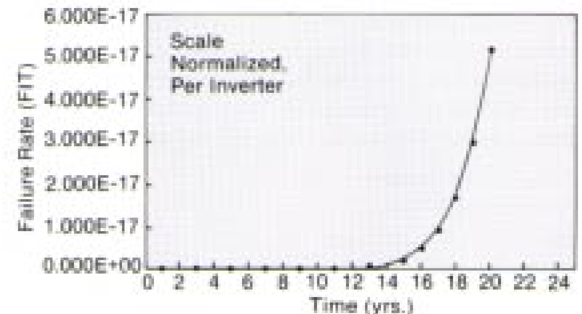
Reliability Analysis

A CAD tool called RELIANT has been developed to analyze a layout for susceptibility to electromigration failure and to predict the interconnect failure rate. Taking input from a manufacturer's CAD system, life test data unique to the process (obtained from test vehicles or drop-ins) are combined with layout data unique to the design to provide reliability assessment with less need for conventional stress testing. The applicability of simulated reliability testing was demonstrated by using RELIANT on an actual design in production at an SRC member company. RELIANT is the first of several planned reliability simulation packages that will include the effect of defects, which result in infant mortality failures, and wearout mechanisms such as electromigration.

Professor K.F. Poole
Clemson University

Features of RELIANT Analysis

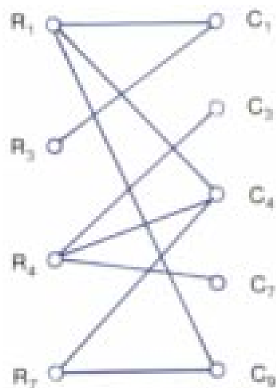
- *Measured data used in analysis*
- *Is an open architecture CAD package*
- *Model data extracted from design data base*
- *Circuit analyzed under real operating conditions*



CMOS Inverter Failure Rate vs. Time

Analysis of Spare Allocation and Reconfiguration to Increase Yield

If VLSI chip sizes are to increase substantially, approaches to design and manufacturing are needed that tolerate or avoid defects, and, thereby, provide for yields greater than those which are now possible with very large chips and wafer-scale integration. One approach to a solution of this problem is through design for yield enhancement by means of restructurable interconnect, logic, and architectural components. A project at Illinois has focused on the development of a computer-aided analysis tool for evaluation of alternative reconfigurable architecturaldesigns. Graph-theoretic models of hierarchical reconfiguration schemes have been developed and analyzed. Based on these models, algorithms for reconfiguration have been developed and implemented. One example application of these algorithms, as illustrated below,



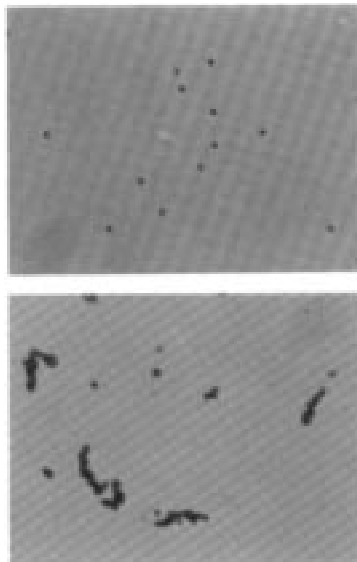
Bipartite description

has been the development of highly efficient heuristics for reconfiguration of large memory arrays in the presence of multiple memory cell defects, using spare rows and columns of cells. Work is currently underway to incorporate the reconfigurability analysis into an architectural-level performance, yield, and reliability evaluation environment.

Professor W. Kent Fuchs
University of Illinois

Particle Removal from Silicon Wafers

Quantitative evaluation of the effectiveness of various cleaning solvents for removing particulate contaminants from Si wafers has revealed that polar liquids are much more effective than the Freons. Ultrasonic and hydrodynamic (shear stress) cleaning systems were developedat RTI for measuring cleaning efficiency and force of adhesion of micron- and submicron-sized particles on Si wafers. Results show that in addition to van der Waal's and electrostatic forces between particles and a wafer, hydrophobic/hydrophilic interactions also play a major role in the cleaning process. For example, the passage of a wafer contaminated with 1 µm polystyrene latex microspheres through the air-water interface resulted in particle agglomeration on the wafer surface. The following photomicrographs show a silicon wafer before and after immersion in a Di-water bath.

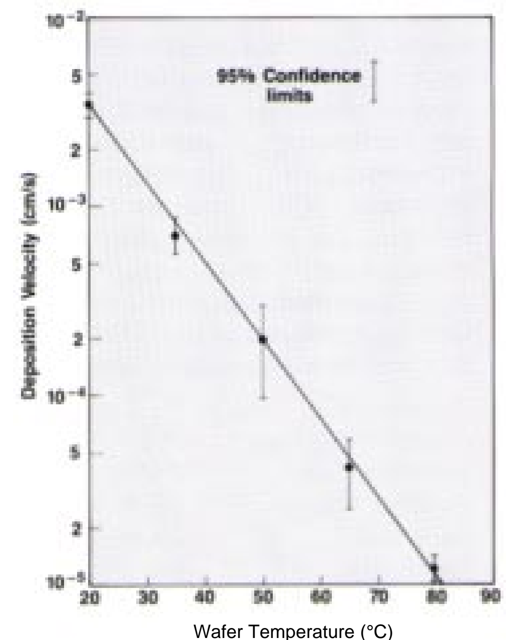


Single particles were found to migrate along the wafer surface to form islands with large clusters of particles. Significant differences in the cleaning efficiency and the mechanism ofparticle detachment were observed when inorganic (SiO_2) particles were compared with organic (polystyrene latex) particles of the same size. Both ultrasonic and hydrodynamic cleaning techniques were found to be capable of achieving high cleaning efficiencies for µm-size particles from Si wafers.

Studies at Microelectronics Center of NC and Research Triangle Institute

Aerosol Particle Deposition on Heated Wafers

Objects warmer than the ambient air are surrounded by a particle-free space because of thermophoresis and thermal convection. This interaction can be used to protect wafers from particulate contamination in both storage and processing. The following graph plots the reduction in particle deposition velocity (particle surface flux and ambient particle concentration) brought about by heating wafers exposed to polystyrene latex spheres suspended in a particle deposition chamber built as part of SRC-sponsored research at the Microelec-



Wafer Temperature (°C)

tronics Center of North Carolina. Simply raising the wafer temperature by 30°C reduces the particle deposition velocity by an order of magnitude. This thermal shielding effect can be useful in planning process procedures. For example, wafers loaded into a vacuum chamber, then fast-pumped and fast-vented, collect an order of magnitude more surface particles than those that are heated to 30°C above ambient for this same procedure in the same apparatus. This particle shielding property is most effective for aerosol particles in the 0.1 to 1.0 µm size range.

Dr. Robert Donovan
Research Triangle Institute

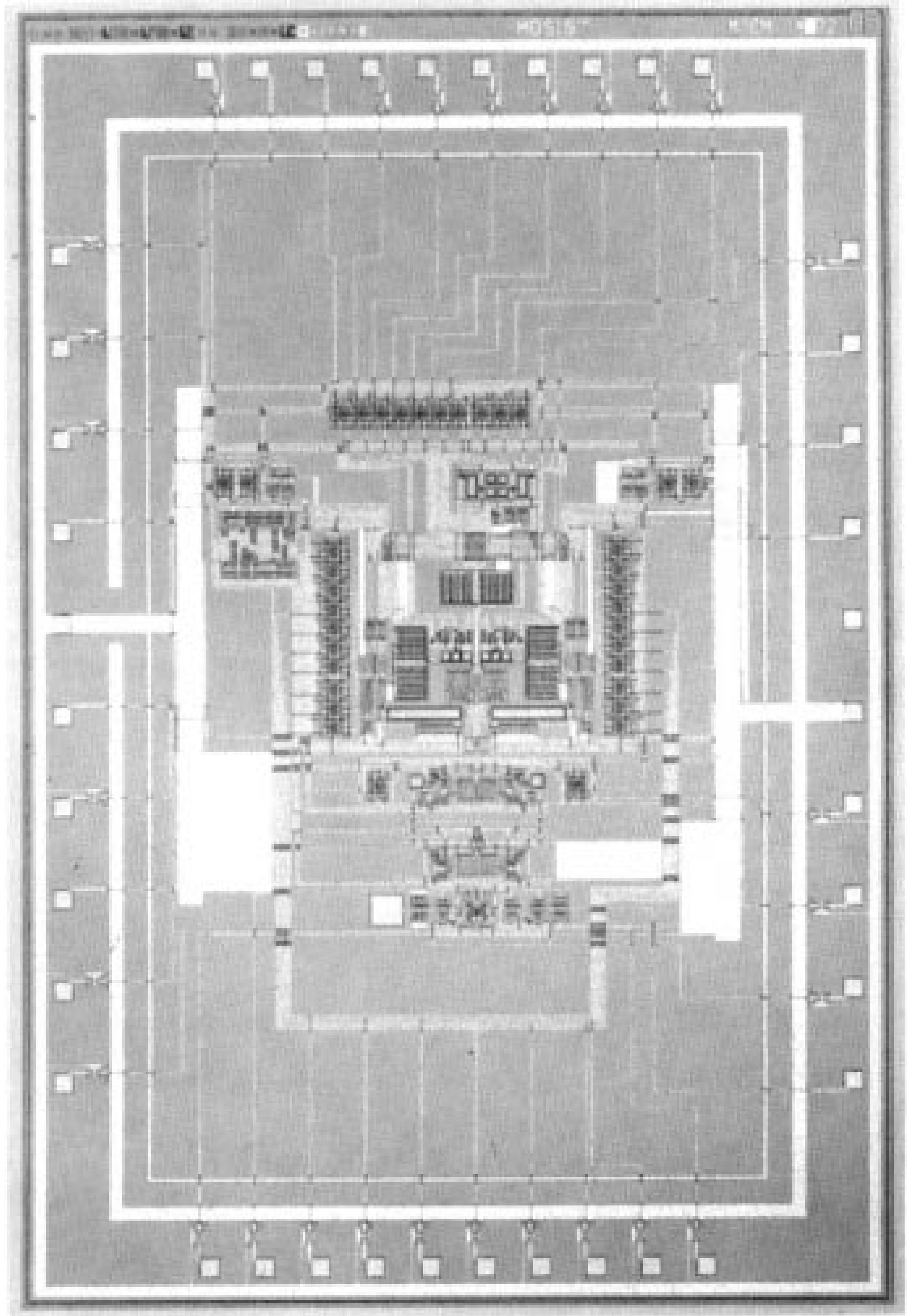
Analog ICs

The complex task of designing analog and mixed analog/digital integrated circuits has been, in general, inadequately supported by computer-aided design tools and systems. SRC research is addressing factors that ameliorate the continuing complexity of the task as the demand for higher performance and more accurate circuits for digital signal processing applications and high precision analog increases.

At Stanford, research directed by Professor Bruce Wooley focuses on the design of oversampled A/D converters. An efficient simulator for sampled-data systems has been developed that is capable of analyzing both the spectral nature of quantization noise and the influence of practical circuit impairments on system performance. Application of the simulator has resulted in the successful design and implementation of a second-order, sigma-delta modulator in a 3 μm CMOS technology. Modulator performance is summarized in the following table.

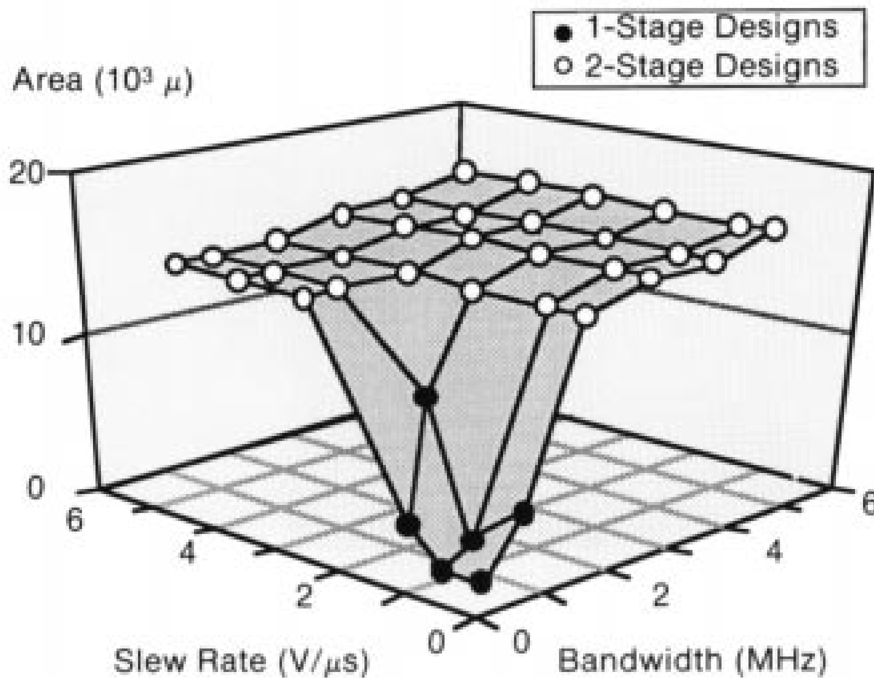
Technology	*3 μm CMOS*
Oversampling Ratio	*256*
Sampling Rate	*4 MHz*
Dynamic Range	*89 dB*
Peak SNR	*79 dB*
Supply Voltage	*5 V*
Power Dissipation	*12mW*
Area	*0.77 mm^2*

Research in continuous-time analog design for MOS VLSI led by Professor Mohammed Ismail at Nebraska has resulted in the fabrication and evaluation of several circuits that demonstrate superior performance to digital switch capacitor circuits for high frequency applications. Future research will focus on exclusively MOS-domain design methods for continuous-time analog circuits and development of on-chip tuning systems.



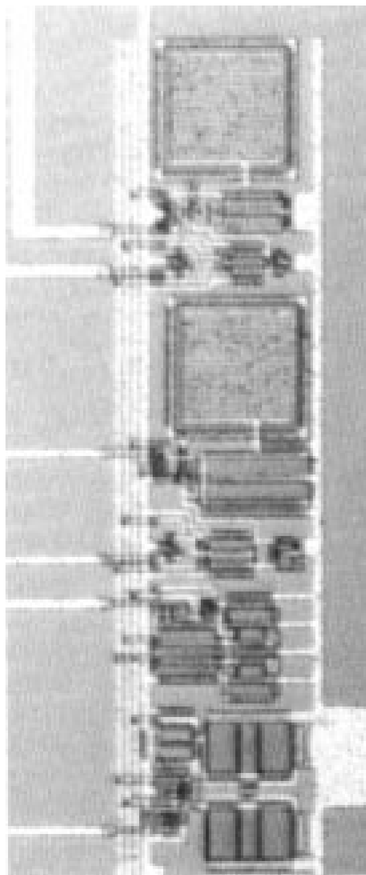
At MIT, a pipelined, self-calibrating A/D converter has been implemented in CMOS technology as shown in the die photograph above. Both loop gain and loop offset errors are calibrated by an on-chip capacitor array and D/A converters. With the incorporation of this self-calibration, it is possible to operate the converter so that only two settling times of the operational amplifiers are required for each bit decision. Projected performance of a 2-stage pipeline is 16 bit resolution at a sampling rate of 200 kHz. Plans include use of this architecture as a test vehicle for a new high performance BiCMOS technology.

Professor Hae-Seung Lee
Massachusetts Institute of Technology



Analog Circuit Synthesis

System-level applications increasingly incorporate analog subsystems; hence, CAD tools that support synthesis of mixed analog/digital circuits are critically needed. A major effort is underway at CMU to automate the syntheses of full-custom analog cells. Work to date has focused on the development of a knowledge-based framework for behavior-to-structure synthesis with the goal of generating sized, topologically correct circuit schematics from a set of process and performance constraints. This synthesis model has been implemented in the prototype system, OASYS, which currently supports the synthesis of CMOS operational amplifiers. Fabricated test chips confirm that OASYS can design real circuits. A set of untuned test circuits, laid out directly from OASYS-synthesized schematics, meets specifications closely (see accompanying table and die photograph). Because synthesis in OASYS is fast, extensive exploration of tradeoffs is feasible. The example design surface, generated in about three minutes on a workstation, illustrates tradeoffs among several parameters and shows where necessary circuit design changes were made automatically. The design knowledge in OASYS iS being broadened to support the synthesis of more complex and nonlinear analog cells to develop styles and algorithms that will generate layouts from schematics, and to develop a knowledge acquisition tool that will permit circuit designers to directly extend and modify embedded synthesis knowledge.



Example 3 μm CMOS Op Amp

Parameter	Spec.	Chip
Gain (dB)	45	48.4
Unity Gain Bandwidth (MHz)	2.8	2.6
Capacitive Loading (pF)	14	14
Slew Rate (V/μS)	2.5	3.0
Power Dissipation (mW)	—	0.56
Area (μm^2)	—	90,450

Professors R.A. Rutenbar and L.R Carley
Carnegie-Mellon University

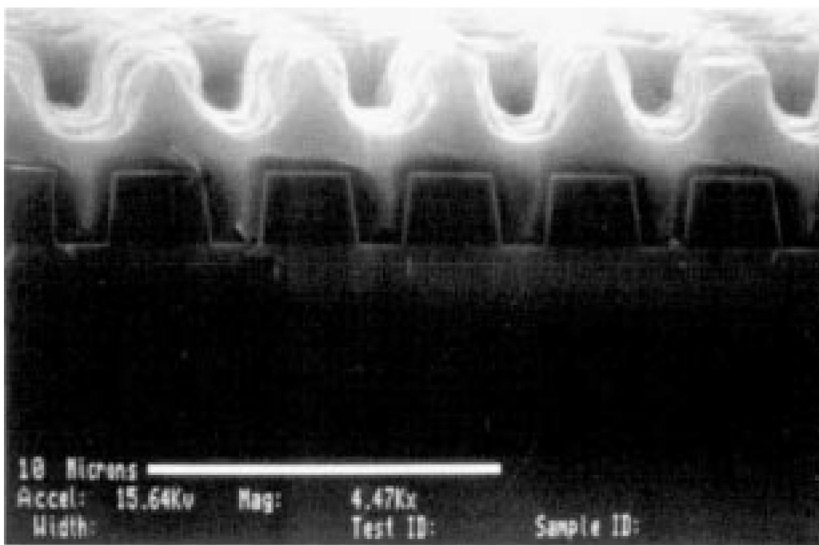
Advanced Process Technology

The next generation IC manufacturing technology will require the use of advanced processes specifically designed for low thermal budget processing with finer geometries and sharper gradients to the dopant distributions. To retain long channel performance for submicron MOSFETs, a recessed gate device design can be employed. To effect a CMOS circuit design with optimum signal to noise, both p- and n- polysilicon will be employed to obtain surface channel devices. Source/drain cladding will be used to reduce surface resistance, and barrier metals will be employed. The understanding of thin film stability and metallurgy with films under high stress will be important. A high density multilevel interconnect technology with low dielectric constant insulation must be developed to support the minimal switching delay achieved with recessed gate submicron channel length FETs. Finally, this must be accomplished with a reliable, low-cost manufacturing approach. SRC research is addressing some of the key issues that must be resolved to achieve the next generation.

Low Cost Silicon Epitaxy

The use of epitaxial silicon layers in ULSI is increasingly attractive, but applications are limited at present by high cost and complexity. Research at UC/Berkeley is exploring the use of a high-capacity, hot-wall, chemical-vapor-deposition system because of the potentially low manufacturing cost for selective silicon epitaxy. A prototype hot-wall system in which the wafers are loaded perpendicular to the gas flow in a "coin-stack" fashion has been constructed by modifying a tube in a commercial LPCVD furnace system. The 9-inch-long flat-zone in the current configuration can potentially accommodate up to 50 wafers with a 100 mm diameter. An epitaxial silicon growth rate of 10 nm/min is achieved with a uniformity across each wafer of ±2%. Spreading resistance profiles show that for a 1.1 µm thick layer grown undoped on an n+ substrate that a "two-order transition-width" of about 0.2 µm with a background concentration of 5 x 10^{14} cm^{-3} is produced. The deposition is perfectly selective, and the growth rate is uniform independent of pattern geometry.

Professor William G. Oldham
University of California at Berkeley



Vias of 2 µm deep and 1 µm widecovered with 2.5 µm PIB Al film.

PIB Metal Deposition

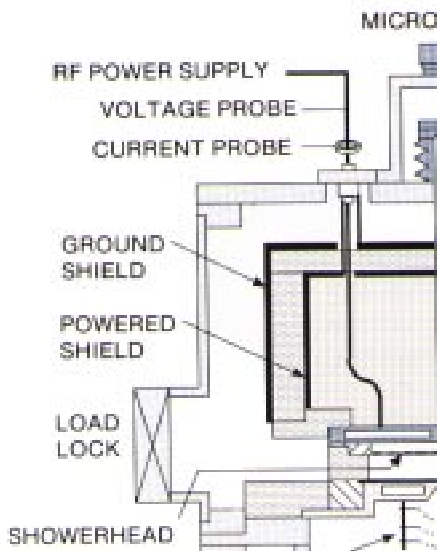
An advanced metal deposition process has been developed at RPI which achieves complete wall-to-wall filling of trenches and vias without developing voids due to overhanging deposition at the uppermost edge of the via. Partial planarization of the metallization is possible in the as-deposited film. Additional processing, e.g., with excimer laser pulsing or continued partially ionized metal beam (PIB) at 300°C substrate temperature, can result in complete planarization of the metal layer. The deposition process employs a PIB with 1-5% self-ions and a bias potential of 1-5 kV applied to the substrate during deposit/on.

Professor Toh-Ming Lu
Rensselaer Polytechnic Institute

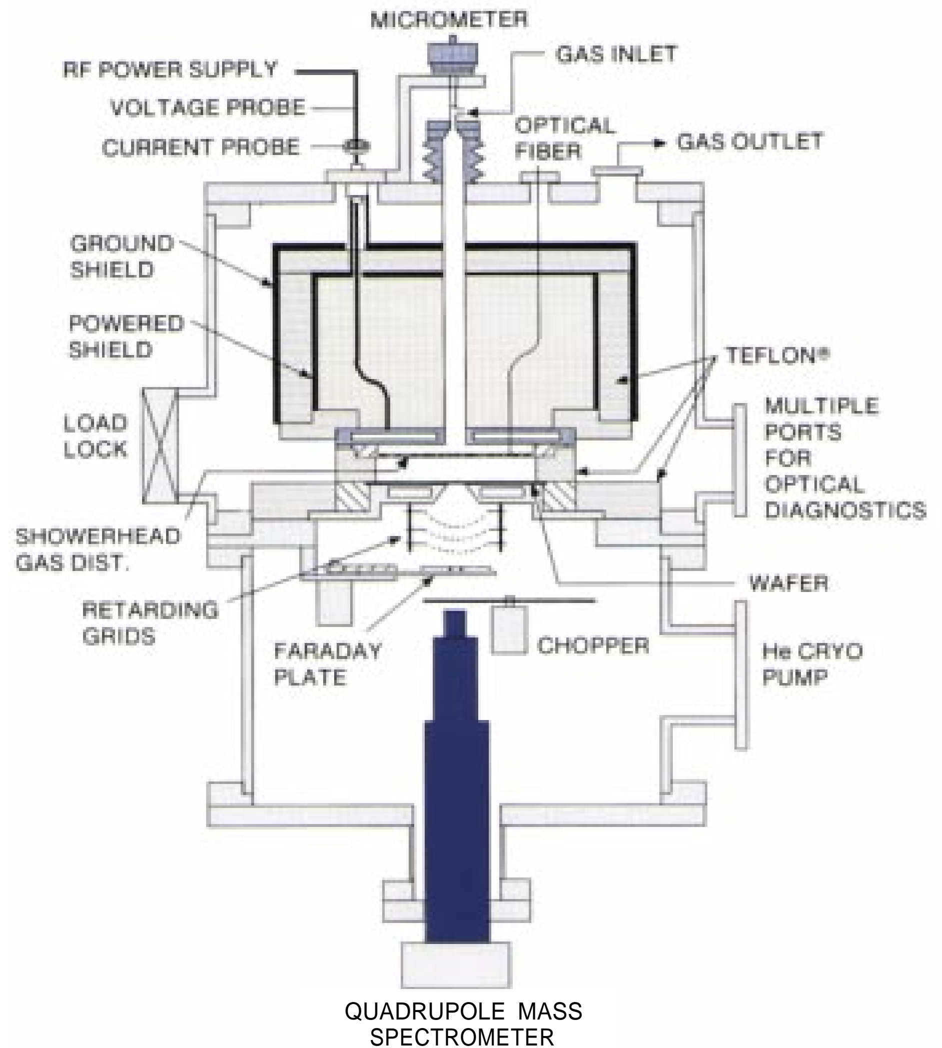
Novel Tungsten Interconnect Technology

A manufacturable, high-performance interconnect technology is key to ULSI integrated circuits. Three of the major aspects required of such a technology are: (1) multilevel — as many as four to ten levels for "system"ICs, (2) vertical level-to-level interconnect without requiring nested vias, and (3) planarization at each level, metal and dielectric. An inherently planar technology has been developed at Cornell that effectively addresses these three issues. Each level of interconnect IS formed by selective deposition of tungsten into oxide channels produced by a highly directional dry etch process. Prior to the tungsten deposition, a high dose silicon implant is employed to modify the oxide surface properties of the floor of the channel so that the deposition of tungsten is initiated only within the channels. A similar process is employed for the filling of vias between metal interconnect planes.

Professor S. Simon Wong
Cornell University



Photomicrograph of a cross section of two levels of planar tungsten interconnect with a contact plug.



Advanced Plasma Etching

A single wafer etcher has been developed at MIT which performs fundamental plasma measurements during directional plasma etching processes. It is anticipated that these measurements, now being used to test and develop kinetic process and equipment models which simulate the glow discharge and chemical kinetics, can be later employed for real-time control of the process. Specific chemical kinetics of chlorofluorocarbon discharges have been modeled and used to successfully predict the etching rate and directionality. Wafer temperature is monitored during etching by a fluoroptic probe and controlled by helium pressurization between the wafer and the electrode. Etch rate is monitored using laser interferometry through an optical fiber; the electrical impedance of the discharge is determined by measuring the current and voltage waveforms to the powered electrode. Spatially and temporally resolved concentration measurements of plasma species are made using both plasma-induced emission and laser-induced fluorescence. During etching, the ion bombardment flux, energy distribution, impingement angle distribution, and composition can be determined by the retarding grid and mass spectrometric analysis of the ion flux which passes through a pinhole in the wafer/electrode surface.

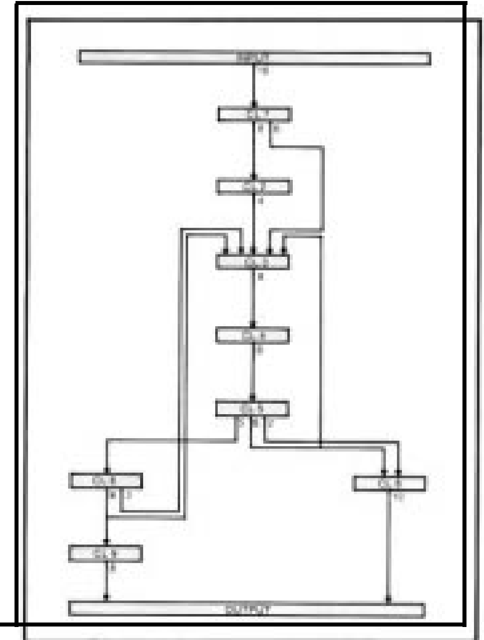
Professor Herbert H. Sawin
Massachusetts Institute of Technology

Design for Test

Significant cost and quality benefits are derived from efficient, high-coverage test of ICs, provided that area penalties are not excessive. The 1994 SRC research goal of a reject ratio due to electrical failure of 1 in 10^6 has mandated that a significant emphasis be placed on testability in the SRC research program. Progress was made in 1987 in automatic test pattern generation, fault simulation, and design for testability.

The hierarchical fault simulator, CHIEFS, developed at the University of Illinois, has been extended to handle bidirectional transistors; and a new program, FOX, has been added to generate a high-level fault description of a module from a low-level (transistor) description. CHIEFS is being tested by application to a large commercial microprocessor. A hierarchical test pattern generator, HITEC, which can handle multiple output blocks and is applicable to sequential circuits, is also under development. HITEC uses the high level circuit structures without flattening them into gate-level primitives. The high level structures can be described in one of three ways: (1) interconnection of lower level structures; (2) Boolean description, e.g., a Boolean equation or truth table; or (3) Functional behavior, e.g., a C program. The Boolean and behavioral descriptions allow the test generation to proceed even before the lower level design of a circuit is complete. This feature should help to identify testability problems early in the design cycle. An early version of HITEC is operational and has been tried on several circuits. The observed performance in these cases has been superior to that of conventional test generation methods which are based on gate-level descriptions.

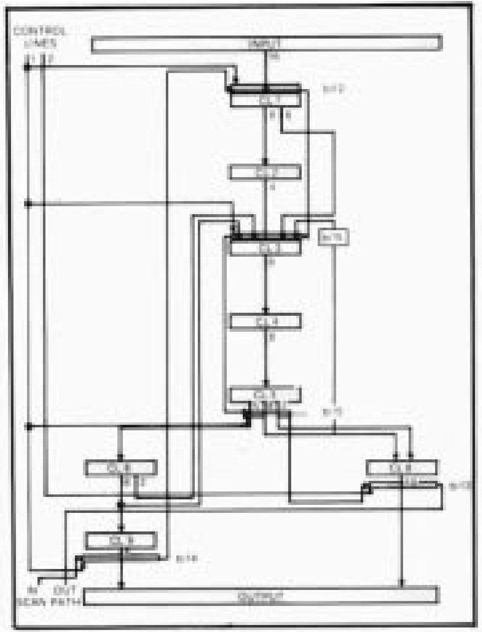
Research is also underway at Carnegie-Mellon University to develop switch-level dual-mode automatic test pattern generation techniques for integrated circuits. In dual mode testing, faulty circuit behavior is detected parametrically by abnormal power supply current levels; and behavioral testing detects abnormal logical values at the circuit outputs. At the board level of design, the expert system single-board computer design system, MICON, has been augmented to produce test information for the designs that it automatically produces. The goal of a research project at the University of California at Berkeley is to improve test generation techniques for sequential digital circuits while reducing the requirement for additional scan logic. The basic idea is to generate tests for a large number of faults for a given circuit, then to determine a minimal subset of memory elements that, if made observable and controllable, will provide easy detection of most remaining non-redundant and difficult-to-detect faults.



First CAST Stage

The Computer-Aided Self-Test System

A three-year research effort at the University of Rochester has produced the CAST (Computer-Aided Self-Test) System: a tool for designing self-testable VLSI chips. CAST is applicable to chip designs that may be represented by data flow diagrams which consist of registers driven by a single two-phase non-overlapping clock, and combinational logic blocks. CAST incorporates a two-stage strategy for transforming applicable designs into self-testable designs. During the first stage, one of two available processes can be used to place BIT (Built-In Test) structures within the chip design. The Built-in Exhaustive Self-Test process uses the Built-in Logic Block Observer technique to provide the design with a functionally exhaustive self-test capability. A lower BIT hardware overhead can be obtained at the expense of test effective-



Second CAST Stage

ness, using the Minimum Overhead Self-Test process that (given an upper limit on the test running time) provides the design with a pseudo-random functional self-test capability. During the second CAST stage, the scan path is designed, the testing procedure is specified, and the minimum required control for the BIT hardware is determined. CAST has been developed using the C programming language and runs on the SUN 3 family of workstations under the SUN UNIX 3.4 operating system. Al/ stages of the design process are displayed using X-windows. A standard Computer Hardware Description Language interface is currently under development.

Professor Alexander Albicki
University of Rochester

Microelectronics Manufacturing Engineering Education

In 1986, the SRC initiated a program for development of interdisciplinary curricula at leading universities so that quality undergraduates and candidates for the Master's degree could gain the wide range of skills needed by today's semiconductor manufacturing engineers. During 1987, the SRC supported a second year of the pilot project at Florida A&M University/ The Florida State University (FAMU/FSU) in Tallahassee, and preparations were completed for expansion of this program to four additional schools by the beginning of 1988.

Faculty from FAMU/FSU aided in program expansion by preparing a Request for Proposals for the development of Microelectronics Manufacturing Engineering Curricula that was sent to twenty of the leading engineering institutions across the United States. Proposals were received from thirteen universities; and the University of Minnesota, Rensselaer Polytechnic Institute, the Rochester Institute of Technology, and the University of Texas at Austin were selected to receive the four new grants.

Multidepartmental teams are being used at each of the five schools to define and develop curricula relative to the needs of the U.S. semiconductor industry. The pilot project's team consulted with industrial and academic personnel, and designed a curriculum questionnaire for distribution to SRC member companies at a workshop and through the mail. The results of this study indicated that the courses considered most essential are Statistics, Semiconductor Physics, Semiconductor Processing, Microelectronics, Materials Science, Packaging, and Computer-Integrated Manufacturing. Courses in Solid State Electronics Devices (Solid State Physics), Microelectronics, and Semiconductor Processing have all been developed and incorporated into the FAMU/FSU curriculum. Additional courses that have been developed and will be added to the curriculum in the coming year are Semiconductor Materials, Fundamentals of Microelectronic Packaging, and Computer-Integrated Manufacturing.

To encourage and facilitate interaction among the participating universities, faculty from each of the five programs have been invited to attend a workshop scheduled for June, 1988, at Research Triangle Park, NC. Each team will be encouraged to share plans and experiences toward stimulating the supply of suitably trained engineers to manage the semiconductor factories of the future.

The TAB and UAC

The Technical Advisory Board (TAB) of the SRC provides essential guidance on goals, priorities, relevance, and strategies for the research program, and coordinates the transfer of research technology to potential users of the results. It consists of technical representatives of members and participants and is organized to correspond to the SRC's program structure.

The University Advisory Committee (UAC) provides insights from the university research community that assist the SRC in management and directing its activities. The committee consists of representatives with backgrounds in semiconductor research from research universities.

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The "APN" is a silicon connection processing node that communicates values in the digital domain and does a nonlinear sum-of-products in the analog domain. On the chip shown above are four nodes, each having four 4-bit "synapses." The chip was fabricated in 3 micron CMOS. *(see research highlight by Professor Hammerstrom. Oregon Graduate Center. on page 23).*

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