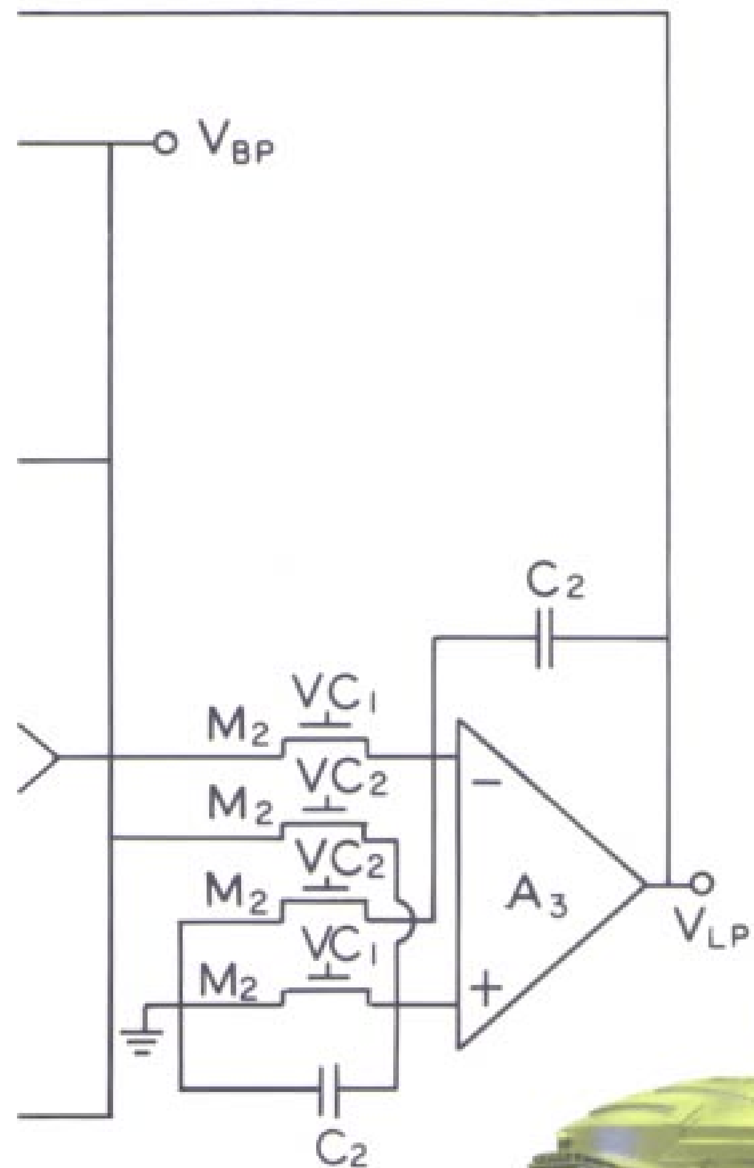
1988 Annual Report



Semiconductor Research Corporation

The Semiconductor Research Corporation (SRC) is a cooperative effort of U.S. companies and government agencies to strengthen and maintain the vitality and competitive ability of the U.S. semiconductor industry.

Its two-fold mission is (1) to identify the scientific and technology needs of the U.S. semiconductor industry and to develop and implement a long-range strategy for meeting these needs; and (2) to enhance the skilled manpower base of the industry.

These goals are realized through an integrated program of basic research conducted by faculty and graduate students at leading U.S. universities. Since 1982, the SRC has committed more than $125 million to this mission and now supports more than one-half of all the silicon-related generic research being carried out at U.S. universities.

SRC research is a “cooperative” effort. The sharing of knowledge, resources, and experience among participants is encouraged through an on-going schedule of SRC activities and events. By creating opportunities for liberal communication among the several thousand persons from industry, government, and academia who contribute to its research effort, the SRC has become a “community” through which many of this country’s best scholars, scientists, and engineers work together to support an industry that is vital to the nation’s security and economic well being.

The model of cooperation provided by the SRC for the efficient use of resources is leading the way within the industry, and between the industry and government, for other cooperative initiatives to strengthen the U.S. technology base.

Executive Message

Robert J. McMillin
Chairman of the Board

Larry W. Sumney
President

1988 was an important year for the Semiconductor Research Corporation. Our industry-sponsored program of cooperative research posted a number of accomplishments which add strength to U.S. efforts to maintain our world leadership position in microelectronics.

Research expenditures were $19.5 million, an increase of $3 million over 1987 and the highest in SRC's brief history. Funds from SEMATECH, the industry's cooperative effort in manufacturing technology, augmented the support flowing to U.S. universities through the SRC. With SEMATECH's increased contribution in 1989, we anticipate a combined research program approaching $30 million.

In 1988, the SRC Research Program produced 22 invention disclosures, 12 new patent applications, and one patent. More than 850 new research reports and papers were generated for distribution to member companies.

Two new SRC Centers of Excellence were designated in 1988: at the University of Michigan at Ann Arbor for semiconductor manufacturing automation and at Stanford University for semiconductor manufacturing systems. And designation of nine SEMATECH Centers of Excellence, focusing on areas of special interest in the semiconductor manufacturing technologies, significantly expanded SRC research.

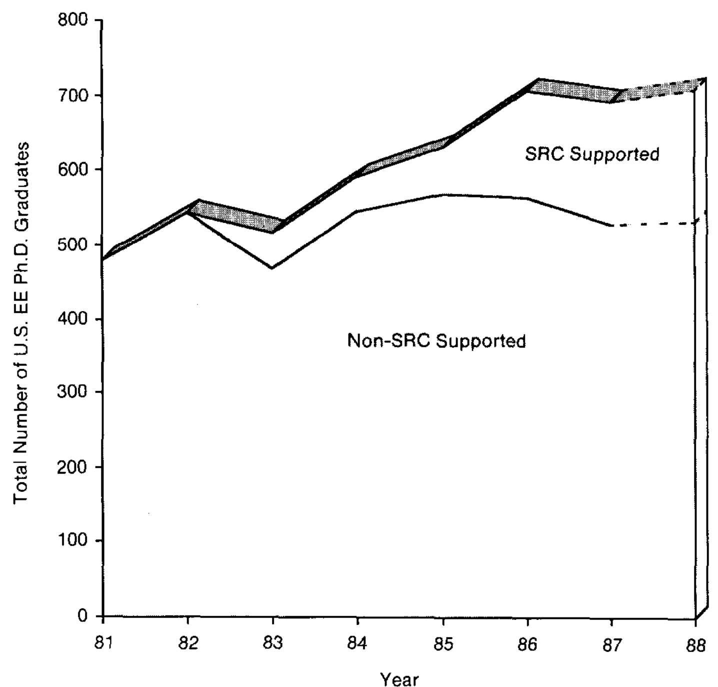
The photo above was taken at the Massachusetts Microelectronics Center during the kickoff meeting for the SEMATECH Center of Excellence that will conduct studies on single-wafer processing for flexible integrated circuit manufacturing.

To demonstrate the research program's scope and depth, the SRC held its first general technical conference, TECHCON '88, in October. The three-day event drew over 650 enthusiastic participants from industry, government, and the university community, including many of the graduate students performing research under SRC contracts. Designed to promote a free exchange of technology, its success was a tribute to the strong support of the semiconductor industry for cooperative research. Described as "stimulating, motivating, and enlightening" by attendees, TECHCON '88 was so well received that plans are underway for a second general technical conference in 1990.

Another dimension was added in 1988 to the industry's cooperative efforts with the creation of the SRC Competitiveness Foundation. It's initial focus will be on educating a capable work force to provide leadership for a competitive national technology base. The foundation is a focal point for new funding sources interested in and supportive of the industry's efforts to increase its supply of trained scientists and engineers. Among the activities to receive Foundation support is the highly successful SRC Graduate Fellowship Program, which is currently supporting more than 30 students. Potential new programs include endorsing interactive pilot projects to acquaint secondary school teachers and students with actual research settings, promoting student career orientation in science and technology, developing technical curricula at all educational levels, establishing scholarships for master's degree candidates, and offering awards to university faculty for distinguished teaching and research.

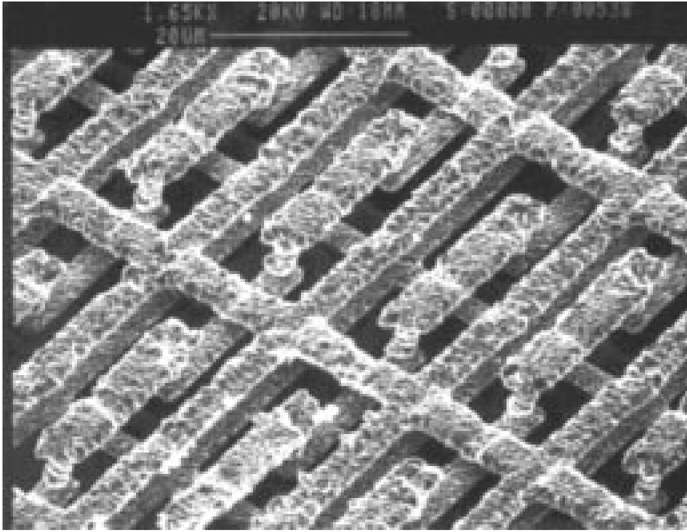
The SRC concept of a National Advisory Committee on Semiconductors, introduced in the U.S. House of Representatives by Rep. Tim Valentine, D-NC, was enacted by the Congress in 1988. NACS is a blue-ribbon, industry-government panel that will explore the technological, financial, and political issues affecting the health of the industry and its continued leadership in semiconductor technology. Committee members, appointed by the President, include the chairman, Ian Ross,

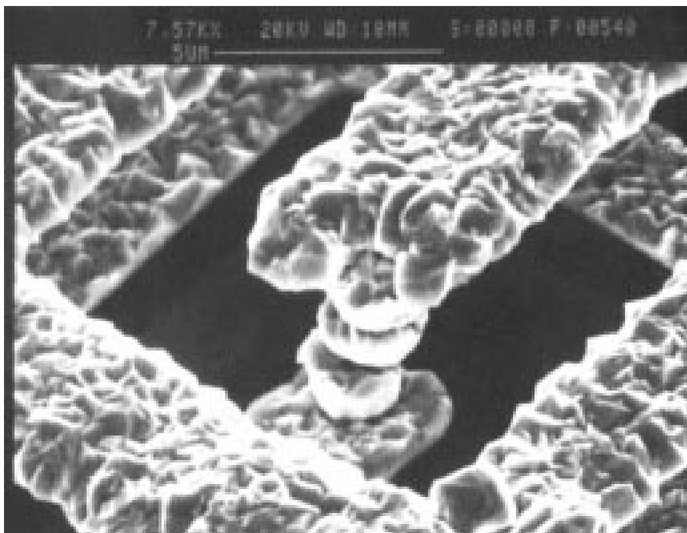
Ninety-five poster sessions at TECHCON '88 proved to be an exceptional technology transfer opportunity between industry/ government representatives and the students researching new technologies.



The SRC's contribution to the U.S. technology manpower base continues to increase.

Executive Message





An inherently planar multilevel metallization technology, which also provides vertical level-to-level connections, has been demonstrated. The technology is based on selective deposition of tungsten into oxide channels and holes to form interconnects and contact plugs, respectively. The upper photograph shows contact chains between first and third levels of interconnect. Oxide has been removed to reveal the structural detail of the vertical connection. Zoom view shows that the contact stack is composed of contact plugs from first-to-second level and second-to-third level, as well as second-level metal shaped like a contact plug. — from research led by Professor S. Simon Wong, Stanford University.

president of AT&T Bell Laboratories, and seven other industry and five high-level federal government representatives.

A review of the goals set by the founders shows the SRC accomplishing everything it was designed to accomplish — and much more.

The SRC was established in 1982 to restore the generic research base relating to silicon integrated circuits. Today, a large, productive research capability in U.S. universities is directed to this technology. We can take great pride in the success of our research program. In each of its three science areas — microstructure, design, and manufacturing — the SRC has had a very positive effect on the technology base. It has strengthened existing university research programs and created new ones. It has introduced new vital research subjects and won their acceptance. One-half dozen years ago, virtually no university research was being conducted in electronic packaging, in integrated circuit reliability, or in semiconductor manufacturing systems. Now, significant, relevant research efforts are under way. The impact is enormous.

The SRC also was directed by its founders to increase the skilled manpower base of the semiconductor industry. Again, it clearly is very successful. Prior to 1982, U.S. universities were conferring fewer than 500 Ph.D.s in electrical and electronic engineering each year, and less than 15 of these focused on silicon integrated circuits. In 1988, the total number of Ph.D.s conferred was close to 700, and more than 175 of the recipients had silicon-related research experience under SRC contracts. This year, our research program supported over 450 graduate students; and of the 224 who completed their graduate education, well over one-half now work for our member companies.

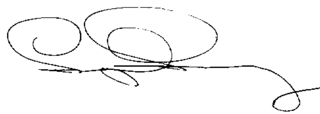
In the broad area of cooperation, the SRC also has had a major impact. The government's attitude toward cooperation with the industry to develop the technology needed to maintain a strong domestic economy has undergone major changes in the last several years. And many persons within the industry believe that, without the SRC, SEMATECH would

not now be a reality. The SRC has provided the strategy and played a vital role in making these things happen.

In spite of these successes, however, the problems that led to the founding of the SRC are far from solved. The US. share of semiconductor markets is continuing to decrease. In technology, the U.S. remains behind in many areas. The competition continues to get stronger. Generic research can be expanded and improved in many ways to better serve the industry and the country. And, in many ways, the SRC, because of the experience and creative talent of its participants, can continue to provide effective leadership and support for innovative activities such as SEMATECH and NACS. Our membership should encourage this.

The SRC is the member companies, the government agencies, the universities, and all the people who participate in the SRC Research Program — working together to seek solutions to some very complex problems. Each participant deserves to regard the SRC's success as a personal success. We look forward to increased opportunities for cooperative activities in the years ahead.

Robert J. McMillin
Chairman



Larry W. Sumney
President

The TECHCON '88 theme, "Cooperation in the Semiconductor Industry," was reflected not only in the overall tone of the conference but also in the numerous hallway gatherings and informal discussions taking place throughout the 3-day event.

Participants

Companies

AT&T
Advanced Micro Devices, Incorporated
Applied Materials, Incorporated
Control Data Corporation
Digital Equipment Corporation
E.I. du Pont de Nemours &Company
E-Systems, Incorporated
Eastman Kodak Company
Eaton Corporation
GTE Laboratories, Incorporated
General Electric Company
General Motors Corporation
Harris Corporation
Hewlett-Packard Company
Honeywell Incorporated
IBM Corporation
Intel Corporation
Micron Technology, Incorporated
Monsanto Company
Motorola, Incorporated
NCR Corporation
National Semiconductor Corporation
The Perkin-Elmer Corporation
Rockwell International Corporation
SEMATECH, Incorporated*
Silicon Systems, Incorporated
Texas Instruments Incorporated
Union Carbide Corporation
Varian Associates, Incorporated
Westinghouse Electric Corporation
Xerox Corporation

*Associate Member

L to R: SRC Board of Directors member Bob Jenkins from Motorola, SRC President Larry W. Sumney, and SIA President Andrew A. Procassini during ceremonies at TECHCON '88 honoring the SRC's eleven founding member companies.

Government

Air Force Wright Aeronautical Laboratories/ Electronic Technology Laboratory
Defense Nuclear Agency
National Institute for Standards and Technology
National Science Foundation
National Security Agency
Office of the Undersecretary of Defense/ Computer and Electronic Technology

Institutions

Arizona, University of
Auburn University
Brown University
California at Berkeley, University of
California at Irvine, University of
California at Los Angeles, University of
California at Santa Barbara, University of
California Institute of Technology
Carnegie-Mellon University
Case Western Reserve University
Clemson University
Columbia University
Cornell University
David Sarnoff Research Center
Duke University
Florida, University of
Florida State University
Georgia Institute of Technology
Illinois at Urbana/Champaign, University of
Lehigh University
Maryland, University of
Massachusetts at Amherst, University of
Massachusetts Institute of Technology
Massachusetts Microelectronics Center
Michigan, University of
Microelectronics Center of North Carolina
Minnesota, University of
Nebraska at Lincoln, University of
New Mexico, University of
North Carolina at Chapel Hill, University of
North Carolina at Charlotte, University of
North Carolina State University
Ohio State University
Oregon Graduate Center
Purdue University
Rensselaer Polytechnic Institute
Research Triangle Institute
Rochester, University of
Rochester Institute of Technology
South Florida, University of
Southern California, University of
Stanford University
Texas at Austin, University of
The Texas A&M University
Wisconsin, University of
Yale University

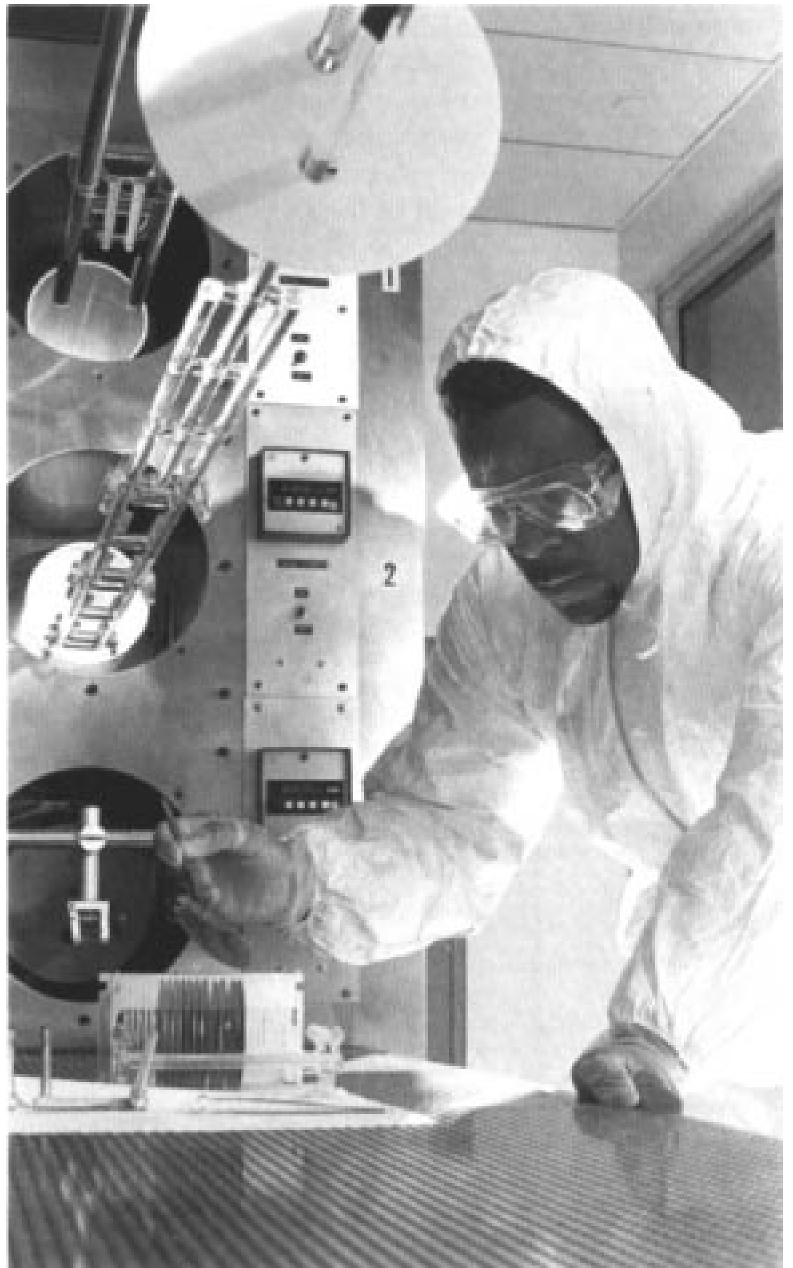


Photo Courtesy of the Rochester Institute of Technology

Research: Overview

Cooperative research, in general, and the SRC's program, in particular, require that the participants must share in ownership of this cooperative effort and its goals and products. To create this mutuality of interests, the SRC has a Board of Directors, Technical Advisory Board, University Advisory Committee, technical meetings, program reviews, and other venues for interaction among industry/ government representatives and the students and faculty carrying out the research. Through these interactions, the views of SRC program participants are merged into policy, goals, and a research program that reflects the encompassing objective of enhancing the competitive strength of the U.S. semiconductor industry. The SRC's success to date and its future successes are dependent upon the quality of interactions.

Universities, the SRC, and Cooperative Research

Dean Gibbons

When discussing the strategy of the SRC's cooperative research mission during an address at TECHCON '88, Dr. James F. Gibbons, Dean of the School of Engineering at Stanford University, included the following observations.

"...SRC has developed a broad strategy for supporting university research programs that is consistent with university research guidelines and, at the same time, supportive of the long-range needs of the industry. In particular, SRC offers university researchers hands-on guidance but stops we//short of hands-on interference.

"...because of the structure of our industry, together with the fact that most basic research is done in universities in this country, we need to plan for and secure effective university/ industry interaction to remain competitive...SRC has been an effective agent in promoting this cooperation on behalf of the semiconductor industry."

Research Goals

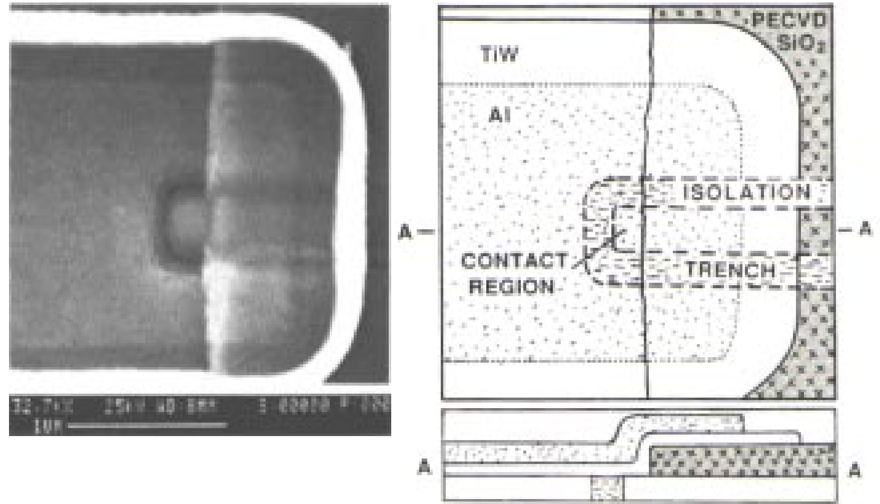
Current research is related to the set of long-range industry goals which was identified in the SRC's early years, 1982-1984. These goals, which reflect the industry's needs for improved performance and higher density integrated circuits, are to make possible by 1994 the prototype production of chips with:

- complexity 250 times greater than those of 1984 (equivalent to a 256 Mbit DRAM),
- functional throughput rates of 5 x 10^{15} gate-hertz per square centimeter,
- reliability such that less than 10 failures occur in 1 billion operating hours,
- cost per functional element reduced by 500 times from 1984 costs.

In 1988, a major planning process was begun to identify new technology goals for the year 2001. These goals are being addressed using a top-down approach in which future chip applications will be used to define their performance requirements and technology capabilities. All segments of the SRC community are involved in this goal-setting process, and the 2001 goals will be used to reformulate the structure and priorities of the SRC Research Program in 1990 and beyond.

Research goals define the interest areas of the SRC. Translation of these into the almost 300 tasks that comprise the research program required judgment by the management and advisors of the SRC, since research is inherently unpredictable. Cooperation requires a balance in the research agenda reflecting the diverse objectives of its participants, while high quality research requires assumption of the risks associated with exploring uncharted technologies. The result is research that ranges from expanding current technology capabilities to exploring fundamental new approaches that will be applicable decades in the future.

A top view SEM of a contact region of a source-drain resistance measurement test structure. The oxide filled isolation trenches are 0.3 μm wide and 0.5 μm deep. The contact region shown is arsenic implanted and covered with 60 nm of $TiSi_2$. Its dimensions are 0.2 μm x 0.3 μm. This structure was fabricated by Asanga Perera, member of a research group led by Professor J. P. Krusius of Cornell University.



In its research program planning, the SRC must continue to recall the reasons that led to its inception in 1981. Government support of semiconductor research had become focused on niche technologies with the expectation that industry would provide for the advancement of the mainstream silicon integrated circuit technology. At the same time, the industry, with its market share being challenged by advantaged foreign competitors, was forced to focus its efforts on short-range objectives. Support of generic research for silicon devices had almost vanished. The SRC was created to reverse this trend, and it has succeeded in this mission. It cannot, however, address important issues that diverge from this seminal purpose without defining the additional mission and providing the needed resources. One of the strengths of the SRC is its focus — a well-defined mission with the appropriate resouces to accomplish it.

Centers of Excellence

The University of Michigan at Ann Arbor and Stanford University in California were named Centers of Excellence for the SRC Research Program in 1988. The Michigan Center focuses on semiconductor manufacturing automation and the Center at Stanford focuses on semiconductor manufacturing systems.

The Center of Excellence designation, made by the SRC Board of Directors, recognizes a university's outstanding semiconductor research capabilities. An SRC Center receives over $1 million annually from the SRC for its research program. Other SRC Centers of Excellence are Carnegie-Mellon University for computer-aided design, Cornell University for microscience and technology, and the University of California at Berkeley for computer-aided design.

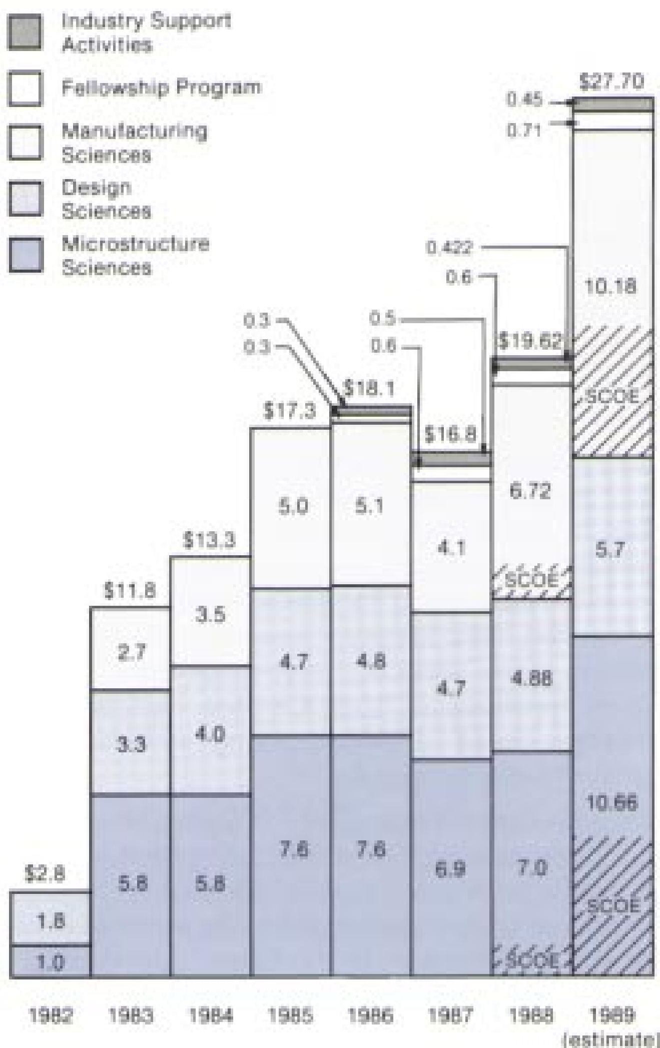
In 1988, the SRC began directing university research funded by SEMATECH, the semiconductor manufacturing technology consortium. Approximately $10 million has been committed to nine Centers of Excellence. Selection of the SEMATECH-funded Centers was based on the quality of the research programs offered, their relevance to the SEMATECH program, and the nature of the available program resources.

These Centers are designated by state and will conduct studies in the following areas: Arizona - contamination/defect assessment and control, California - lithography and pattern transfer, Massachusetts - single-wafer processing for flexible integrated circuit manufacturing, New Jersey - advanced plasma etch processing, New Mexico - metrology, New York - multilevel metallization, North Carolina - single-wafer processing, Texas - manufacturing systems, and Wisconsin - X-ray lithography.

Located in Austin, Texas, SEMATECH is a consortium of 14 U.S. semiconductor manufacturing firms. All of its members are members of the SRC. One-half of its $200 million annual budget is provided by its member companies and the remainder by the federal government.

Research: Overview

Research Program Commitments
($ in Millions)



The SRC Research Program

In 1988, over 450 graduate students were participating in research supported by the SRC that addresses defined industry research needs. The number of students will be larger in 1989. It is the largest cooperative university research program that has ever existed. The quality of this research is confirmed by its strong presence in peer-reviewed publications and at the best technical meetings, its ability to attract participation of outstanding faculty and graduate students, and by the large number of researchers submitting unsolicited research proposals to the SRC.

Silicon semiconductor devices are recognized as one of the key areas of international high technology competition and of great importance to the future economic and defense posture of the U.S. This has elevated the importance of SRC's research and places even greater emphasis on its quality and productivity.

Even though SEMATECH's contribution has increased total SRC research funding from circa $18 million/year to almost $27 million/year, the amount that would be required to support the number of scientists and engineers who would like to participate in the SRC program far exceeds budgetary limitations. This provides the SRC with the ability to maintain high quality, relevance, and productivity by selecting only those research projects with the greatest potential, but it also means that many researchers who might make valuable contributions are not given the opportunity. In particular, the SRC's program is focused most strongly in electrical engineering and inadequate participation from other disciplines with highly relevant capabilities.

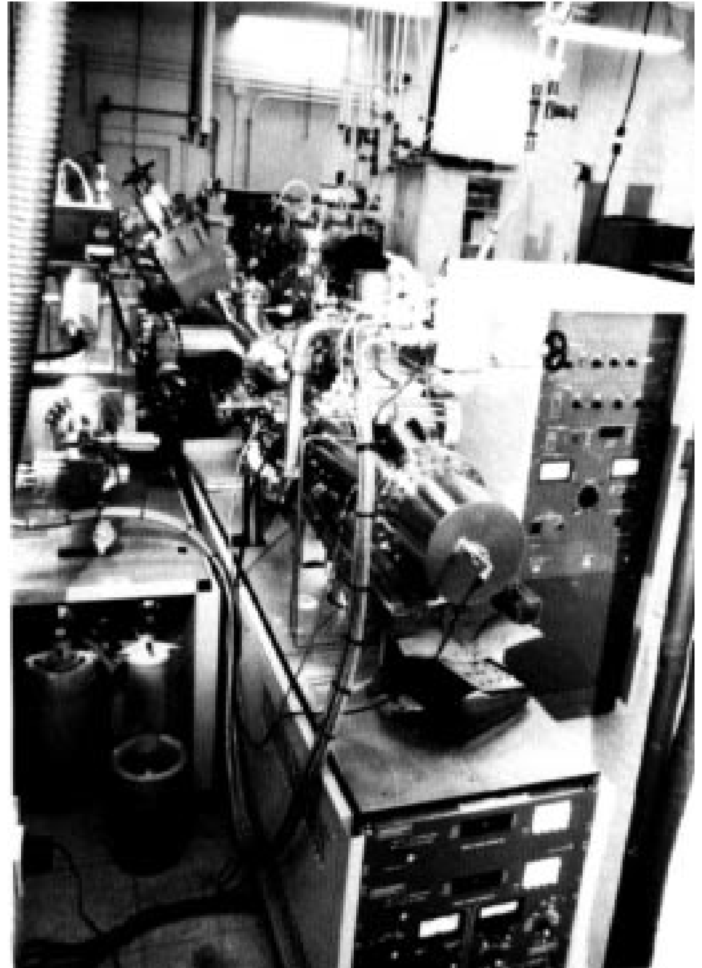
The SEMATECH Center-of-Excellence program has skewed financial resources in the three science areas of the SRC The estimated research budgets for 1989, including SEMATECH funds, in the three areas are as shown in the accompanying graph (Design Sciences, $5.7 million; Microstructure Sciences, $10.7 million; Manufacturing Sciences, $10.2 million).

Manufacturing Sciences Research

Manufacturing Sciences technology transfer highlights in 1988 included the introduction of two new semiconductor equipment products. One is a new optical microscope coming from the confocal optical microscopy research carried out at Stanford University and the second is a new particle detector/counter developed for clean room use evolving from studies at the Research Triangle Institute and the Microelectronics Center of North Carolina. Manufacturing Sciences sponsored more than 30 modeling and software projects, and results from this work include more than 200 beta-site tests of factory simulators, factory management software, and packaging CAD software.

Design Sciences Research

In 1988, Design Sciences research was very productive both in terms of quantity and quality of results and in the breadth of activities of the SRC design community. Three Technology Transfer Courses were conducted; three workshops were held in the areas of Sea-of-Gates Technology, Analog Design Automation, and Design for Manufacturing; and a new software directory containing 95 entries was released. The two SRC Centers of Excellence in IC CAD at the University of California at Berkeley and at Carnegie-Mellon University, together with the programs at the University of Illinois at Urbana-Champaign and the University of Southern California, have provided sustaining leading-edge contributions to the SRC Design Sciences program over a wide range of research. Significant results have been achieved in a number of individual projects on other campuses, and a new program in Design-for-Test at the University of Texas is expected to make substantial progress in the year ahead.



Integrated Si-based MBE equipment for quantum-based device research at UCLA.

Microstructure Sciences Research

Research programs in Microstructure Sciences reached the $10.7 million level in 1988. Process technology accounts for 45% of the total, with one-half of this being conducted at the New York and New Jersey SEMATECH Centers of Excellence. Principal activities are being undertaken in interconnect metallurgy for multilevel interconnect systems, plasma etching, and one-quarter micron materials technology. Process engineering is chiefly concerned with equipment modeling, process integration, and thermal process modeling and includes principal activities at MIT, Texas, and Stanford. Device technology programs are addressing BiCMOS, bipolar, and quantum devices, with main efforts at Cornell, Florida, and UCLA. Specific instances of technology transfer during 1988 came from the ROXNOX project at MIT, the radiation hardness and hot-electron effects results from Yale, the epitaxial layer overgrowth techniques from Purdue, and understanding of the electron trap generated in doped oxides from RPI.

The highlights of SRC projects given on the following pages are representative of the diversity, quality, and relevance of the research being performed.

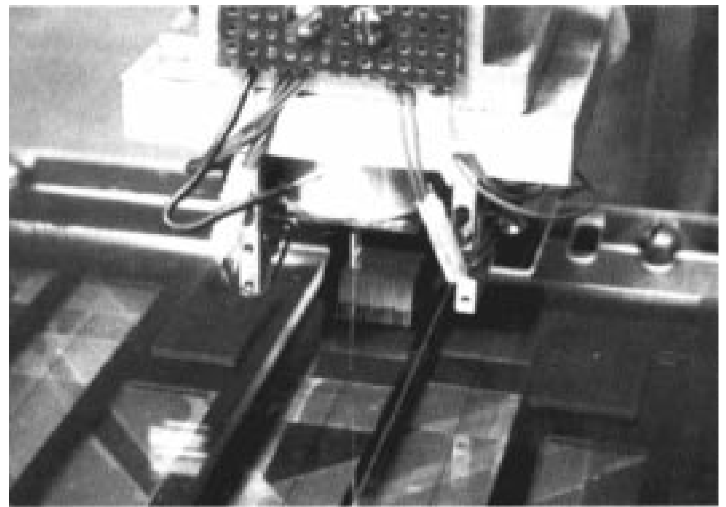
During 1988, the maturing of manufacturing science as an academic discipline was recognized by the designation of the SRC research commitments at Stanford University and the University of Michigan as Centers of Excellence in the area of Computer Integrated Manufacturing for Integrated Circuits (CIM-IC). The research programs at each of these centers cover a broad range — from devising specification languages for describing the many aspects of the manufacturing process to designing storage and communication systems for the massive quantities of data associated with IC manufacturing, to designing novel process equipment and equipment control methodologies. Similarly broad programs at Carnegie-Mellon University and the University of California at Berkeley are partially supported by the SRC.

Related software research is being sponsored at Carnegie-Mellon University, and an experimental study in magnetically controlled micro-robots is being carried out at the University of Texas at Austin.

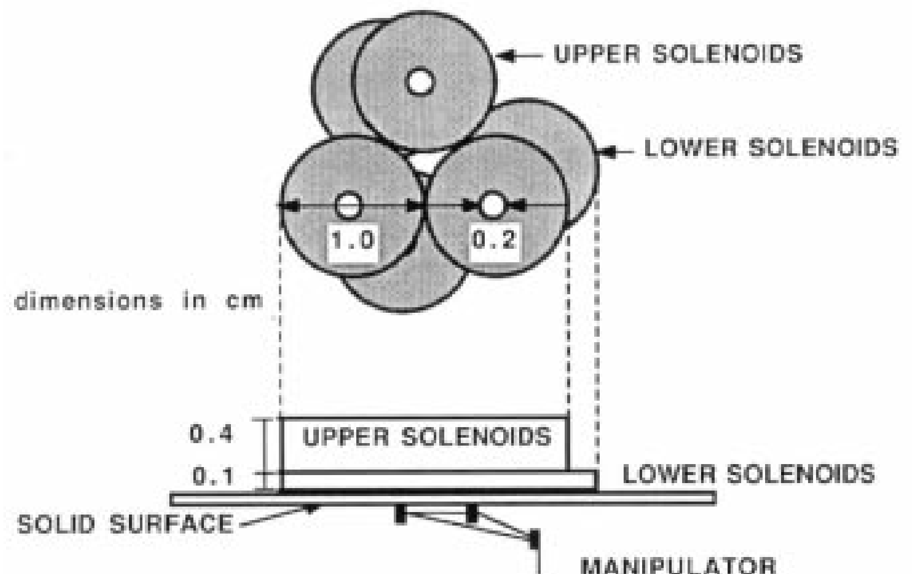
Magnetically Levitated Micromachines

The automation of manufacturing processes in semiconductor device fabrication poses a serious challenge to current technology because of the need for cleanliness, high speed, high precision, and large workspaces. An effort is underway to meet this challenge using magnetically levitated micromachines. Work to date has focused on a triangular-shaped, rigid manipulator that is driven by a set of six air-core electromagnets. The manipulator has rare earth passive magnets in each of the three vertices and weighs 0.5 gram. This system has shown an ability to perform up to 136 fifteen-micrometer random direction moves per second with 0.5 μm accuracy. It also may be used to mechanically or electrically probe a three-dimensional structure. In the second phase of this research, magnetically levitated micromachines will be used to address three specific problems: transport (various scales), analytical probing, and nondestructive TAB bond testing.

Professor Ilene Busch-Vishniac
University of Texas at Austin

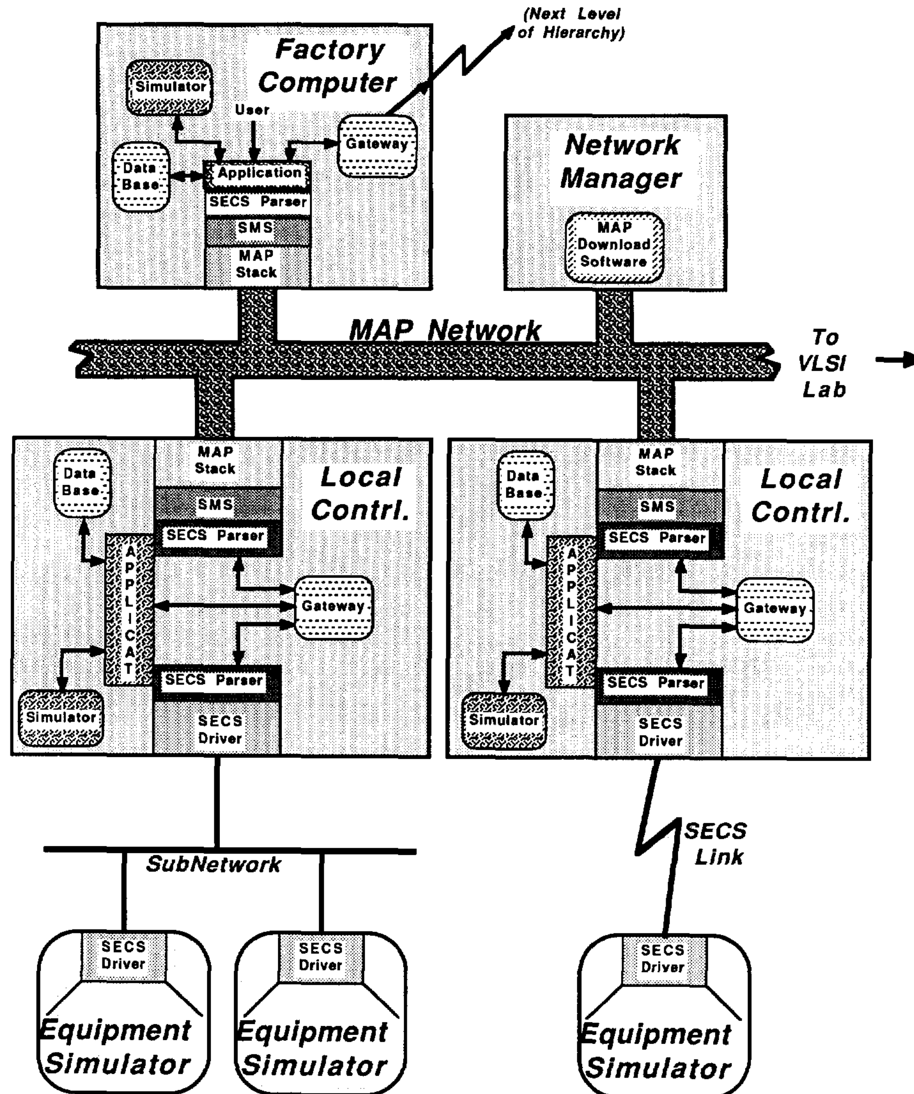


Micromachine electrically probing a substrate. The substrate has several thin lines which the micromanipulator tracks. The solenoids driving the machine are fixed on the arm of a robot which moves during the tracking operation.



System Geometry

FACILITY AUTOMATION CONCEPT MODEL



Factory Automation

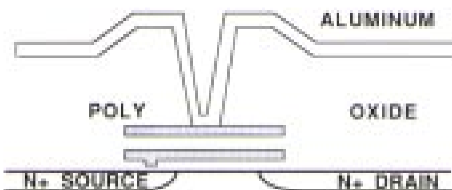
A data communications system, based on the commercially available MAP system and the SECS standards, has been developed. This multilevel hierarchy is illustrated in the accompanying diagram, showing how the local controllers for each piece of processing equipment interface with the overall factory system on the one hand and with equipment simulators on the other. A MAP network has been installed in the Fabrication Facility that allows broadband communication with a guaranteed response time. This network has been characterized for message lengths from 1 to 1000 bytes with maximum effective data rate of about 350 Kbits/sec. To interface the network to equipment configured for the SECS protocol, a SECS Message Service (SMS) has been created. SMS incorporates the desirable features of the SECS protocol into an Open Systems Interconnection application layer environment, achieving the advantages of both environments — including higher speed, flexibility, and a well-defined interface. This development has been the result of cooperation with personnel from SEMI and from industry.

Professor Leo C. McAfee, Jr.
University of Michigan

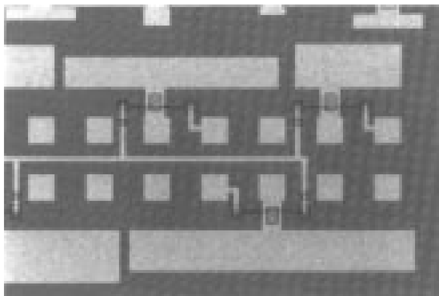
Wafer Surface Charge Monitor

Charge build-up on the surface of the wafer is a potentially important processing parameter, particularly in plasma and ion implant steps. A special test circuit has been designed and demonstrated to measure this parameter *in situ,* as a part of the testing and diagnostics task within the Stanford Center of Excellence program. The structure is essentially that of a floating gate, electrically alterable MOS PROM cell whose control gate is connected to a metal charge collection plate. If sufficient charge is collected on this plate during the process being evaluated, the resulting potential will charge the floating gate and cause a shift in the gate threshold voltage of the MOS transistor, which can be measured at the conclusion of the process. The collection plates can have different areas to vary the charge sensitivity of the monitors as shown in the photo.

Professor Wieslaw A. Lukaszek
Stanford University



Cross section of the monitor device, showing double-poly PROM cell with collection plate.



Micrograph of part of the completed die, showing individual 3-terminal EEPROM cells with collection plates of varying sizes.

The Integration of Equipment and Process Models

Equipment Settings
- temperature
- gas flows
- pressure

Processing Environment
- temperature distribution
- partial pressures of reactants

Change in Wafer State
- physical
- electrical

Equipment Model

Process Model

Accurate equipment and process models can provide a modern semiconductor processing facility with the means for extensive automated process control. Equipment models predict the wafer processing environment from actual equipment settings. The physical and electrical changes to the wafer can then be predicted using existing process models.

Nonlinear Response Surface Methods

Physically-Based Analytical Process Model

PHENOM

Physically-Based Equipment Model Using Nonlinear Multi-Layered Regression

A software tool, PHENOM, builds customized physically based equipment models by combining conventional nonlinear response surface methods with established process models. The resulting hybrid model provides robust equipment control and diagnostic capabilities.

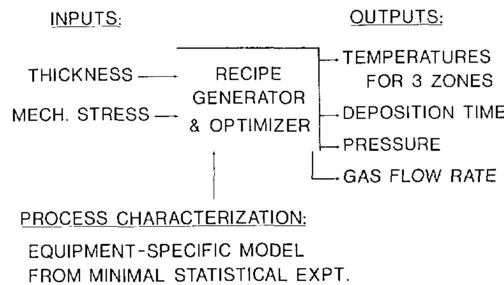
Professor A.J. Strojwas
Carnegie-Mellon University

Process Recipe Generation

Research in Berkeley's EECS Department is primarily oriented towards developing computer applications in support of IC processing. The program includes the development of a model for the low-pressure chemical vapor deposition (LPCVD) of polysilicon. The model is designed to generate the process/equipment parameters required to produce polysilicon films with the desired thickness and mechanical stress. The LPCVD process is initially characterized with a minimum set of depositions carried out under statistically designed sets of conditions, and the results are used to adjust the model for the particular process, The model can then be used to select the deposition parameters for desired film characteristics. The LPCVD equipment is shown in the photo.

Professor David A. Hodges
University of California at Berkeley

RECIPE GENERATOR FOR LPCVD POLYSILICON

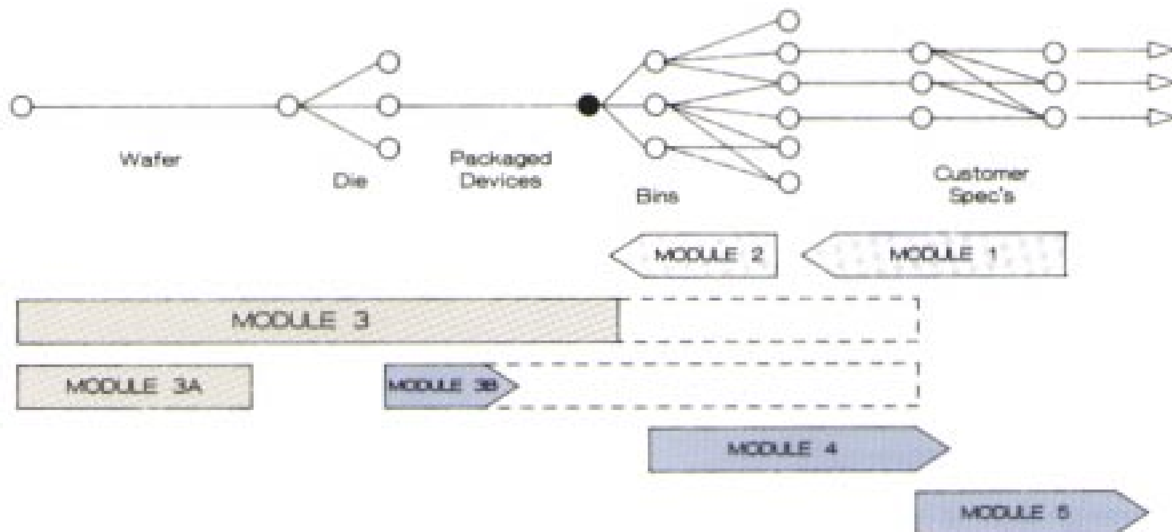


Experimental LPCVD System

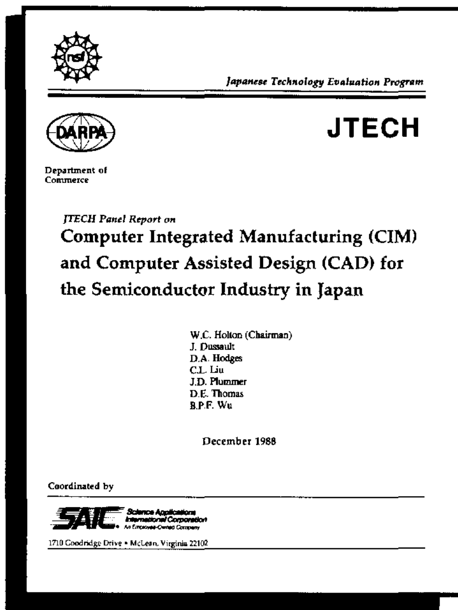
Factory-Level Business Planning

SRC-sponsored work at the Berkeley Operations Research Center is focused primarily on the factory-level business planning for semiconductor manufacturing. The overall framework of the Corporate Planning System project is illustrated below, showing the way in which various software modules being developed map onto the manufacturing wafer flow — from the bare silicon wafer to the customers with their often unique requirements. The arrow ends of the module blocks indicate where the modules are "forward planning" (assuming a given material supply and optimizing the use of the downstream capacities to meet the desired demands), "backward planning" (taking the downstream demand and optimizing the upstream inputs to best meet these demands), or "complete planning" (allowing the input and demands to vary to optimize the use of the capacities). All of the modules but one are operational, and several are available in both VMS and Unix versions.

Professor Robert C. Leachman
University of California at Berkeley



Corporate Planning System


Japanese Technology Evaluation Program

JTECH

Department of Commerce

JTECH Panel Report on

Computer Integrated Manufacturing (CIM) and Computer Assisted Design (CAD) for the Semiconductor Industry in Japan

W.C. Holton (Chairman)
J. Dussault
D.A. Hodges
C.L. Liu
J.D. Plummer
D.E. Thomas
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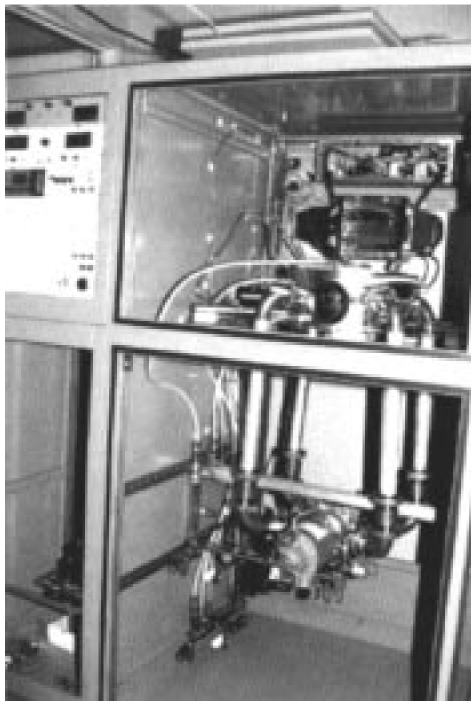
1710 Goodridge Drive • McLean, Virginia 22102

JTECH Panel Report

Visibility of significant integrated circuit activities in Japan and Europe is maintained by the SRC through participation of the SRC staff and its contractors in study groups and visits abroad to evaluate technological advances and developments. In 1988 Dr. WC. Holton served as panel chairman for the National Science Foundation's Japanese Technology Evaluation Program on "Computer Integrated Manufacturing (CIM) and Computer Assisted Design (CAD) for the Semiconductor Industry in Japan," fields which are key to the continuing growth of the semiconductor industry.

The report examines the U.S. competitive position in CIM &CAD through a study of the quality and direction of Japanese R&D and factory implementation of the resulting technology. Briefly, the study concludes that although the U.S. has maintained a favorable position in CAD, the Japanese semiconductor industry has developed a commanding five-year lead in CIM.



A single-wafer multiprocessing reactor for in-situ growth and deposition of dielectrics, semiconductors, and metals by combining lamp heating, remote microwave plasma stream, and photonic processing in a cold-wall chamber.

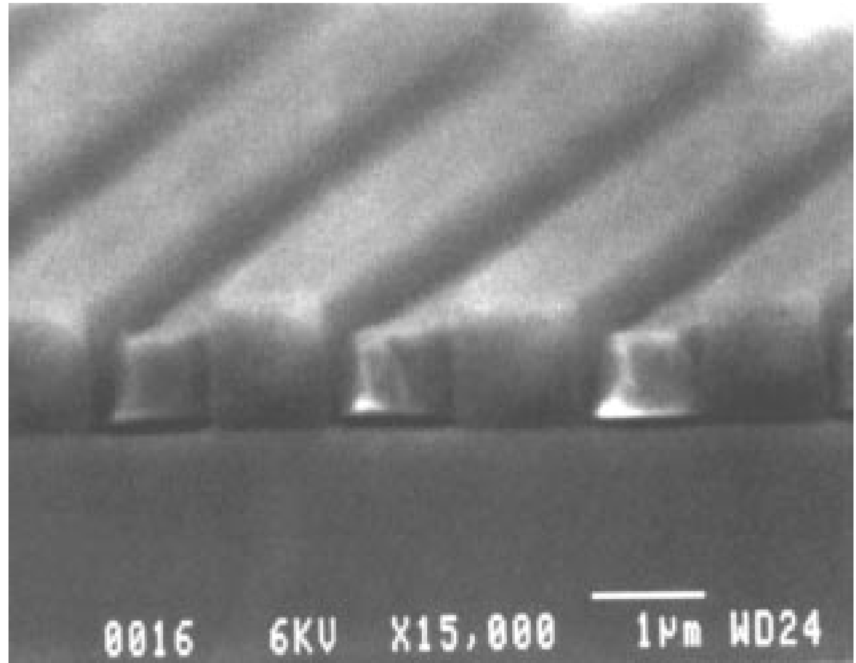
Rapid Thermal Multiprocessor

A new class of equipment is being developed for single-wafer *in-situ* multiprocessing. The motivation for this line of research is the expectation that VLSI manufacturing of the future will use larger wafer diameters, require lower defect densities, and demand substantially greater process flexibility than can be readily achieved with current equipment. The computer-controlled, multiprocessing class of equipment has the potential for significant improvements in each of these areas, by processing one wafer at a time through several sequential process steps, thereby reducing handling and exposure to the ambient. A prototype reactor has been constructed that combines thermal, plasma, photo, and low-pressure processing with *in-situ* monitoring and extensive computer control (see accompanying photo). The goal is to achieve sufficient process flexibility to tailor the processing of each wafer to satisfy the requirements of individual circuits and/or customers.

Professor Krishna C. Saraswat
Stanford University

Lithography research is the leading edge of next-generation manufacturing technology required for megadevice fabrication. Deep ultraviolet lithography (DUV), planned for use in manufacturing megadevice ICs in the 1990s, will require new stepper technology and new photoresists. Beyond DUV, X-ray lithography is being evaluated for use in manufacturing multimegadevice ICs well into the 21st Century. The photoresist research at UNC/Charlotte, described below, illustrates how photoresist polymers can be modified to improve the performance of the photoresist in patterning processes.

To expand research in this critical area, two new SEMATECH Centers of Excellence were established in 1988 to concentrate on lithography technology. The California Center for Lithography and Pattern Transfer will carry out research in DUV lithography. Under this center, studies will be conducted by faculty and graduate students at the University of California at Berkeley and at Stanford University, and by participants in a Deep UV Consortium composed of university and industry researchers. The Wisconsin Center of Excellence for X-ray Manufacturing Technology has been established at the University of Wisconsin at Madison and will benefit from the synchrotron X-ray source operated by the university. Although the international competition has already made major investments in X-ray lithography, U.S. researchers still hold leading positions in many of the component technologies; and funding of the Wisconsin Center will allow the U.S. semiconductor industry to capitalize on this technology leadership.



Micrograph of 800 nm aluminum lines, which remain between 0.96 µm of PMGI after metal lift off.

Chemically Modified Photoresists and Their Application to VLSI Processes

DUV lithography, planned for use in manufacturing megadevice ICs in the 1990s will require new photoresists. This project is addressing the need for new photoresist materials that are resistant to plasma etch environments.

The characteristics of polyimide that make it suitable for microelectronics are good dielectric properties; planarizing ability; radiation resistance; and thermal, mechanical, and chemical stability. Patterning polyimide films in an oxygen plasma using conventional photoresist is difficult because of the similar etch rates of the two organic materials. In an effort to increase the etch resistance, researchers at Charlotte have modified conventional photoresist by the incorporation of a phosphorus-containing compound. The modified resist forms an etch barrier layer when exposed to oxygen plasmas. In laboratory experiments, no measurable resist etch rate could be detected after this barrier layer was formed. The modified resist has been successfully used to mask and etch 12 µm of polyimide.

The modified photoresist remains soluble after oxygen plasma exposure. This property has allowed submicron two-layer metal liftoff processes to be successfully accomplished. The structure shown in the micrograph is aluminum that has been deposited in trenches etched in a PMGI dielectric. This structure was formed by exposing and developing the modified resist above a layer of PMGI. The PMGI was etched, and 96% aluminum and 4% copper alloy was evaporated. The metal was lifted-off by dissolving the modified resist with a 5-minute acetone immersion in an ultrasonic bath. This work is the subject of a patent application filed with the U.S. Patent Office in 1988.

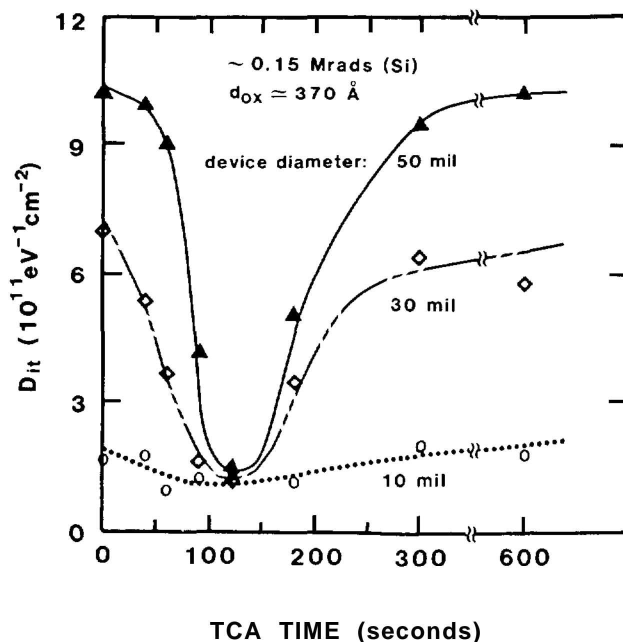
Professor Farid M. Tranjan
University of North Carolina at Charlotte

A focus on the manufacturing process is key to achieving low cost and ease of production. Further, as continuing advancements are made in the device and circuit technology, process technology improvements become necessary. Limitations are reached both in the properties of the materials used and in the process procedures employed so that they no longer may be controllable to the required degree or meet other conditions for the manufacture of the higher-performance, greater-density IC structures. In particular, submicron integrated circuits will require the introduction of new materials, and the manufacturing process will be carried out at lower temperatures or with less time at elevated temperatures. In addition, the sensitivity of the final product parameters to process variations is increasing — necessitating the development of new processes with less sensitivity and *in-situ* measurement methods that will more tightly control the process conditions. Accurate process models are essential for determination of process centering and process sensitivities. SRC process technology research is focused on investigating new materials and process methods and developing physically based process models.

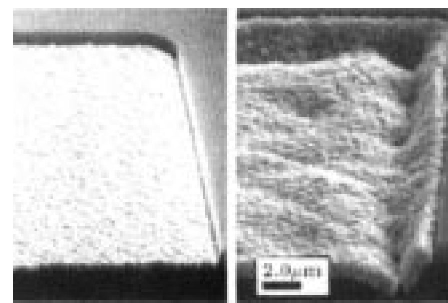
Radiation Hardness and Hot-Electron Effects

Being investigated are the effects of 1 , 1 , 1 trichloroethane (TCA) in the silicon thermal oxidation environment on the hardness of the resulting gate oxide structure to damage caused by ionizing radiation and hot-electron injection. It has been found that the use of minute amounts of TCA during the initial stage of oxidation dramatically improves the hardness of the interface.

Professors T.P. Ma and R.C. Barker
Yale University



Interface trap peak density generated by X-ray irradiation as a function of TCA time for different gate size. TCA bath temperature is kept at 5°C, and the pickup rate of TCA is approximately 35 mg/min.



The figure on the left shows the W film morphology after selective W deposition. The figure on the right shows the new morphology of the W pad after a 900°C anneal that resulted in silicide formation, with massive silicon consumption and cracking of the film.

Tungsten Silicide Films

Selective CVD tungsten (W) is being evaluated for VLSI metallization and silicides for device contacts. Silicide formation is a possible consequence of exposure of W to high temperatures. For oxide-confined W features, Si consumption, volume changes, and stress concentrations at edges during silicidation anneals can produce large undesirable changes in morphology. Also, the high temperature behavior (e.g., de-adhesion, silicide forming reaction) of W thin films is sensitive to interface contaminants from the CVD process as well as from other processes, Results of high temperature anneals are thus an indicator of the overall quality of the tungsten/substrate interface. The figures above show the morphological changes that can result from silicide formation in pads of CVD W.

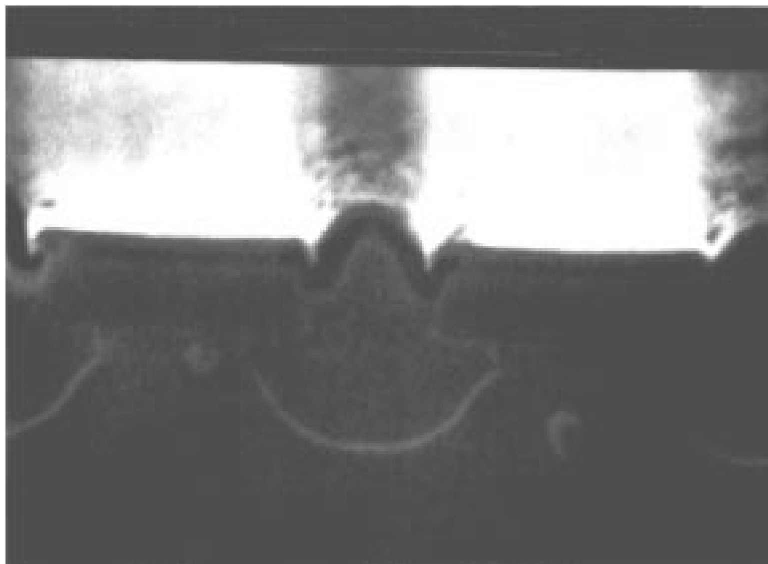
Professor James W. Mayer
Cornell University

Professor S. Simon Wong
Stanford University

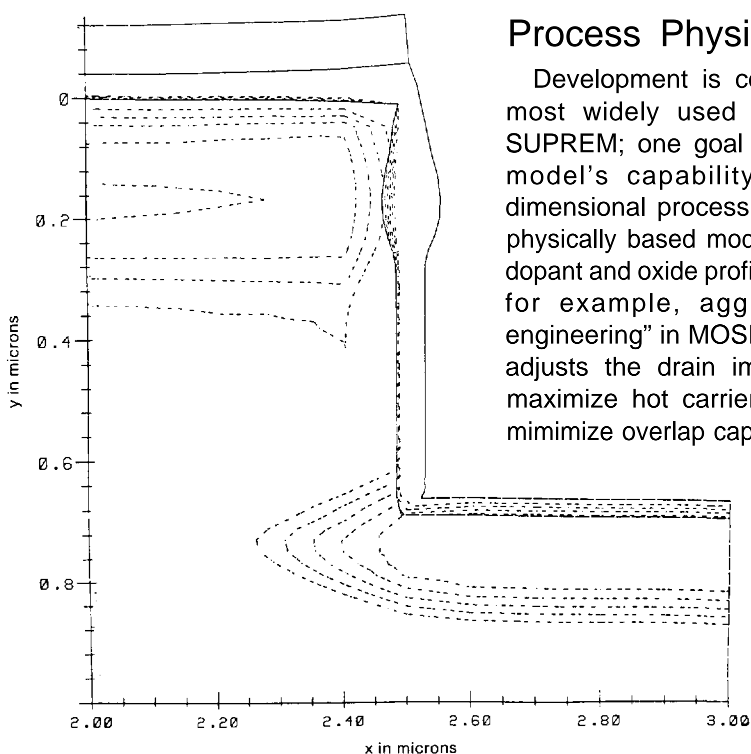
Field Oxide Thinning in Poly Buffer LOCOS

Field oxide thinning as a function of the spacing of the transistor geometries for the poly buffer LOCOS process has been examined, and a phenomenological model has been developed. The figure is a SEM of a narrow field oxide stripe produced by high temperature oxide growth using a Si_3N_4/polysilicon/SiO_2 isolation stack designed to reduce encroachment to 0.1 μm. Note that reduced thinning of the field oxide is achieved by the high growth temperature which reduces the field oxide viscosity and alleviates the oxidation-inhibiting stress in the oxide.

Professor J.P. Krusius
Cornell University



Narrow field oxide stripe exhibiting reduced field oxide thinning.



SUPREM-IV: Oxidation of a small trench structure.

Process Physics Modeling in SUPREM-IV

Development is continuing on the most widely used process model, SUPREM; one goal is to extend the model's capability to be a two-dimensional process simulator, using physically based models to predict 2D dopant and oxide profiles. This enables, for example, aggressive "drain-engineering" in MOSFETs, where one adjusts the drain impurity profile to maximize hot carrier resistance and mimimize overlap capacitance. The full stress-dependent model is capable of predicting second-order effects, such as the "bird's head" structure due to different nitride thickness in local oxidation structures. It also allows the stress in the silicon substrate to be calculated. The SUPREM-IV figure shows the oxidation of a small trench structure. A high dose boron implant at the wafer surface increases the sidewall oxide thickness at the top of the trench because the high dopant concentration enhances the oxide growth rate. The boron concentration falls sharply near the trench because of boron segregation into the growing oxide. A light phosphorus implant at the base of the trench diffuses farther than normal because interstitials generated by the oxidation enhance the dopant diffusion. The oxide thickness at the lower corner of the trench is thinner than normal, posing a possible reliability problem.

Professor James D. Plummer
Stanford University

Research: Plasma Processing

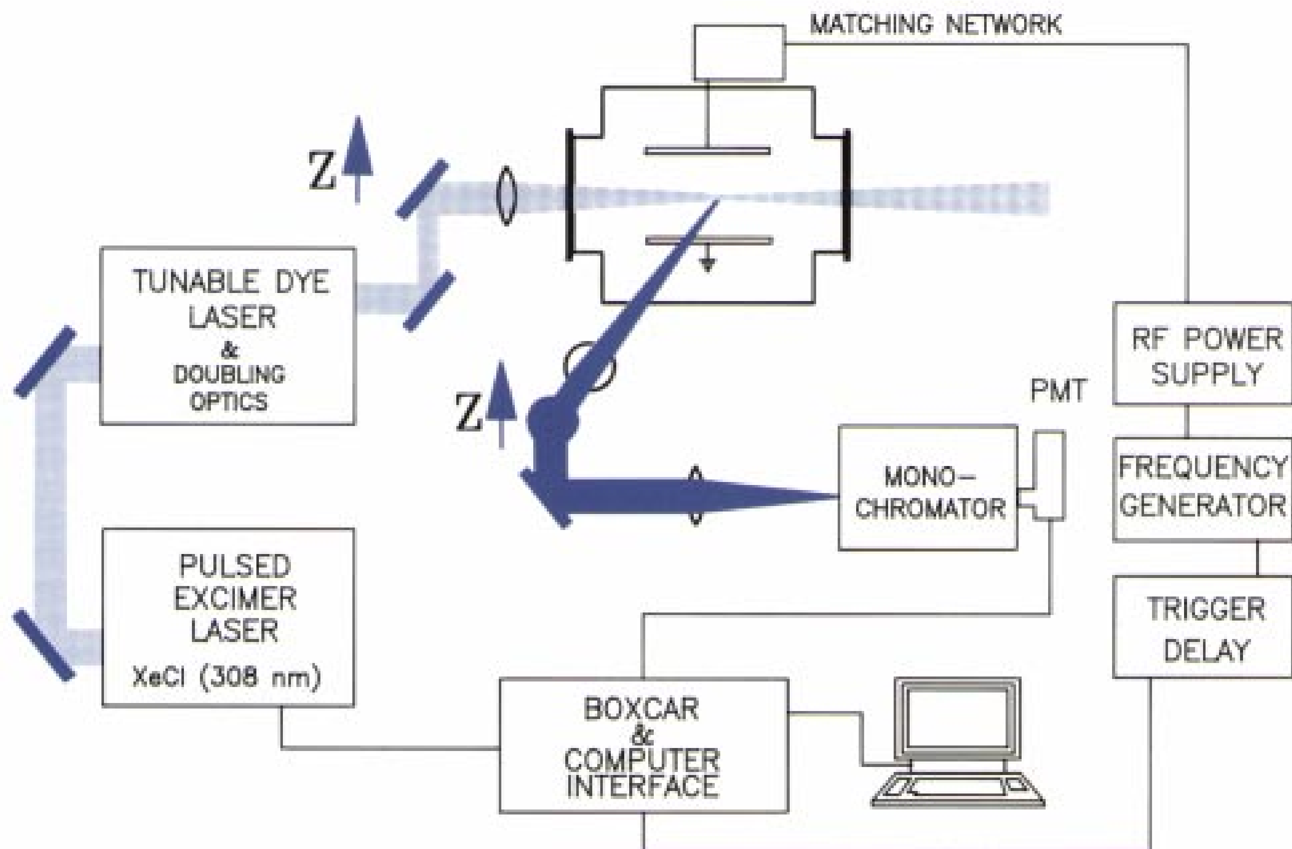
Plasma-enhanced etching and deposition tools have been used for some time by the semiconductor IC manufacturing industry. Typically, these tools have been tuned during manufacturing to optimize their performance for a specific device/circuit configuration. This tuning is usually done empirically without adequate understanding of the physical processes being controlled. Thus, when the variance of a process becomes too large, the source of the disturbance often is difficult to isolate; and the result is excessive downtime.

To manufacture integrated circuits with submicron feature sizes, greater control of the etching and deposition processes will be needed for achieving the required tolerance, uniformity, and throughput constraints. This, in turn, will require improved understanding of the equipment and process parameters and more precise measurements of these parameters.

Characterization and Modeling of Anisotropic Plasma Etching Processes

The accompanying schematic is a diagram of the apparatus being used to study the time dependence of the atomic chlorine concentration in a parallel plate etching reactor. The concentration of Cl is detected as a function of position by measuring the fluorescence radiation from Cl after it is excited by the incoming laser radiation. This work has shown the significance of Cl loss by recombination with the electrodes and nonuniform etching resulting from compositional differences in the two electrodes.

Professor Herbert H. Sawin
Massachusetts Institute of Technology

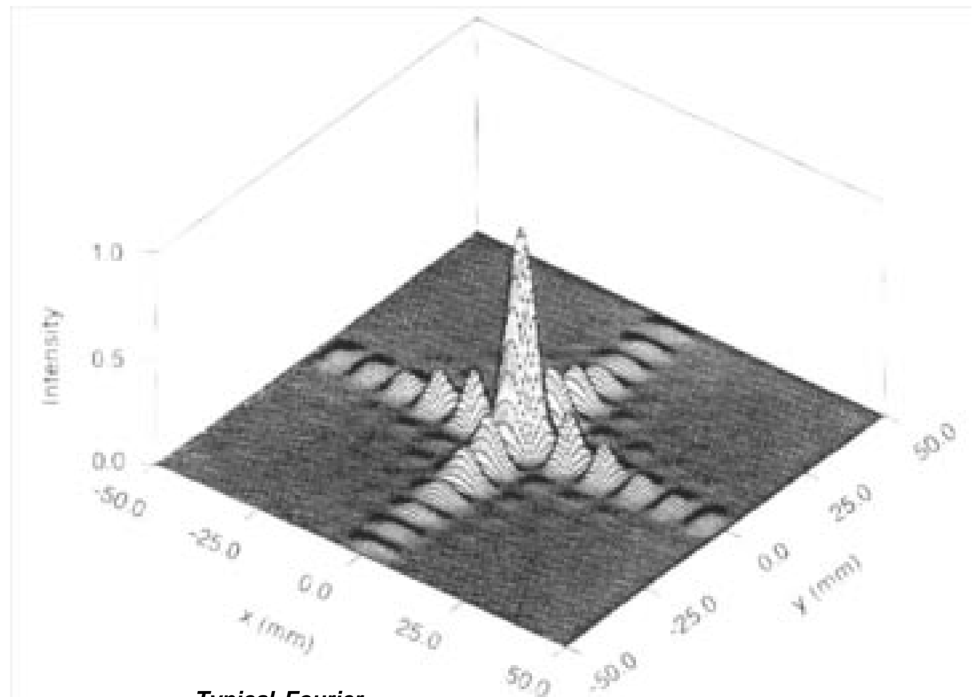


Schematic of Laser-Induced Fluorescence Apparatus

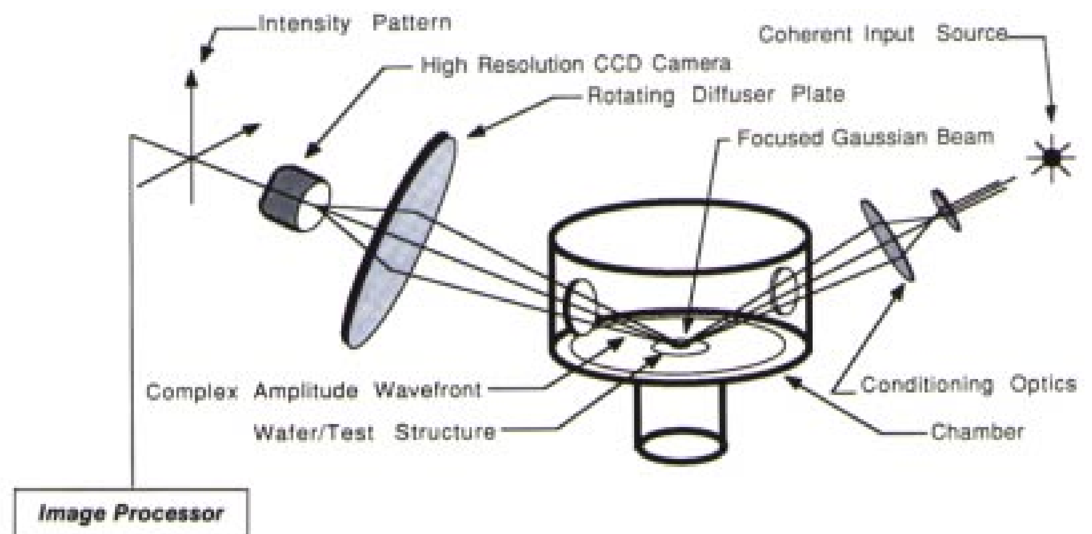
Fourier Imaging for In-Situ Control of RIE

Reactive ion etching (RIE) is being utilized as a vehicle for examining issues associated with automated sensing, control, and facilities integration. Among the *in-situ* techniques under investigation for monitoring wafer topography during the etching process is Fourier imaging. In this process, a coherent optical beam is filtered, magnified, and focused onto a dielectric feature on the wafer surface through an input port on the reactor. The two-dimensional complex amplitude distribution from the wafer surface is then imaged via a rotating diffuser plate onto a CCD imaging array. This pattern represents the Fourier transform of the wafer surface, translating the surface topography to the frequency domain. The resulting intensity distribution is analyzed by an image processor to produce topographical data from the wafer surface. For a surface feature nominally 10 μm wide, for example, the measured feature resolution is about 30 nm.

Professor Ken D. Wise
and Dr. Michael Elta
University of Michigan



Typical Fourier intensity distribution of a rectangular feature.



Principal components of the Fourier Imaging System. This system converts surface topography information to the Fourier domain to realize in-situ, real-time process monitoring for RIE.

Research: In-Situ Manufacturing

Emphasis on development of an *in-situ* IC manufacturing technology is increasing because of considerations arising from the established trend toward a larger volume of ASIC production (whereby a large variety of IC designs are manufactured at relatively small volumes for each design), increasing demands for lower defect density as dimensions are further reduced (approaching 0.1 μm minimum feature size), and continuing pressure to maintain an acceptable cost of manufacture. As a result of a research-planning workshop held in the spring of 1985, the SRC has had *in-situ* manufacturing research underway for the past four years. *In-situ* processing involves the positioning of single wafers in a carefully controlled contamination-free environment where a succession of fabrication tools are brought to the wafer. One *in-situ* concept employs a non-serial, beam-writing lithography tool that is compatible with a resistless all-additive process technology. SRC research projects arefocused on different facets of this concept.

In-situ Vacuum Multiconnected MBE and Analysis Stations installed at the Illinois Epi Center in 1988.

Epi Center at Illinois

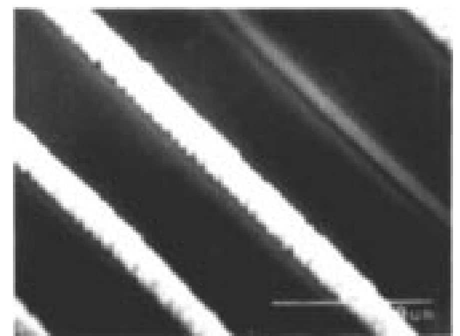
The Epi Center, inaugurated in the fall of 1988, is an MBE megacomplex. It consists of seven separately-pumped, interconnected growth chambers located in a specially constructed clean room. Also included are *in-situ* analytical stations, including RHEED, XPS, spectroscopic ellipsometry, Raman scattering, and triple axis X-ray diffraction. The wafer may be transported between the growth chamber and these analytical tools while being maintained in the controlled environment. Techniques are being developed for the selective deposition of high quality epitaxial silicon at conditions approaching room temperature. The Epi Center is presently being used by SRC-sponsored researchers to investigate low-energy accelerated-beam doping during MBE Si and the use of accelerated metal-ion beams for controlling the microstructure and topography of metal gate and contact layers on insulators and semiconductors.

Professor J.E. Greene
University of Illinois at Urbana-Champaign

Technique for Patterning

A process for "latent" image patterning of interconnect on a silicon substrate followed by nucleated growth has resulted in the enhancement of conductor-line thickness to more than 1.0 μm. Thin (less than 50 nm) aluminum lines have been defined by irradiating either the silicon substrate or a silicon-oxide-coated wafer with a 257 nm laser in an atmosphere of dimethyl aluminum hydride (DMAIH). Following initial activation, continued deposition is accomplished by heating the wafer *in-situ* to 150°C. The SEM shows conductor stripes formed by this process next to a non-thermally grown conductor line.

Professor Richard M. Osgood, Jr.
Columbia University in the City of New York

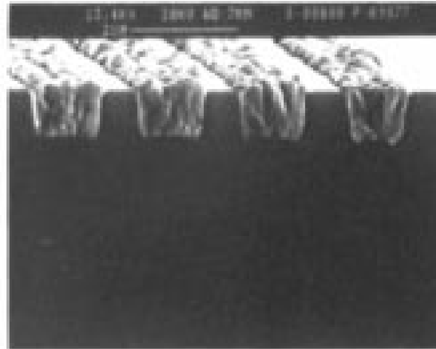


Micrograph of thermally grown lines next to a non-thermally grown line.

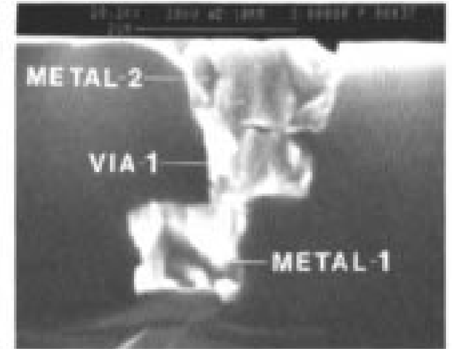
A Multilevel Tungsten Interconnect Technology

A multilevel tungsten (W) interconnect technology, which is inherently planar, has been developed to address the various issues of metallization for VLSI. This technology relies on the implanting of Si into oxide channels that are later selectively filled with W and has been extended to realize three levels of W metallization. The advantages include planar surface after each level of metallization, self-aligned and stacked vias, and high resistance to electromigration. The minimum metal pitch is 2 micrometers at all levels. Line resistivity is approximately 7 $\mu\Omega$-cm and contact resistance is less than 0.5 $\Omega/1\ \mu$m square contact.

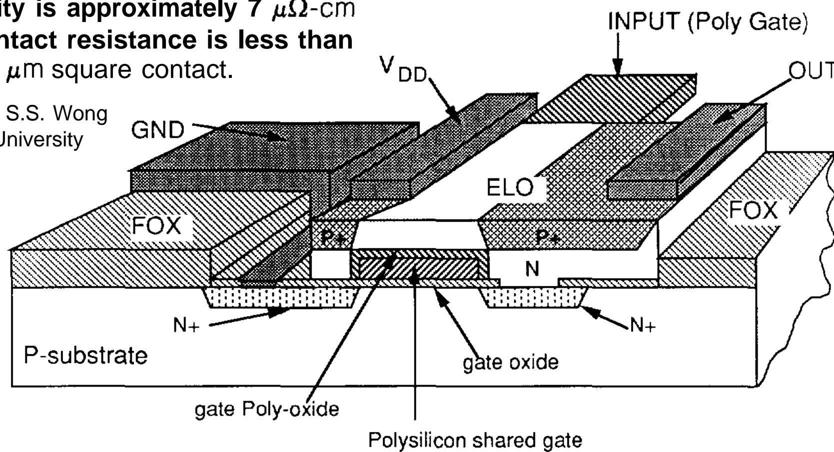
Professor S.S. Wong
Cornell University



Micrograph of tungsten interconnect cross section.



Micrograph of Tungsten plug between two levels of interconnect.



Three-Dimensional Stacked Gate CMOS Inverter

Three-Dimensional CMOS Structures

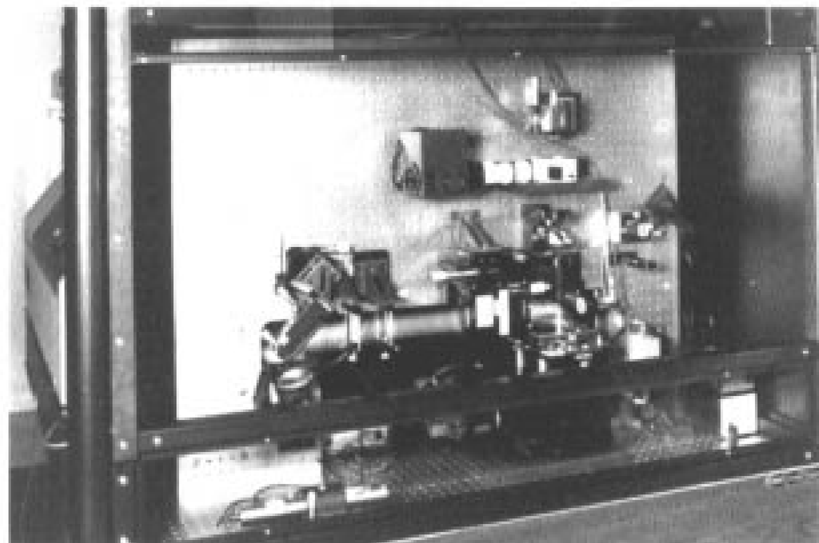
Evaluation of the Si/SiO_2 interface created by selective epitaxial lateral overgrowth of monocrystalline silicon over existing thermally oxidized silicon indicates interface quality comparable to that obtained between thermally grown oxide and the silicon substrate. The silicon overgrowth can thus be used as the basic building block of an *in-situ* manufacturing process for the fabrication of three-dimensional CMOS ICs.

Professor Gerold W. Neudeck
Purdue University

Gas Immersion Laser Doping

Gas immersion laser doping (GILD) is being investigated for junction formation in ULSI processes. High-energy excimer laser excitation is being used to produce surface melting of the source/drain regions in the presence of the desired dopant. Crystalline regrowth occurs with a resulting shallow 50-nm-deep junction which has a high dopant concentration gradient at the metallurgical junction edge, meeting the requirement for submicron device structures.

Professor Thomas W. Sigmon
Stanford University



Laser Apparatus for GILD Process

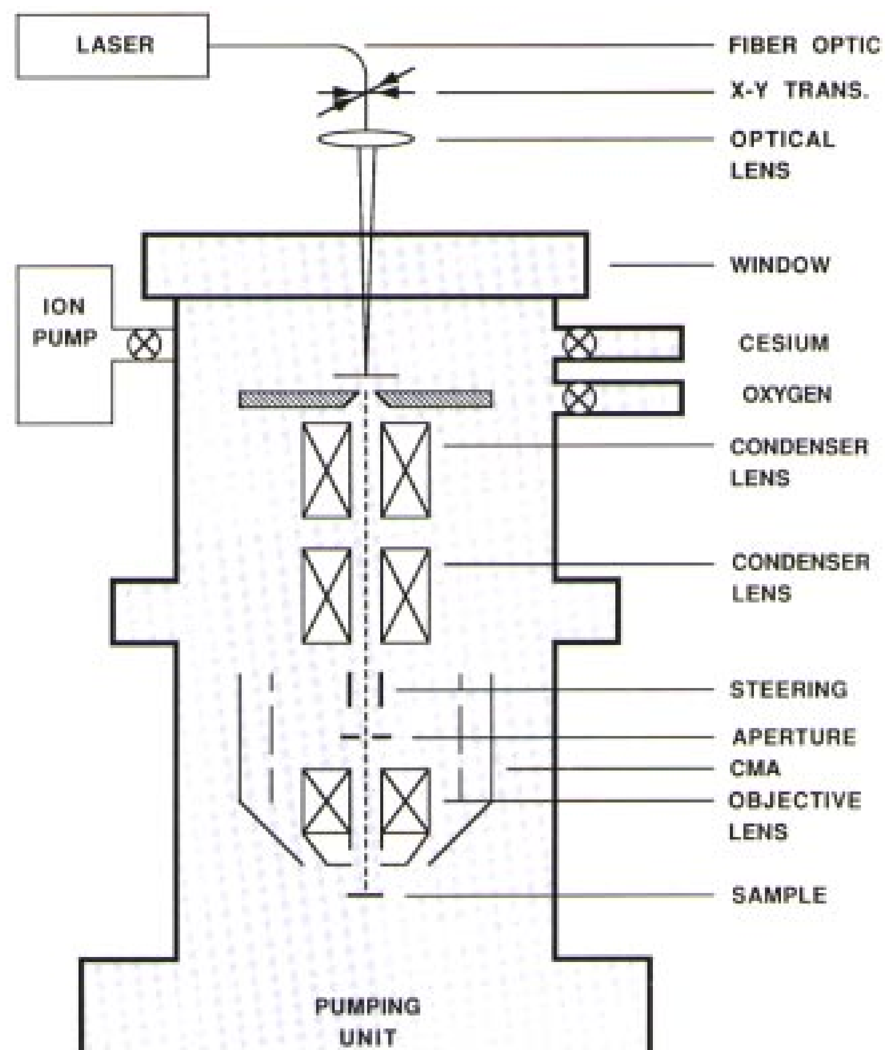
In order to be able to manufacture submicron ICs with high throughput and reliability, the vision of semiconductor metrology must be extended far beyond where it is today. General improvements are essential in the ability to measure and to understand what is being measured in order for U.S. technology to be at the leading edge of IC fabrication. To do this, an effort should be made to evaluate how measurements are done in other fields. At the dimensions being considered for semiconductor technology, much could probably be learned from the biological sciences.

For 0.25 μm feature-size integrated circuits, particles as small as 20 nm will have to be detected on a wafer, or a methodology will be needed for establishing that process tools are not producing such particles, More precise techniques for measuring exposure and profile in photolithographic patterns are necessary. More precise methods to measure mask registration between layers are essential. Accurate temperature measurement in the presence of emissivity changes during deposition is required. This is especially true for rapid thermal processing where uniformity is also a major concern. Real-time measurements of the composition and properties of films during deposition is needed to reduce rework time. This applies to dielectrics, interconnection metal and isolation, and planarization of glasses.

Time Domain Metrology for ULSI Circuits

A high-speed (<70 ps), high-spatial-resolution (<100 nm), time-resolved metrology system has been developed for measurement of voltage waveforms on ULSI circuits. The equipment approach is shown in the schematic diagram. A pulsed or CW laser in the 600 to 750 nm wavelength is coupled through fiber optics, a converging lens, and a window in the vacuum system onto the backside of a p+ GaAs film whose front side is coated with cesium oxide. The cesium oxide coating gives the conduction band of GaAs a negative electron affinity with respect to the vacuum level. As a result, a high intensity electron beam can be excited by low energy lasers. Based on initial results, it is anticipated that the brightness of a field emission cathode with the stability of a thermal source will be achieved. These features will greatly enhance both the time and spatial resolution needed to evaluate the performance of ICs with higher clock rates.

Professor Noel C. MacDonald
Cornell University

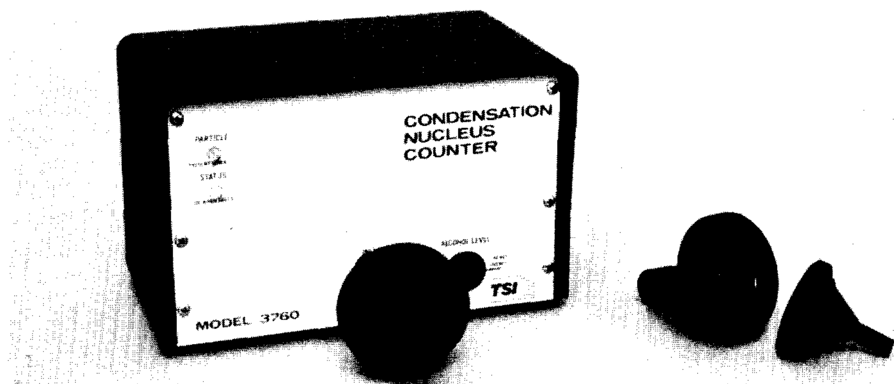


Schematic diagram of electron gun with transmission mode GaAs negative electron affinity cathode mounted on a scanning Auger microprobe.

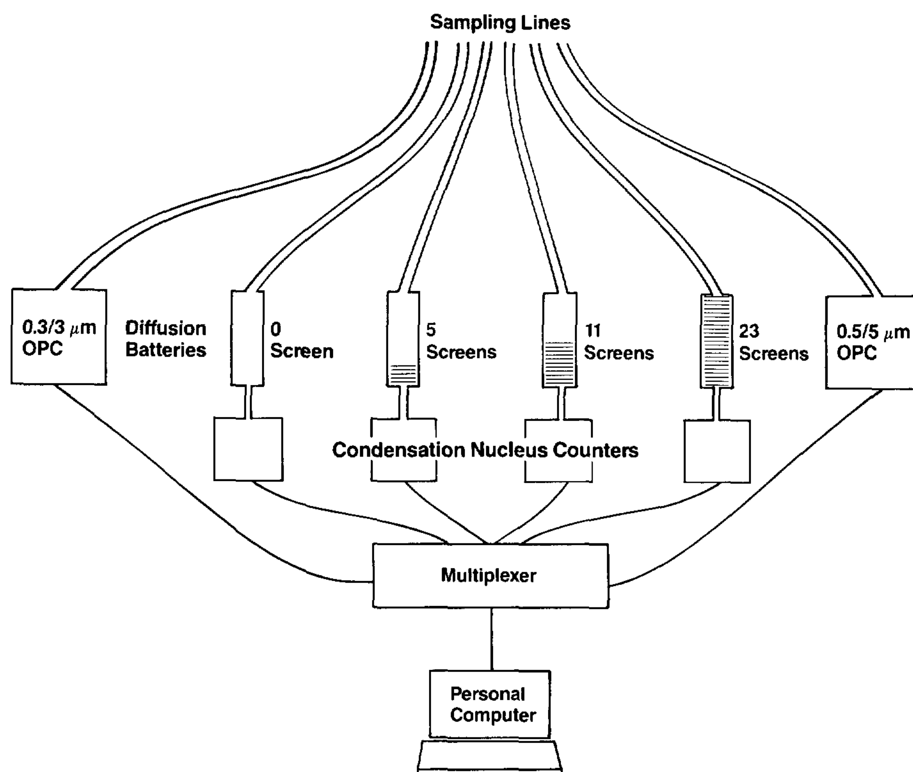
Commercial Instrument from SRC Research

Based on metrology research conducted at Research Triangle Institute, a commercial product was derived in 1988 by TSI Incorporated of St. Paul, Minnesota — a manufacturer of particle measuring instrumentation. RTI researchers designed a parallel array of diffusion battery/condensation nucleus counter combinations (DB/CNCs) to create a unique configuration capable of measuring particle concentrations typical of state-of-the-art semiconductor clean rooms in near real time without lengthy data inversion routines. The figure illustrates how the measurement is done. Diffusion batteries contain a series of screens, the number of which determines the smallest size particle that can transit a particular battery. In the condensation nucleus counters that follow, the particles are enlarged by vapor condensation and then are detected by conventional optical particle counters. The photograph shows the packaged TSI product that is capable of a parallel sampling of a particle size distribution extending over the range of 0.01 to 0.2 μm.

Dr. Robert P. Donovan
Research Triangle Institute



TSI Particle Size Selector, Model 376060, shown attached to a 3760 CNC and also shown partially disassembled.

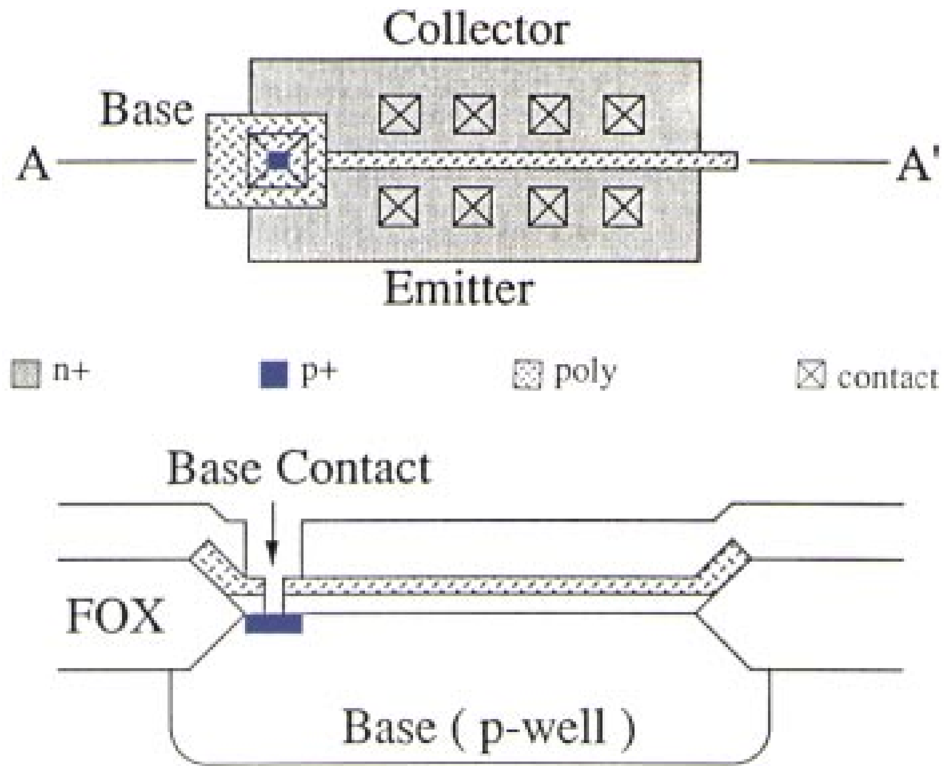


Schematic of parallel array of DB/CNC pairs plus two optical particle counters (OPCs).

Historically, bipolar and MOSFET devices have been used separately in those applications where their unique advantages resulted in the greatest benefits to the user. However, in the continuing march toward finer dimensions and greater performance, it is necessary to find ways of using both technologies for selected parts of the same VLSI/ ULSI device. On the other hand, this commonly leads to additional process complexity with the associated yield and cost disadvantages.

For those cases where the optimum is represented by limited use of bipolar structures in a largely MOS device, the concept of lateral bipolar transistors has been tempting. But this has usually resulted in poor bipolar performance. Researchers at Stanford and the University of California at Berkeley have now developed a device that largely overcomes this problem.

Taking the concept of combining the desirable characteristics of both bipolar and FET technology one step further, a research team led by Professor Plummer at Stanford has developed and built a silicon-based version of a recently proposed device structure. The BiCFET indeed exhibits many of the advantages of a traditional bipolar device as well as the characteristics that have made possible the agressive scaling of MOS devices over the last 15 years. As a result, it is expected that the device is well-suited for ULSI.



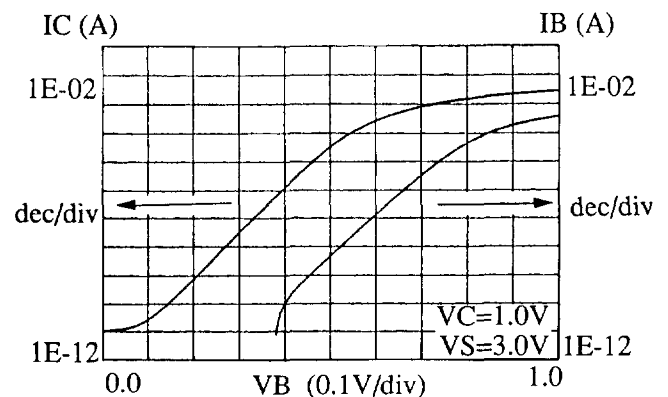
Top and cross-sectional view of lateral bipolar transistor.

High Gain Lateral Bipolar Transistor

A lateral bipolar transistor with very high current gain has been developed. The bipolar transistor is very similar to a MOSFET and is inherently available in a CMOS process. The emitter and collector are the source and drain, respectively; whereas the base is formed by connecting the gate and the well. In such a configuration, the base region is mostly depleted; and, hence, the effective base width is much shorter than the drawn one. Current gain larger than 1,000 for drawn base width of 0.5 μm has been achieved.

Professor S. Simon Wong
Stanford University

Professor Ping K. Ko
University of California
at Berkeley

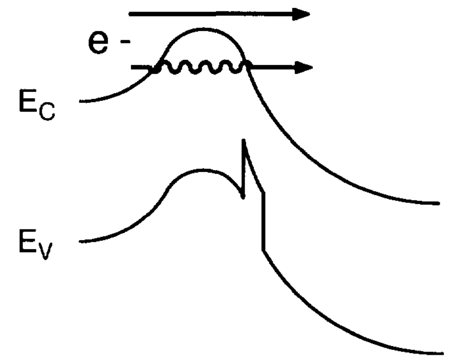


Performance of lateral bipolar transistor. Drawn base width is 0.4 μm.

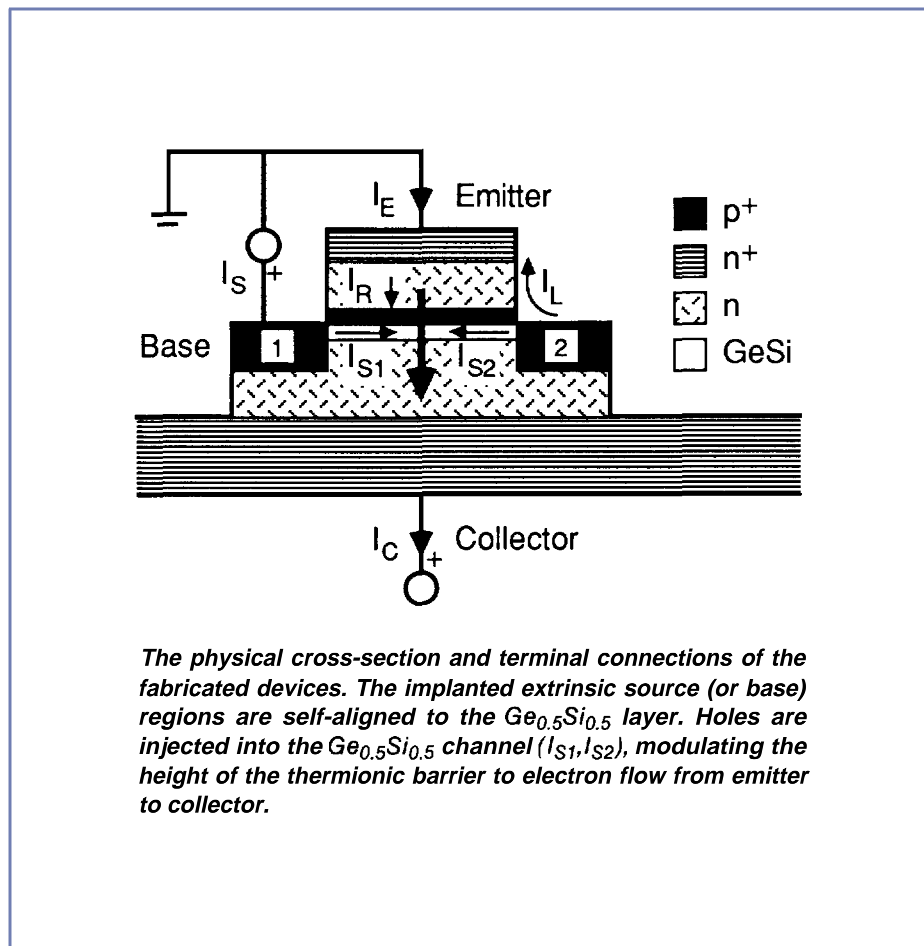
Inversion Base Transistors

Inversion base transistors are of interest as a potential VLSI device because of their short intrinsic switching time constants and large current drive capability. In addition, their narrow base width (approximately equal to 10 nm) reduces the scaling constraints for submicron lateral geometries. Recently, an inversion base transistor has been demonstrated, based on the Ge_xSi_{1-x} system, in which molecular beam epitaxy growth allowed fabrication of the abrupt doping profiles and the commensurate $Ge_{0.5}Si_{0.5}$ region. Although the electrical output characteristics of these transistors are similar to those of standard bipolar devices, quantum effects play a significant role, especially at low operating temperatures (see figures on this page). The transistors were shown to have current gains between 300 and 500 at a current density of $5x10^4$ A/cm^2, making them very suitable for digital applications.

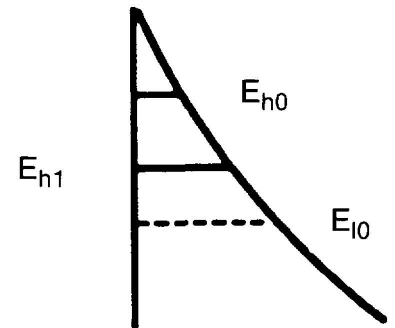
Professor James D. Plummer
Stanford University



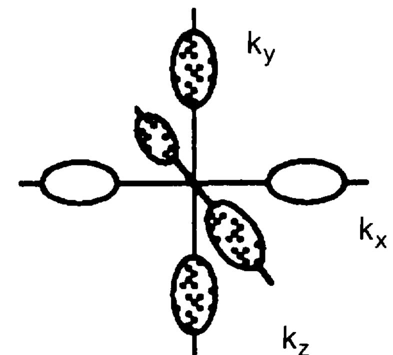
The band structure — showing the minimum conduction band energy, E_C, and maximum valence band energy, E_V, as a function of verticaldistance through these "BICFET" devices. The inversion channel is contained by the offset in the valence band between $Ge_{0.5}Si_{0.5}$ and silicon.



The physical cross-section and terminal connections of the fabricated devices. The implanted extrinsic source (or base) regions are self-aligned to the $Ge_{0.5}Si_{0.5}$ layer. Holes are injected into the $Ge_{0.5}Si_{0.5}$ channel (I_{S1},I_{S2}), modulating the height of the thermionic barrier to electron flow from emitter to collector.



Inversion channel formed by a very narrow quantum well.



Electron transport across the thermionic barrier includes a tunneling component, involving only four of the six equivalent conduction band minima.

Research: Analog ICs

Design tools for analog and mixed analog/digital integrated cicuits have lagged behind those for digital ICs. An SRC workshop was held in December, 1988, on Analog Design Automation to explore major issues and research needs in analog CAD and to begin to identify components of a strategic analog CAD roadmap.

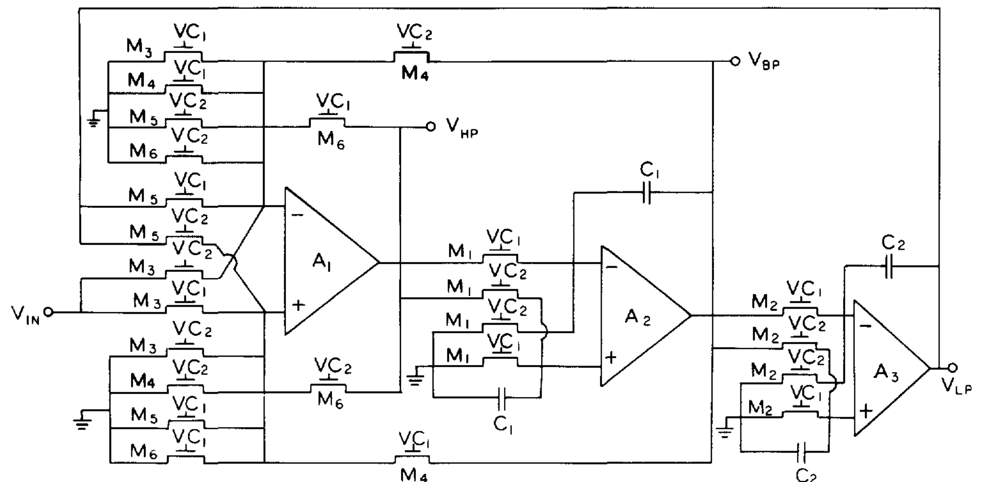
In addition to the SRC-funded projects highlighted on these pages, research is underway at Carnegie-Mellon University by Professors R.A. Rutenbar and L.R. Carley on the ACACIA analog synthesis system. The OASYS portion now designs CMOS Op Amps and comparators with excellent agreement between measured performance and specifications. Future work will include the synthesis of DACs and ADCs.

At the University of California at Berkeley, analog module generation research directed by Professor P. Grey is focused on the synthesis and automatic layout of CMOS SC filters (ADORE), Op Amps (OPASYN), and ADCs (SA-ADC). This work has been fully integrated on the OCT/VEM/RPC framework for CAD tools. Investigations continue on the automatic synthesis and layout of more complex and nonlinear analog cells with the goals of competitive area and performance with custom hand layout and CMOS process technology independence.

Continuous-Time Analog ICs for MOS VLSI

Continuous-time analog MOS ICs are naturally suited for high-frequency applications in mixed analog/digital MOS VLSI systems. Research at Ohio State is introducing innovative continuous-time circuit topologies and design methodologies for linear and nonlinear analog cells, providing such features as simplicity, versatility, reconfigurability, and a high degree of modularity. The new cells require less design time, make effective use of available VLSI CAD tools, and could eventually be part of an analog knowledge-based system. Theoretical foundations for the development of such cells include the goal of closing the gap between classical continuous-time analog circuits and MOS VLSI and on incorporating process/device nonideal effects and technology limitations into the design process. Results of these novel circuit design concepts on silicon have shown that MOS continous-time techniques can be successfully applied to the design of analog ICs.

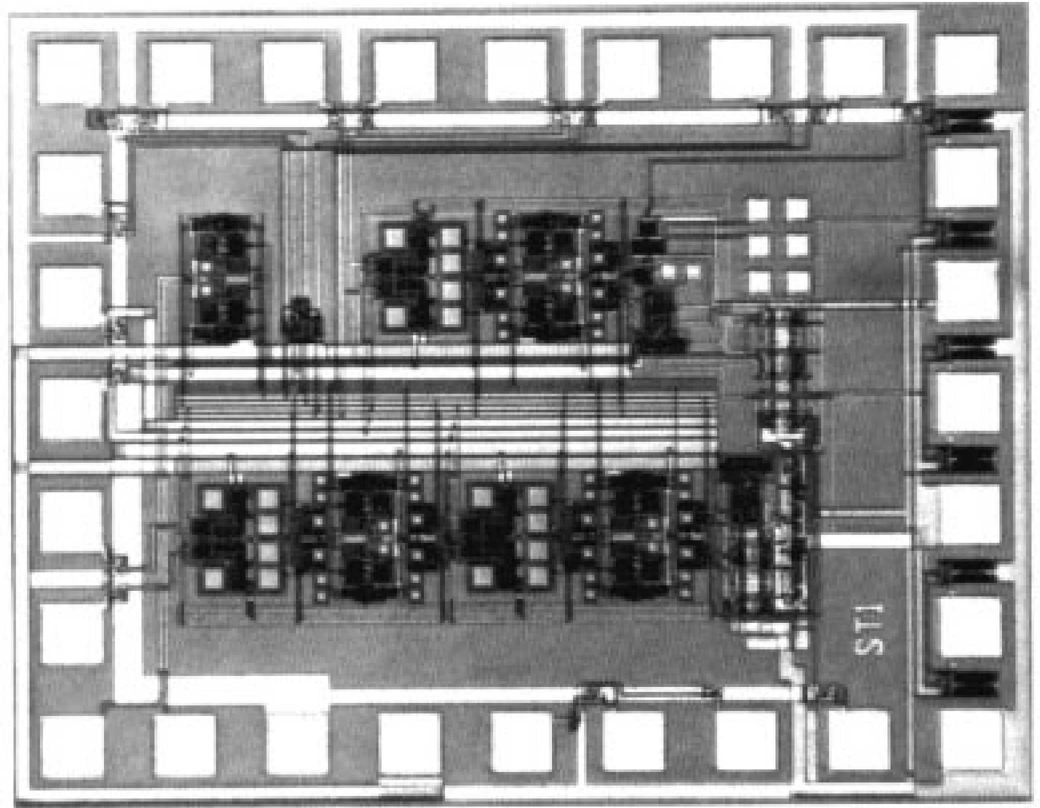
The new MOSFET-C universal filter structure, shown in the schematic, is successfully tuned with high precision over a wide range of pole frequencies, 0→100 kHz, by changing VC_1 or VC_2, using op-amps having only 1 MHz gain bandwidth. The structure was developed and fabricated using the 3.5 μm AT&T Bell Labs double-poly CMOS process and has an active area of only 0.7 mm^2. It provides the three basic filter functions of low pass, high pass, and band pass; and thus can be used in many on-chip signal processing applications, resulting in a cost-effective VLSI design solution.



MOSFET-C Universal Filter Structure

Current research is focused on the development of self-tuned, robust and programmable analog structures. This is very attractive from a CAD automation perspective since a single layout design for the cell, using programmability, can be performed instead of the layout's being redesigned to meet different design specs for the same cell. This avoids the use of layout compaction software packages which are primarily digitally oriented.

Professor Mohammed Ismail
Ohio State University



Die photograph of a second-order sigma-delta modulator designed at Stanford University and fabricated in a 1 μm CMOS technology at Texas Instruments Incorporated.

Oversampled Data Conversion Interfaces for VLSI Signal Processing

Architectural and circuit issues in the design of oversampled data conversion systems are being explored. Because such systems combine severe nonlinearities with feedback, the computation analysis of their behavior is especially demanding. Consequently, a major component of this research has been the development of reliable and efficient tools for simulating and testing oversampled systems. The initial results are embodied in the program MIDAS, a general purpose functional simulator for mixed digital and analog sampled-data systems. This program includes means for evaluating the influence of analog circuit imperfections of the performance of systems and provides distortion and quantization noise analysis, using a minimum error algorithm that is considerably more efficient than conventional spectral estimation methods.

A preliminary version of MIDAS has already been used for the design and evaluation of a second-order sigma-delta modulator suitable for use as a macro-cell in the design of custom VLSI signal processing interfaces. This circuit was integrated in a 1 μm CMOS technology at Texas Instruments as shown in the die photograph.

Professor Bruce A. Wooley
Stanford University

Knowing that continued scaling of bipolar and MOS devices will not continuously lead to improvement in integrated circuit performance while current technology permits fabrication of ever-smaller dimensions, the SRC is exploring device structures based on quantum principles.

In some instances, guidance in the development of a new field can be based on analogy with an existing technology. It is well known that electrons possess wave properties much like electromagnetic waves or photons. However, in conventional devices, interference effects due to this wave nature are unobservable for three principal reasons: (1) scattering processes cause phase randomization, (2) electrons have a large spread in energy (analogous to frequency of electromagnetic waves), and (3) electron transport takes place in numerous sidebands (analogous to multimodedness in waveguides). However, in submicron devices at low temperatures, all of these factors are minimized; consequently, quantum wires raise the possibility of duplicating, with electrons, many of the device concepts that are well-known in integrated optics or microwave networks.

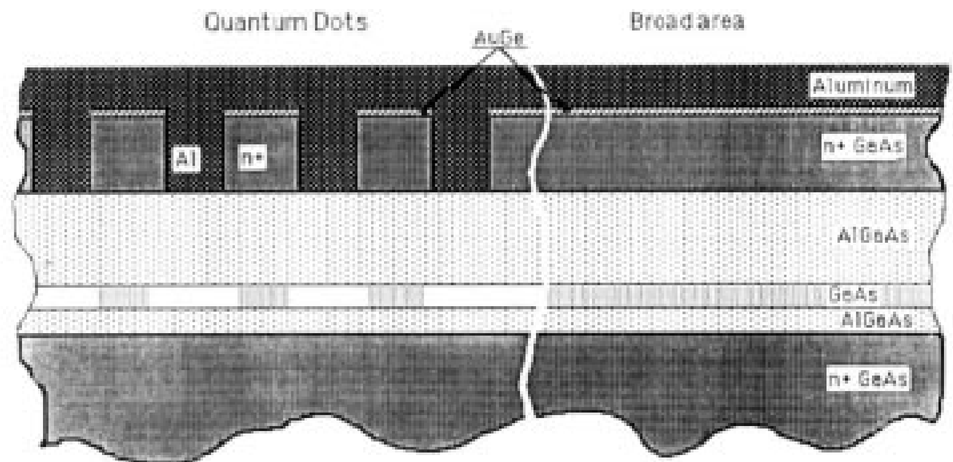
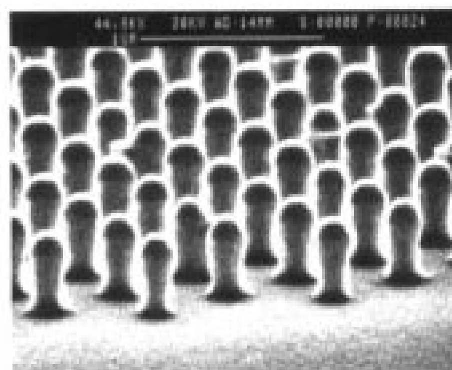


Figure Ia: fabrication of the Cornell quantum dot samples; Figure Ib: schematic of the wafer.

Physics of Submicron Scale Electron Confinement

The combination of patterning and MBE growth techniques has been used to produce “quantum dot” structures (isolated pockets of electrons containing a few to a few tens of electrons each). Figure 1 a illustrates the fabrication of the quantum dot samples. Figure 1 b indicates schematically the wafer—grown by MBE (in which a GaAs quantum well is grown, separated by an AlGaAs tunneling barrier having a thickness about 15 nm, from a degenerate n-type substrate). An insulating barrier of AlGaAs is grown above the well, and then an n+ semiconducting gate to which ohmic contact may be made with an AuGe layer.



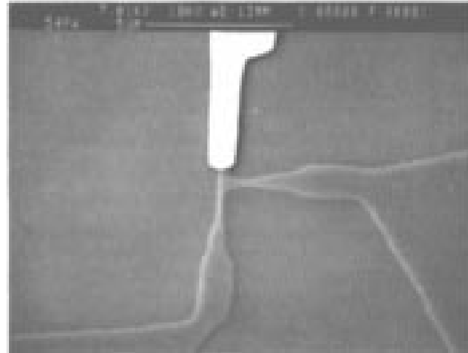
Quantum Dot Sample

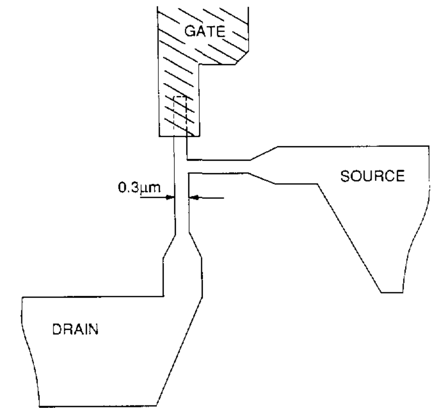
To prepare a quantum dot sample, the AuGe is evaporated in an hexagonal array of a million dots using E-beam lithography and lift-off. Reactive ion etching, with the AuGe dots as etch mask and the GaAs/AlGaAs boundary as an etch stop, leaves the sample shown in the micrograph. A final Al evaporation fills the voids to give a Schottky gate over most of the sample, interpenetrated by the array of n+ gates, as in Figure Ia. The quantum well is depleted under the Schottky gate but remains full under the n+ gate for a suitable range of biases applied to the gate structure. In a capacitance spectroscopy technique, tunneling is induced between the dots and the substrate by the AC voltages used to measure the device capacitance. The results are interpreted in terms of the electronic density of states of the dots and the tunneling conductance to the substrate.

Professor R.H. Silsbee
Cornell University

Quantum Devices Based on Microwave Analogies

In submicron devices at low temperatures: (1) devices can be shorter than a mean free path so that negligible scattering occurs; (2) electrons only at the Fermi level contribute to conduction, so the energy spread is minimal; and (3) the number of subbands is very small. A quantum wire structure analogous to a microwave network is shown in the figure. This structure can be viewed as a three-port network where the gate changes the reflection coefficient at that port. In microwave engineering, changing the load at one port (gate) of a multiport network changes the transmission between the other ports (source and drain). The current from the source to drain is modulated by the gate. A surprising feature of the quantum device is that the gate is not necessarily positioned between the source and the drain but can be placed anywhere within an inelastic scattering length. With single mode wires at low temperatures, a large fractional modulation should be possible. Tests of the device shown in the micrograph, fabricated by electron beam lithography at Purdue, verify that the remote gate does indeed modulate the current from the source to the drain.





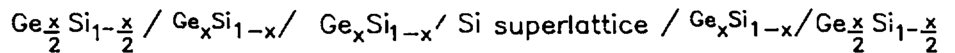
Quantum device based on microwave analogy. Line drawing identifies the features shown in the micrograph.

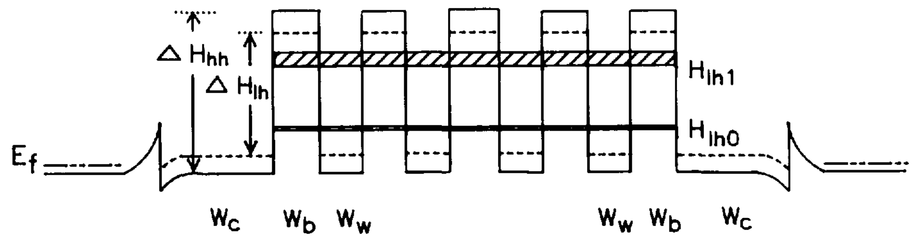
Professors Supriyo Datta
and Mark Lundstrom
Purdue University

Producing Quantum Devices by Molecular Beam Epitaxy

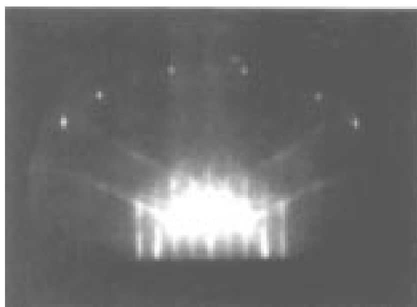
Molecular beam epitaxy (MBE) has been used to form a superlattice of $Ge_{0.4}Si_{0.6}/Si$. In superlattices, the compositional periodicity results in energy minibands comparable to the electronic energy bands normally formed by atomic periodicity in a homogeneous crystal. Two-dimensional confinement of electron waves has been achieved within a fifteen period structure and, for the first time, hole transport has been observed through the minibands in the symmetrically strained superlattice. The high quality of the material is shown by the Kikuchi lines and high definition of the RHEED pattern.

Professor Kang L. Wang
University of California at Los Angeles

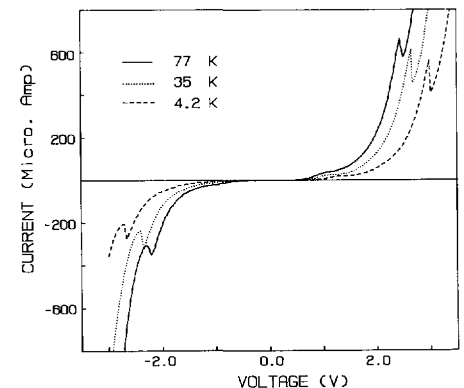




Schematic band diagram of the $Ge_{0.4}Si_{0.6}/Si$ superlattice showing miniband conduction process without bias.



Reflection high electron energy diffraction (RHEED) showing a (2x1) pattern along azimuthal angle of <110>, indicating a high quality of Si epitaxial layer growth by MBE.

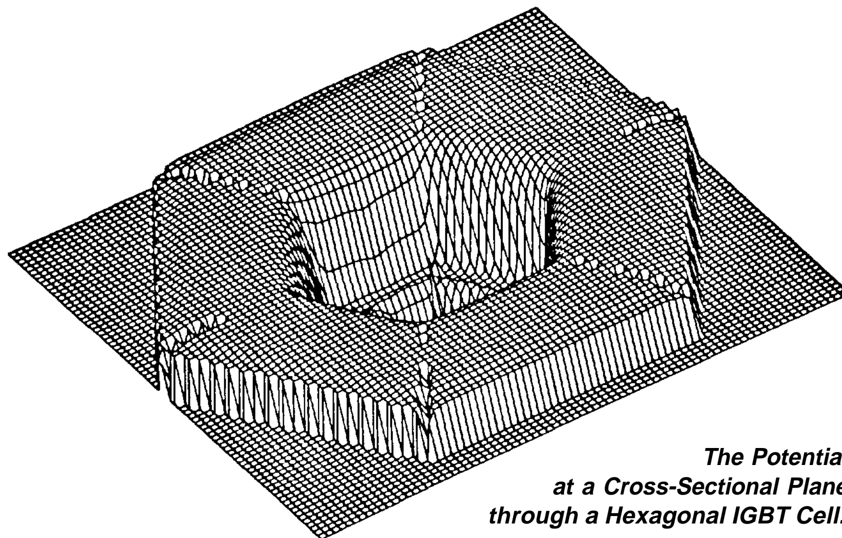


Observed current-voltage (I-V) relations of a superlattice. Barrier width = 1.5 nm; well width = 5 nm.

Research: Process and Device Modeling

As process technology matures and dimensions shrink, the modeling of higher order effects complicates the behavior of submicron transistors and their models. The challenge is presented to create models that reflect these effects accurately, yet have readily obtainable and computationally efficient parameters.

At the University of California at Berkeley, the new submicron CMOS transistor model BSIM2, created for the SPICE3 circuit simulator, can also model transistor behavior over a very wide temperature range (from 77 K to 500 K). At the California Institute of Technology, a simple submicron MOSFET circuit model that is continuous over all regions of operation has been derived and is being used to support analog sensory renewal network design. At Stanford, researchers have improved and enhanced the models used in the SUPREM process simulator and PISCES device simulator in collaborative research with the topological modeling activities of Berkeley's SIMPL project.

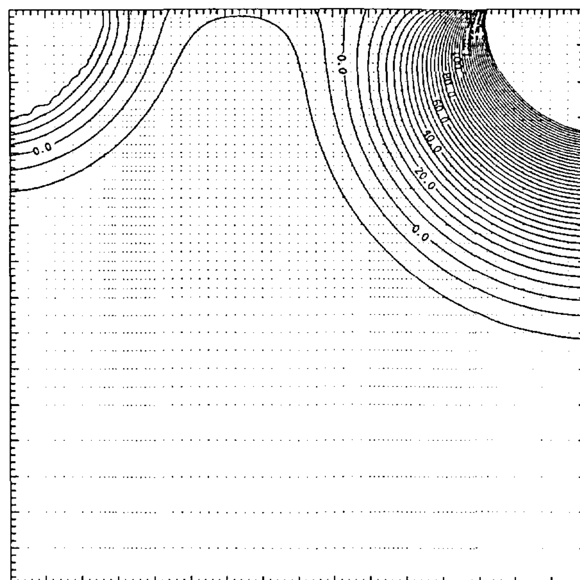


The Potential at a Cross-Sectional Plane through a Hexagonal IGBT Cell.

Numerical Modeling of Semiconductor Devices

Numerically efficient and accurate modeling of both semiconductor devices and interconnects is essential for expansion of current CAD facilities. In developing formulations and numerical techniques, theoretical and experimental studies are being conducted on devices such as the MOSFET and IGBT (insulated gate bipolar transistor), together with multiline interconnect configurations. New, globally convergent, iterative techniques, based on fixed point principles, are being developed for the solution of the discretized partial differential device equations. Features of these techniques make them quite robust and permit their implementation on computers with small RAMs. Moreover, these techniques are inherently parallel and ideally suited for implementation on parallel processors with fine-grain architectures Full-wave (suitable for arbitrary frequencies) formulation and numerical solution techniques have been applied in the study of interconnects Specific geometries of interest involve a number of lines on one or more planes with an inhomogeneous dielectric and arbitrary terminations. Topics being addressed include approaches to improve isolation, finite conductor thickness effects, characteristic impedance definitions, and the analysis of various discontinuities.

Professors Isaak D. Mayergoyz
and Kevin J. Webb
University of Maryland



Contour plot of the potential for a MOSFET. This example is for a 7 μm n-channel device with a 50 nm gate oxide, $10^{16}cm^{-3}$ acceptor substrate doping, 10^{19-3} donor junction doping, and an energy-dependent interface trap distribution with a peak 0.1 μm from the drain junction.

Research: Submicron Models

Over the years, sophisticated existing models of MOSFET devices have accurately predicted device performance. However, most models are directly or indirectly based on average or effective, rather than locally varying, parameter values. Extreme scaling and feature sizes approaching the dimensions of local nonuniformities now invalidate this approach. Different and more accurate models are required.

Research at the University of Texas at Austin has resulted in refined models for carrier transport in submicron-size devices, taking into account subtle effects of smaller features. University of California at Berkeley research has also resulted in a better understanding of the behavior of aggressively scaled devices. In this case, a software tool for CAE, named BSIM (Berkeley Short-channel IGFET Model) has been developed.

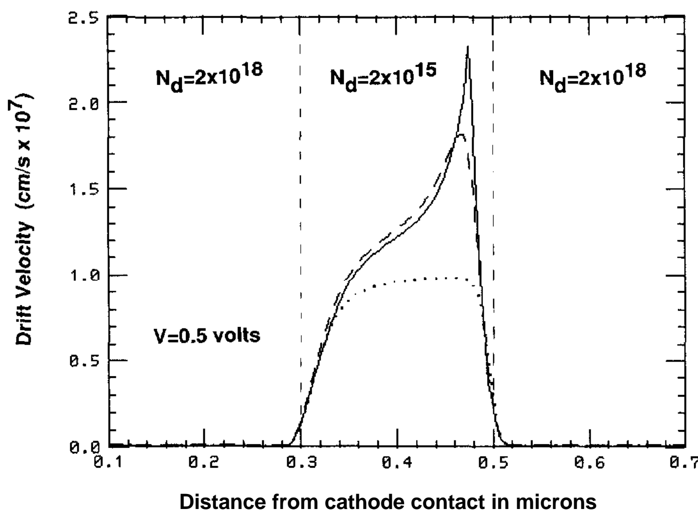


Figure 1. Velocity overshoot in N+-N-N+ silicon with 0.5 V bias. The solid line represents the complete hydrodynamic model, the dashed line results when the carrier energy is assumed to be entirely thermal. The dotted line is the solution given by the drift diffusion model with field dependent mobility.

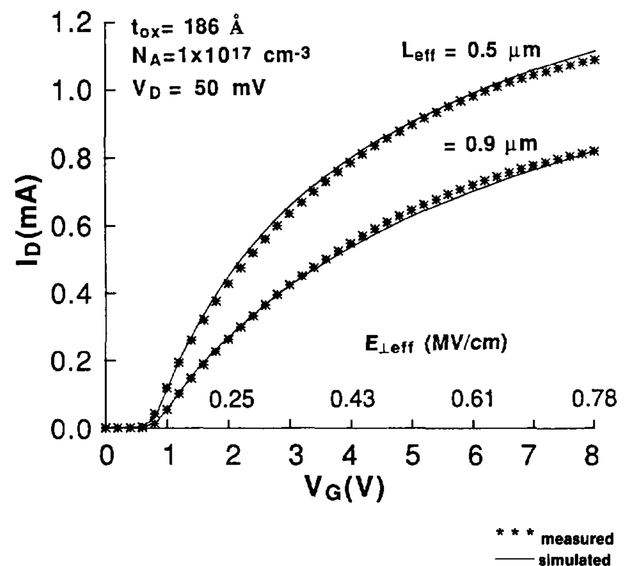


Figure 2. A comparison of simulated and measured drain current as a function of gate voltage for a submicron MOSFET.

Hydrodynamic Transport Model

As device dimensions shrink into the submicron regime, a field-dependent mobility is no longer able to accurately describe carrier transport within the drift-diffusion framework. The hydrodynamic model, based on the first three moments of the Boltzmann Transport Equation, offers a computationally efficient alternative to Monte Carlo methods for accurately describing such nonstationary transport, but the model poses a considerable numerical challenge for 2D device simulation. To evaluate the validity of approximations that allow use of reliable numerical algorithms, studies are being conducted on nonstationary transport in an n+-n-n+ silicon structure (Figure 1). Velocity overshoot becomes pronounced in silicon devices with active regions less than 0.3 μm. By studying transport in this 1D structure, researchers can better evaluate the appropriateness of simplifications that will aid in the development of a computationally efficient 2D device simulator.

Surface Mobility Modeling

Among the phenomena requiring accurate, efficient simulation is the transverse field dependence of carrier mobility in MOS inversion layers. Several attempts to develop a model for this phenomenon have realized limited success. A new modeling approach employs a new, important boundary condition and extracts the functional dependence on transfer field within the inversion layer directly from the experimentally measured average mobility. This approach guarantees that the resulting local field mobility will yield the experimental average mobility and has been applied to a mobility model for electrons in MOS inversion layers. The model is implemented in PISCES, and excellent agreement with experimental data has been achieved for a wide range of channel doping and transverse and longitudinal electric fields (Figure 2).

Professor Al. F. Tasch, Jr.
University of Texas at Austin

Research: Digital Synthesis

Digital synthesis is challenged by ever-growing complexity and intense market pressures to reduce product design times. SRC-sponsored research in digital synthesis tools now exists at every level of design abstraction.

On the lowest level of design synthesis from Boolean or logic descriptions, the logic synthesis tools from the two-level (EXPRESSO) and the multilevel (MIS) logic synthesis systems at the University of California at Berkeley can match or exceed expert human designers in either number of gates or performance.

One level of abstraction higher, digital logic systems can be synthesized that match strictly behavioral or functional descriptions. At Berkeley current logic synthesis tools are being extended from behavioral descriptions to combinational and sequential network synthesis. At Carnegie-Mellon, research continues on the System Architect's Workbench, an implementation system that works from register-transfer-level hardware descriptions. Recent work investigated tradeoffs in the partitioning of designs and area versus performance considerations in parallel (concurrent processing) and serial (pipelining) architectures. Additional work at this level of design abstraction is underway at the University of California at Irvine, Southern California, and Massachusetts at Amherst.

Research is also in progress at Carnegie-Mellon on specialized design tools that synthesize only a particular family of digital designs. The MICON project demonstrated the first successful board-level design in White Dwarf—a hardware accelerator board for finite element methods. "Designer Assistants" research provides highly specific expertise in a focused applications area. YODA is a generic expert system that has been configured to evaluate tradeoffs in circuit area, performance, and power dissipation for a wide variety of digital filter implementations.

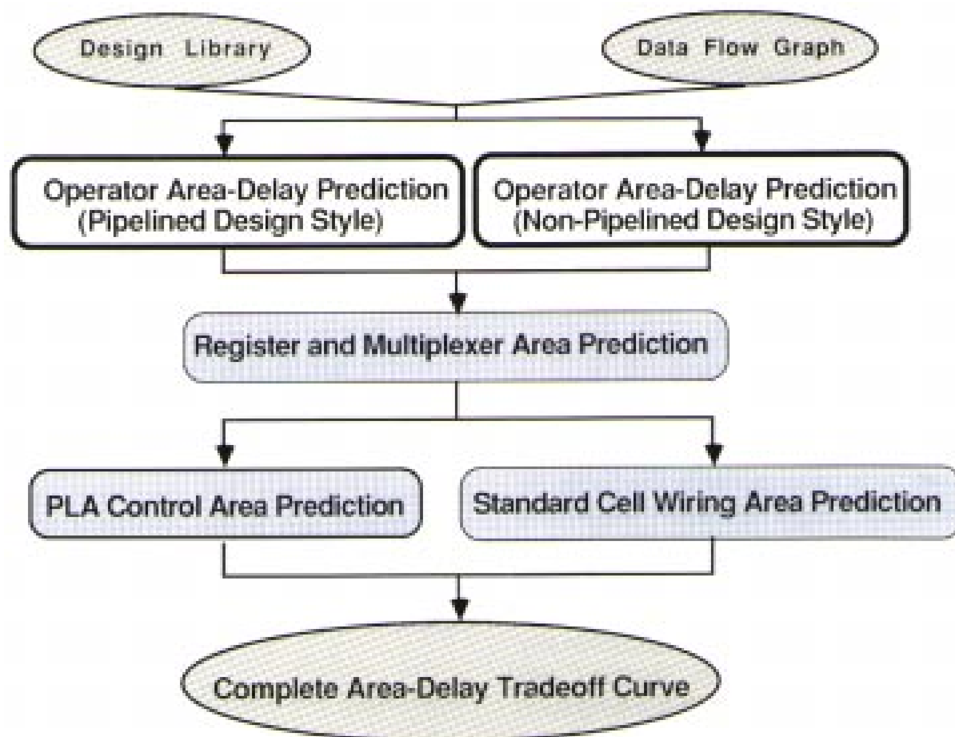
The ADAM Synthesis System

The ADAM Synthesis System assists designers in producing digital systems from high-level specifications. ADAM provides tools and techniques to predict the resultant cost and performance of digital designs, given information on their required behavior.

The operator (functional unit) costs and delays are predicted first, followed by the costs of registers, multiplexers, control, and wiring. The predictions are combined to form an overall area-delay tradeoff curve for each design under consideration.

The prediction theories form the basis for design style selection, module selection, and high-level transformations in the ADAM system. These packages also can be used to measure the quality of synthesis programs by comparing the outcome with the predictions.

Professor Alice C. Parker
University of Southern California



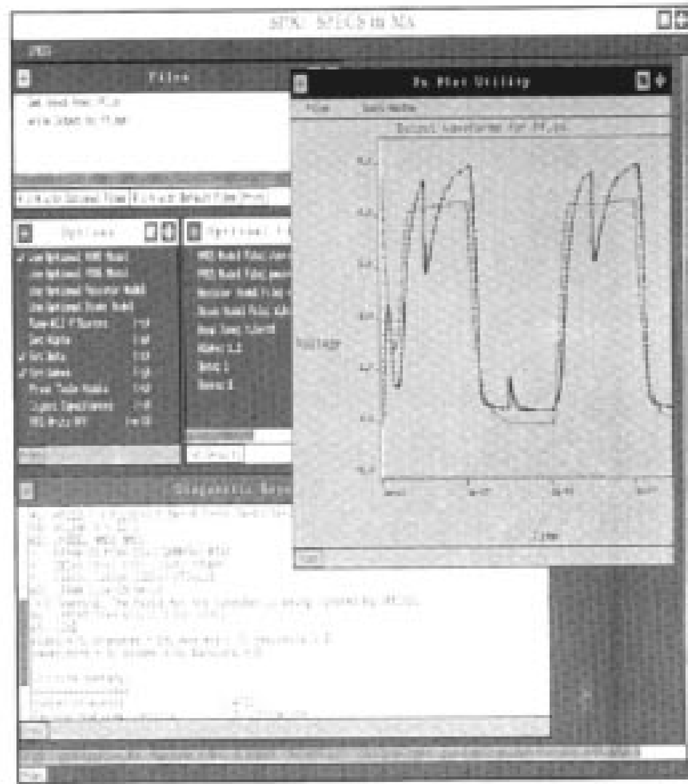
High-Level Synthesis Predictors in the ADAM System

Design verification, principally simulation, has been challenged by the explosion in IC complexity. The number of logic gates available in an integrated circuit currently doubles in a two- to three-year period. Commercial ICs with over a million transistors are available. SRC-sponsored research addresses this complexity issue with research in three areas: creation of highly efficient simulation algorithms, use of parallel processors, and development of hierarchical mixed-mode simulators.

Highly efficient simulation algorithms are the goal of the COSMOS project at Carnegie-Mellon University and the XPSim project at the University of California at Berkeley. COSMOS is a unit delay switch-level simulator at least ten times faster than its widely used predecessor, MOSSIM. The COSMOS project also investigates the use of symbolic formal verification techniques and the extension to a time-based resistive/capacitive simulation. The XPSim project has improved the performance of circuit-level simulation through the use of exponential waveforms.

Research on the use of parallel processors to improve simulation times is underway at Carnegie-Mellon in the COSMOS project, at the University of Illinois in wave relaxation algorithms, and at Berkeley in circuit simulation.

Mixed-level simulation improves efficiency by the partial transference of circuit complexity into higher-level models. At Berkeley, CODECS bridges the gap between device and circuit simulation; and at Carnegie-Mellon, SPECS bridges between circuit-level and logic-level simulation.



Simulation Program for Electronic Circuits and Systems

Circuit Simulation with SPECS

The escalating complexity of VLSI designs poses an acute need for a reliable and efficient transient simulator that can provide more detailed waveform and timing information than switch and gate level logic simulators. SPECS (Simulation Program for Electronic Circuits and Systems) is a piecewise-approximate transient simulator that fills the void between traditional circuit and logic simulation.

SPECS allows the user to trade efficiency for accuracy on both local and global bases by varying the modeling resolution. Thus CPU time may be better distributed with respect to critical portions of circuits and critical simulation runs. Macromodeling, a higher level of modeling abstraction, is being incorporated in order to provide mixed-mode simulation capabilities. SPECS now provides inexpensive computation of time domain sensitivities. SPECS has been benchmarked in an industrial environment on production circuits of more than 1500 MOS transistors. On progressively larger circuits, the CPU performance increased to two orders of magnitude faster than a traditional nonlinear circuit simulator, while maintaining reasonable accuracy.

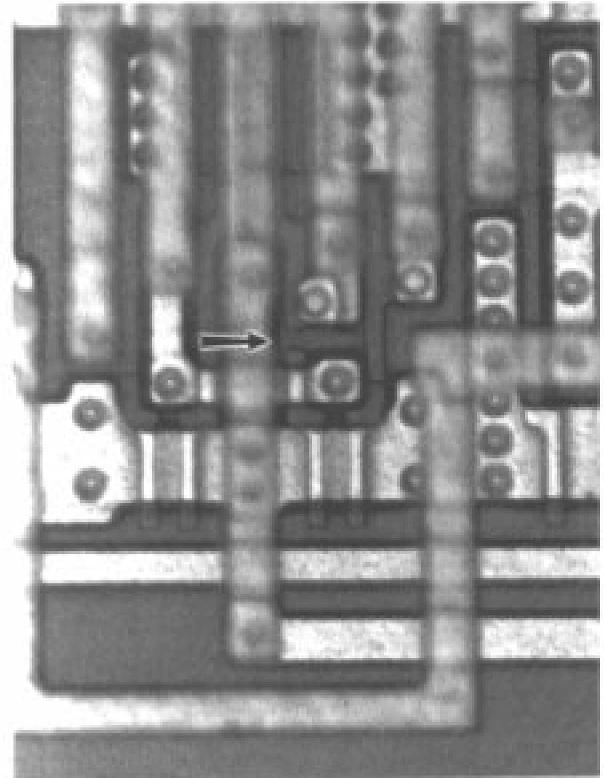
Ongoing research includes the efficient analysis of stiff systems, the incorporation of bipolar transistors and nonlinear capacitors, applications of transient sensitivity, and extension of macromodels as diagnostic aids to design verification.

Professor Ronald A. Rohrer
Carnegie-Mellon University

The goal of design for test is the efficient, high coverage test of ICs with minimal or no impact on area, performance, or design time. The two SRC research goals of an electrical reject ratio after final IC testing of 1 to 1,000,000 and a design time of six person-months has placed considerable emphasis on automatic synthesis with design for test.

Research is underway at the University of California at Berkeley on synthesis of testable combinational and sequential logic structures. Emphasis is on the automatic synthesis and testability of electronic systems from high level descriptions and on generation of minimal-sized test vector sets.

The University of Texas at Austin is developing design techniques and tools to incorporate testability into designs produced by synthesis systems and test vectors for those designs. It will address hierarchical fault simulation, automatic test pattern generation, and new approaches to relate the level of testing effort to defect levels.



Layout of a segment of an IC with artificially created defect (an open) which was used during the performance evaluation of the 18-transistor BIC sensor implemented on the same chip.

Built-In Current Testing

Research at CMU indicates that significant improvement can be achieved in the efficiency of current testing to detect abnormalities in integrated circuits by using Built-In Current (BIC) sensors instead of off-chip current measurements. To investigate the feasibility of BIC testing, prototype CMOS circuits have been built and issues have been analyzed, such as quality of BIC testing (characterized in terms of defect detectability) and optimal design of BIC sensors to provide maximum defect detectability and speed of testing with minimal area overhead. A spectrum of possible applications of BIC testing has also been investigated.

Results obtained suggest that BIC testing is a very attractive technique. It supplements standard testing techniques by the ability to detect otherwise undetectable or difficult-to-detect defects (e.g., timing defects due to opens) and can have a speed approaching that of an IC under test (orders of magnitude faster than off-chip current testing). It is also very attractive from the test generation point of view (no observability limits).

BIC testing also has a number of uniquely attractive applications. One is reliability-oriented passive testing. Such testing performed concurrently with the normal operation of an IC may provide an “early warning” about failures before an actual IC malfunction occurs.

Professor Wojciech Maly
Carnegie-Mellon University

Hierarchical Fault Simulator and Test Pattern Generator

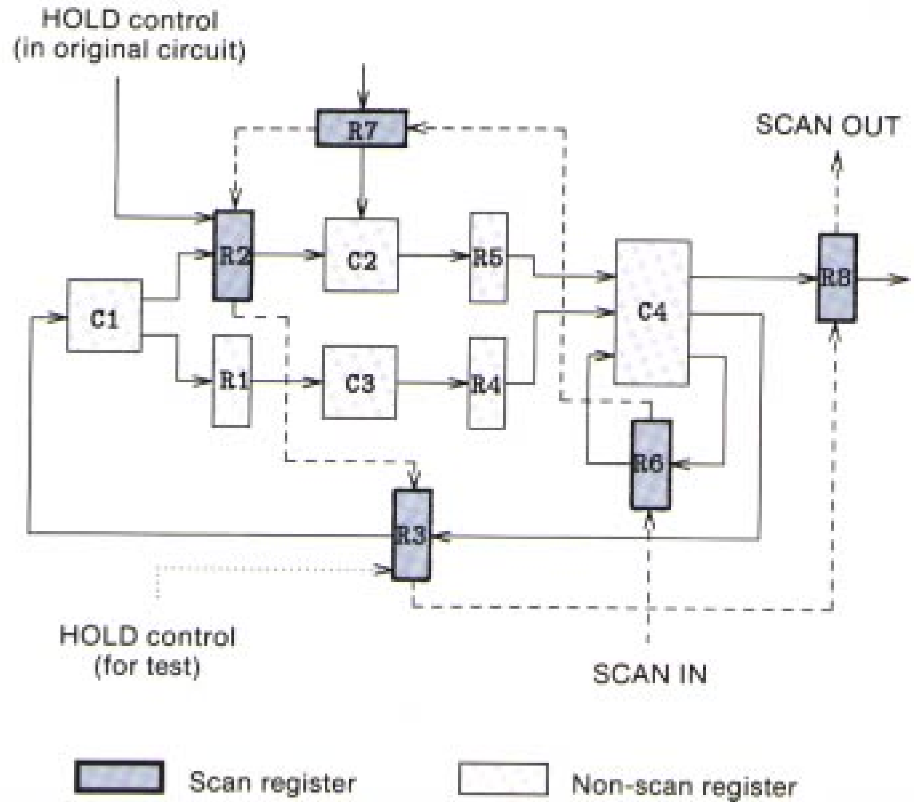
A new hierarchical switch-level logic and fault simulator, CHAMP, has been developed. The program is written in C and runs on a Sun workstation. CHAMP simulates directly from the hierarchical circuit description by exploiting the hierarchy to reduce memory requirements. The program performs mixed-mode simulation: parts of the circuit can be simulated faster at a behavioral level by supplying a high-level software description.

CHAMP allows assignable delays and bidirectional signal flow inside circuit blocks, which are represented as transistor networks, as well as across the boundaries of high-level blocks. The program models both stuck-at and transistor faults, giving accurate and meaningful results. CHAMP has been used to fault simulate a switch-level model of a commercially available microprocessor on a Sun4 workstation. The circuit is described as a mixture of gates (given as transistor networks) and pass transistors.

The companion program HITEC, a hierarchical test pattern generator, uses the high-level structures present in the design without flattening them to the gate-level primitives. The high-level structures can be described as interconnection of lower-level structures. The Boolean and behavioral descriptions in CHAMP and HITEC allow the test generation to proceed early in the design cycle to help identify potential testability problems and reduce design time.

Professors Janak H. Patel
and Daniel G. Saab
University of Illinois at Urbana-Champaign

BALLAST Implementation



The BALLAST Partial Scan Methodology

BALLAST is a new partial scan design methodology that achieves reduction in the logic overhead required in full-scan designs without any increase in the difficulty of testing. As in full-scan design techniques, test patterns can be generated with BALLAST using purely combinational test pattern generation techniques; and 100% coverage of detectable faults in the combinational logic can be achieved. This ease of testing arises from the manner in which the scan path is constructed.

The storage elements to be included in the scan path are selected such that the remainder of the circuit belongs to a well-defined class of circuits called balanced sequential structures (B-structures). Circuits in this class have certain desirable testability properties. Any arbitrary sequential circuit can be converted into a B-structure by excluding some subset of its storage elements. BALLAST determines the smallest such subset of storage elements and connects them into a scan path. Some scan path storage elements may need to be provided with a HOLD mode. A complete set of test patterns for a circuit designed using BALLAST can be obtained by carrying out test pattern generation on a *combination equivalent* derived from the circuit. A special test procedure is used in which dummy bits are introduced into each input test pattern. Using this methodology, BALLAST achieves its objectives of high fault coverage and ease of test generation with a minimal logic overhead.

Professor Melvin A. Breuer
University of Southern California

Research: Physical Design

Physical design of integrated circuits is challenged by the threefold constraints of area, power dissipation, and performance. Current physical design research can be divided into two groups: automatic placement/routing and logic module generation.

Automatic placement/routing projects at the University of California at Berkeley include sea-of-gates or channelless gate array design (ORCA) and standard cell design (MOSAICO and BEAR). Researchers at the University of Illinois are investigating an evolution-based placement analogous to the natural selection process in biological systems. And at Yale, the TIMBERWOLF family of gate-array and standard cell placement-and-routing tools is being extended to analog and digital logic systems.

In the automatic generation of CMOS process-independent logic modules, Berkeley researchers are working on the TOPOGEN project.

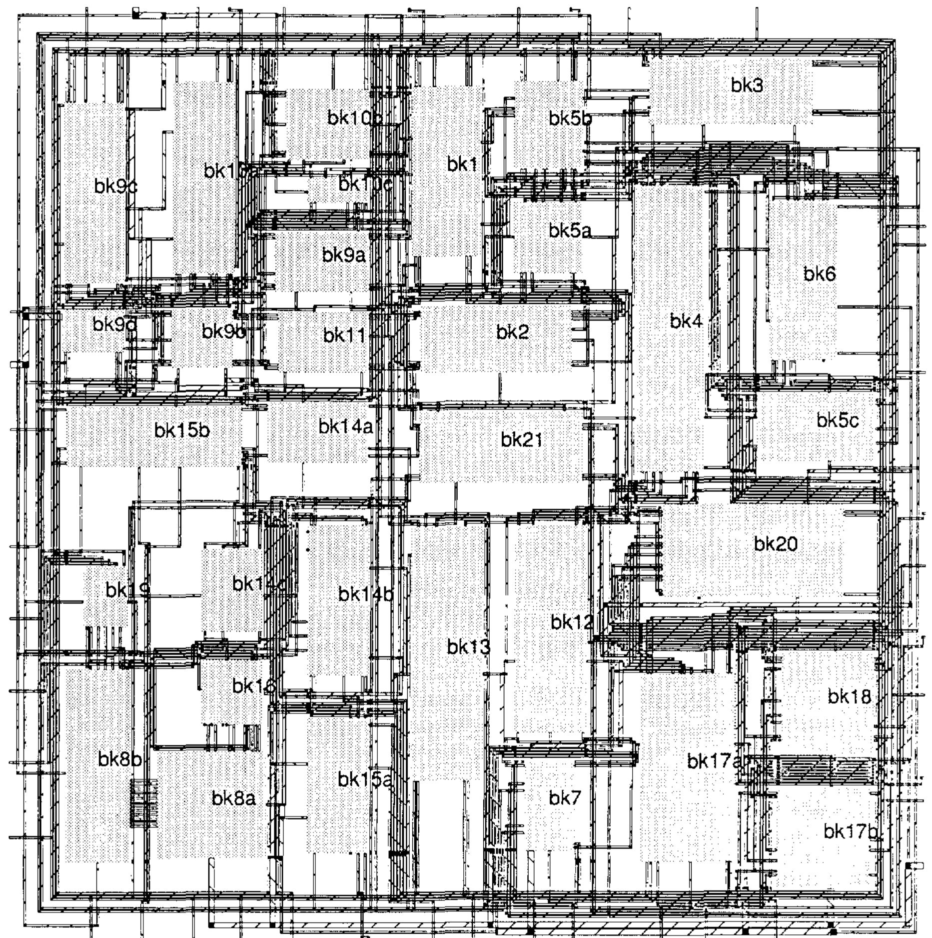
The difficulties of both automatic placement/routing and logic module generation are fused together in datapath synthesis. Issues relating to datapath structures, which have the interconnection wires embedded within the logic modules, are being addressed by the LASSIE project at Carnegie-Mellon.

BEAR Layout System

BEAR (Building-block Environment Allocation and Routing system) is a second-generation, macrocell-based layout system. The goal of the system is to lay out a chip in both a top-down and bottom-up physical design environment. BEAR includes a new scheme for achieving feasible routing order in a non-slicing structured placement, unified topological and geometrical representations, and efficient methods to update topological (global routing) information after geometrical operations (block movement) have been developed.

The BEAR system is being developed in the C language using the X-Window manager with 4.3 BSD UNIX. The primary input and output is EDIF (also CIF). BEAR is being interfaced with other Berkeley CAD tools via the VEM/OCT CAD framework.

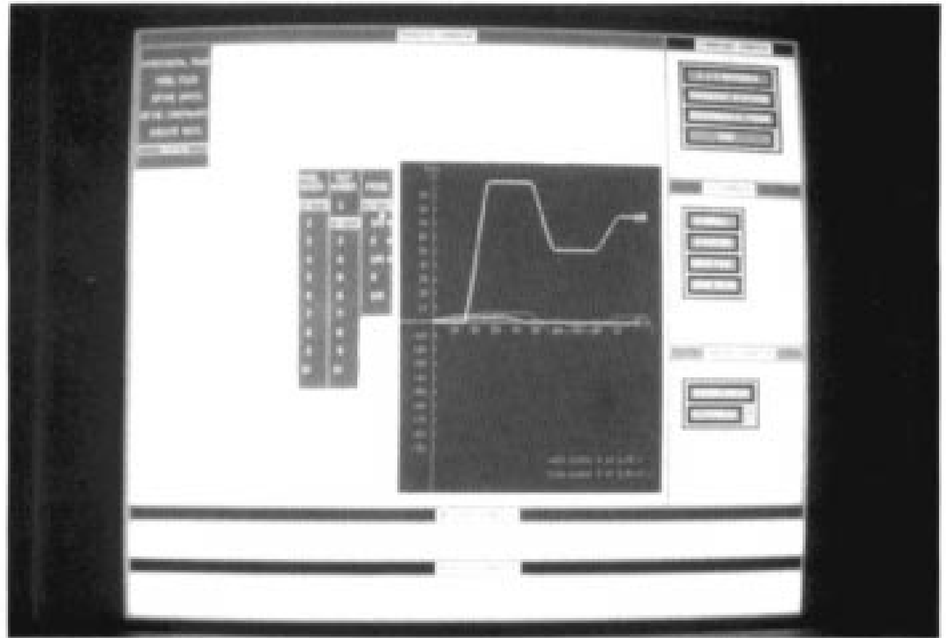
Professor Ernest S. Kuh
University of California at Berkeley



A Sample BEAR Macrocell Layout

During 1987 and 1988, increases in chip functionality have resulted in ICs with much lower cost per function and a 500% increase in electrical performance as measured by the speed of operation of the chip. So much progress has been made in chip performance that packaging and interconnections have become pacing research areas for high performance IC systems. Interactive designs for chip and package are imperative for optimum system performance. SRC packaging research addresses many of the critical industry needs for next-generation ICs, including: simulation and modeling for the package as a system element, packaging material systems that provide reliability without hermeticity, optimum power distribution systems that adequately handle large currents, high-capacity heat transfer techniques, and low-cost multichip packaging methods.

Research is being conducted by six university groups at Arizona, Auburn, Cornell, Lehigh, Purdue, and Stanford, with research projects ranging from materials characterization to the development of CAD tools for package design. Arizona research is bringing packaging CAD more in line with techniques that have been developed for the integrated circuit chip. Auburn is developing a methodology for evaluating package reliability. Cornell and Lehigh are covering both materials and performance aspects of densely packed designs. At Purdue, emphasis is on building an accurate database of important materials used in packaging. Research at Stanford focuses on using silicon substrates for high-performance interconnections.



Packaging Design Support Environment

Packaging CAD: Design Support Environment

Packaging Design Support Environment (PDSE) is a software shell integrating simulation tools for prediction of electrical characteristics of IC packaging structures. Currently, parameter extractor tools and a transient waveform simulator are available. PDSE runs under UNIX and X Windows on a DEC VAXstation GPX-II. In a typical simulation session, the user communicates with the shell through a menu-driven, graphics interface and selects the type of analysis to be performed (e.g., parameter extraction or transient analysis). If models for the selected simulation type are available, they are retrieved from the model base, and a simulation run is automatically initiated. Results can be displayed in a graphical form and stored for future reference. PDSE facilitates interactive specification and editing of circuit models. Graphic display of conductor geometry is provided.

During 1988, development focused on automatic coordination of simulation modules. The user specifies the desired objectives of the simulation (e.g., the computation of capacitance and inductance matrices). PDSE then suggests the appropriate tool, and a relevant menu window is displayed for interactive entry of parameters. In simulating transient response, the system automatically verifies that both capacitance and inductance matrices are available for input to the simulator. If these matrices are not available, parameter calculators are invoked to compute them and route them to the waveform simulator module. Work in progress concerns the separation of models and experiments to give users broad flexibility for evaluating a class of models within the same experimental setup, or, conversely, the same model within a class of different experiments.

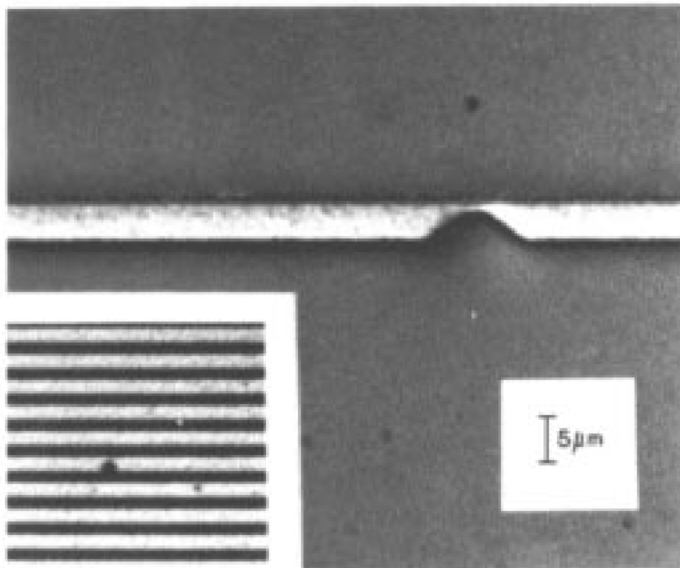
Professor John L. Prince III
University of Arizona

Integrated circuit reliability is a high priority concern from the initial design through the fabrication and testing stages, SRC reliability research extends from design for reliability to device and phenomena studies with the goal of providing the knowledge and tools required to predict circuit reliability *in the design phase,* given the layout and process information.

Three reliability related phenomena — oxide wearout (including hot-electron effects), electrostatic discharge damage, and electromigration of circuit interconnects — are being investigated and the results incorporated into design software at Clemson University. Additional electromigration research is being performed at Cornell and the University of South Florida.

Another major reliability concern is degradation in thin insulating films subjected to high electric fields and/or hot electron impacts. This failure mode is increasingly important in the thinner films of submicron ICs. Fundamental atomic-level studies of trap formation and annealing are being conducted at Yale University, Rensselaer Polytechnic Institute, and the University of Illinois; and modeling of the circuit effects of the resultant oxide defects is the subject of research at both Cornell and the University of California at Berkeley. As with the electromigration research, the ultimate objective is to develop sufficiently accurate models to allow the prediction of circuit reliablity in the circuit design phase.

Examples of recent results are described on these pages.

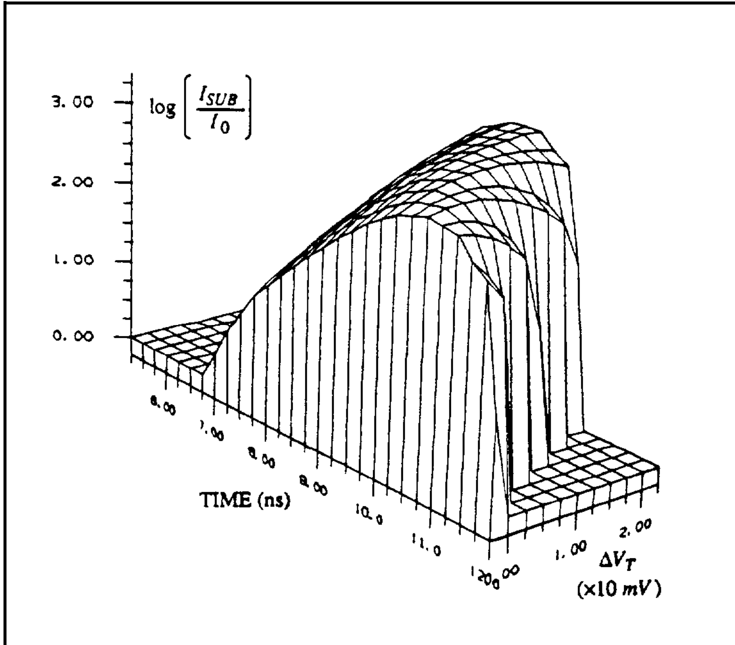


A portion of an intentionally defected metal line that will be subjected to accelerated testing to determine its electromigration failure characteristics. Inset is a photograph of the metallization pattern of a commercialchip in which one of the lines has a similar, but unintentional, defect.

Prediction of Early Failures in the Metal Interconnect System of VLSI Devices

The RELIANT computer program extracts current density information from circuit design, and predicts electromigration failure rates based on a model for this failure mechanism. In addition to the inherent electromigration failures, arising from the conductor structure and composition, early failures occur due to process defects in the conductors. To support the development of a model for these failures to be added to RELIANT in the CAD reliability suite, the effects of intentionally introduced defects on metallization failure rates are being studied. The test structures shown have been fabricated in Clemson's new Microstructures Laboratory which was built with funds appropriated by the State of South Carolina, in large measure because of SRC's support of the VLSI Reliability Research Program at Clemson University.

Professor James W. Harrison, Jr.
Clemson University



Simulator output showing the way in which the substrate current waveforms change as the device parameters degrade in a CMOS differential sense amplifier circuit.

Hot-Carrier Induced Circuit Performance Degradation

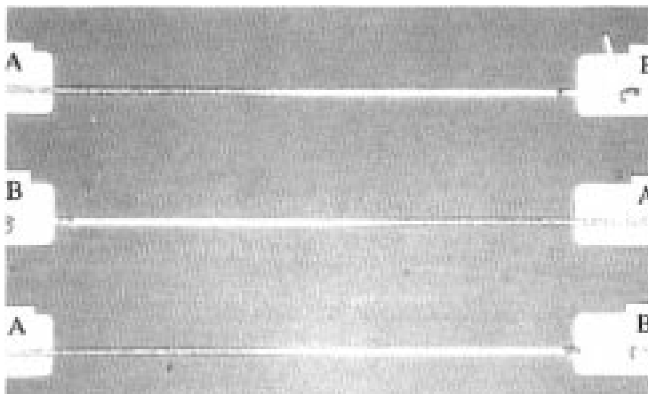
Effects of hot-electron degradation on circuit performance are being studied and modeled. A reliability simulator has been developed to estimate the hot-electron-related device parameter degradation in MOS circuits. It uses a novel degradation model that has been proposed to account for the localized charge deposition near the drain end of the MOS device channel. As the degradation depends strongly on the configuration and operating conditions of the circuit, the sensitivity of each circuit to the device degradation parameters must be determined and included in the model.

Professor S.M. Kang
University of Illinois at Urbana-Champaign

Molecular Dynamics Simulation of Grain Boundary Diffusion in Metals

The Cornell National Supercomputer Facility (CNSF) enables detailed, atomic level, calculations of the diffusion of Al at grain boundaries and the effects of adding Cu “dopant” — which is known experimentally to significantly inhibit electromigration degradation. The results of these simulations are being compared with experimentally determined electromigration parameters and the model iteratively refined to match the real world. The effects of electromigration can be dramatic as shown in the accompanying optical micrographs.

Professor Edward D. Wolf
Cornell University



An optical micrograph of P-micrometer-wide aluminum lines running between larger contacts on a semiconductor substrate. The Al lines were stressed at a current density of 106 amps/cm^2 at 200°C for two days. Extensive electromigration damage is evident. Electron flow in each line was from A to B. At the B side is a large pileup of Al; the top line, in particular, shows a whisker growth extending several micrometers away from the line. In a real IC, if this were to contact an adjacent line, a “short” would occur, and the chip would likely fail. By contrast, the A side of each line is partially depleted of Al along nearly half the line length.

Scanning electron micrograph of the B end of a typical line showing the piled-up hillocks of Al. The hillocks are approximately 2 μm high.

Research: MMEE Curricula Development

The initiative in Microelectronic Manufacturing Engineering Education (MMEE) matured during 1988 into a fully fledged program at five of the country's leading engineering academic institutions.

Building on the pilot program for development of interdisciplinary curricula begun in 1986 at Florida A&M University/Florida State University (FAMU/FSU), additional grants were awarded in 1988 to the University of Minnesota, Rensselear Polytechnic Institute, Rochester Institute of Technology, and the University of Texas at Austin to develop an overall educational effort with a wealth of diversity. Each of the five schools has built on its unique strengths to develop graduate and undergraduate course curricula to educate students for careers in microelectronic manufacturing.

Photo Courtesy of the Rochester Institute of Technology

Four of the programs are aimed primarily at the master's level, with emphasis this first year on expanding the scope of course offerings to include such topics as Yield Management in Microelectronics, Microelectronic Manufacturing Science, Statistical Quality Control, and Semiconductor Processing Operations. The Minnesota program is aimed primarily at the undergraduate level, and new course developments include Materials Science and Clean Room Technology. The master's program at both Rensselear and Rochester have been largely populated by employees of member companies who are preparing for new job assignments in IC manufacturing.

The experience of some of the persons who have returned to academia after being away from the classroom for several years suggests the need for some additional preparation to keep abreast of changing technology and manufacturing processes. These and other lessons from this first full year of the MMEE program have indicated directions for extension of the program in the coming year.

Recruiting top-notch students into these new curricula will continue to be one of the critical facets of the program. As these programs continue to develop, it is anticipated that they will become of increasing value to the semiconductor industry — both as a source of new, suitably trained graduates and as a vehicle for the continuing education of member company employees in the manufacturing disciplines.

TAB and UAC

The Technical Advisory Board (TAB) of the SRC provides essential guidance on goals, priorities, relevance, and strategies for the research program, and coordinates the transfer of research technology to potential users of the results. It consists of technical representatives of members and participants and corresponds to the SRC's program structure.

The University Advisory Committee (UAC) provides insights that assist the SRC in managing and directing its activities. The committee consists of faculty members from research universities.

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**Through August 1988

ABOUT THE COVER: Photograph appearing on the outside/inside front cover is of an Applied Materials hex RIE that is one of several dry etch tools in the University of Michigan Solid-State Fabrication Facility being used with an adaptive sensor-driven, closed-loop controller to extend tool performance in submicron pattern transfer (see Fourier Imaging highlight on page 21). Diagram across the top of the outside front/back cover is a MOSFET-C Universal Filter Structure developed at Ohio State University (see highlight on page 28).

The Annual Report of the Semiconductor Research Corporation is published each June to summarize the directions and results of the SRC Research Program, present the formal financial report, and provide information on activities and events of the SRC industry/government/university community for the previous calendar year. The highlight material contained in the research section and most of the illustrations used in this publication are provided by the faculty and graduate students conducting SRC-sponsored research. The remaining text is written by the technical staff of the SRC. Production is guided by the SRC's Editorial Coordinator, Marian Regan.

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