
# Semiconductor Research Corporation

SRC
COOPERATIVE RESEARCH

1990 Annual Report

### *Poster Sessions*

***Posters depicting results generated from SRC-sponsored research are prepared by graduate students to enhance their presentations at SRC events. The poster sessions foster camaraderie and enthusiastic dialogue between the students and their audience of industry/government scientists and engineers.***

***On the left in the upper photograph, Robert Molyneaux is describing research at the University of Rochester. In the center of the lower photo-graph, Alan Mantooth is describing his project at the Georgia Institute of Technology.***

# *Semiconductor Research Corporation*

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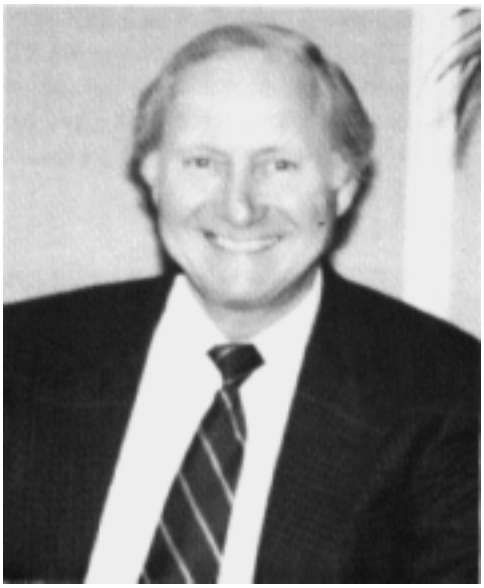
*The Semiconductor Research Corporation (SRC) plans and implements a program of applied research at leading U.S. universities to strengthen the competitive ability of the U.S. semiconductor industry.*

*Its mission is to:*

- *Identify the scientific and technology needs of the industry, develop a long-range strategy for meeting those needs, and carry out research that implements that strategy.*
- *Enhance the semiconductor industry's manpower resources.*
- *Disseminate information and transfer technology from the research program to SRC members on a priority basis.*
- *Increase cooperation, provide technology leadership, and advance and support competitive responses.*

***Contents***



*Dr. Schwettmann*

*Mr. Sumney*

# *Executive Message*

COOPERATIVE RESEARCH

*Since its formation in 1982, the Semiconductor Research Corporation has pioneered cooperation in semiconductor technology at the research end of the technology chain. Today, the SRC is well positioned to continue its contributions to the competitiveness of the U.S. semiconductor industry.*

*Following the early success of the SRC, other cooperative ventures addressing technology needs were created and new programs are being discussed. As the value of cooperation becomes more and more apparent, we will continue to examine the means by which we can increase our effectiveness as an important part of these broader cooperative activities.*

*In 1990, the SRC had more than 100 contracts with 60 research organizations that supported approximately 250 faculty members and 700 graduate students. Every year, many of these students complete their graduate education and, having an excellent background in silicon microelectronics, join the manpower base of the U.S. semiconductor industry. During the year, the program generated 897 research reports and a variety of intellectual property, including 8 U.S. patents issued and 22 invention disclosures.*

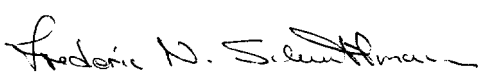
*Our second general research conference, TECHCON '90, gave more than 550 attendees a look at both the best results of the SRC Research Program and the technologies that will affect the semiconductor industry and the program in the future.*

*The long-range research goals, originally written for the year 1994, have been extended to the year 2001. This new goal set is now being used to define the SRC Research Program. The SRC is charged by its members with developing the long-range research strategy for the U.S. semiconductor industry, and the research goals were developed through an extensive planning process involving hundreds of people from our member companies and participating government agencies.*

*The SRC's membership base continues to expand. The number of small companies participating in the research program as Affiliate Members more than doubled in 1990, and two national laboratories, Sandia and Los Alamos, became Associate Members. In a significant change in policy, the SRC opened membership opportunities to Canadian companies for the first time.*

*This Annual Report provides a picture of our cooperative program in 1990. As part of this report, we particularly want to thank the people from industry and government — some 700, in all — who served as members of the committees of our Technical Advisory Board and as mentors for individual research tasks. in large measure, the success of the SRC reflects their efforts.*

*Frederic N. Schwettmann*



*Chairman of the Board*

*Larry W. Sumney*

*President*

***TECHCON '90***

***The photo above is an overhead view of the poster displays at the Technology Fair of TECHCON '90, the SRC's second community-wide conference that was held in San Jose, California, for three days in October.***

***Conference activities opened with a Plenary Session featuring leaders from industry, government, and academia who called for changes in the trends that show a decline in the posture of the United States relative to international technological leadership. During seventeen technical sessions, SK-funded researchers presented 99 papers describing their projects. A Technology Fair, including more than 100 poster sessions and software demonstrations that were prepared and conducted by SRC-funded graduate students, afforded the opportunity for one-on-one dialogue between the students and industry/government attendees. Eight invited papers given by industry scientists and engineers addressed future research directions and challenges.***

***TECHCON '90 surpassed TECHCON '88 in stimulating interactive communication among the more than 550 participants. The exchange of ideas continued during breaks between sessions, as shown in the picture on the facing page.***

# *Mission*

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# *The Cooperative Research Mission*

*In nine years, the mission of the SRC has not changed, although it is often expressed in different ways and with different emphasis:*

*... generic research in semiconductors,*

*... manpower with relevant skills,*

*… technology competitiveness*

*In whatever way the mission is described, it has been so successful that the expectations to which the SRC must respond have expanded.*

*in silicon-device-related research in universities, the SRC's efforts have rebuilt a strong community of researchers. This accomplished, the effectiveness of this community must now be increased. The SRC must be the source of knowledge that helps industry meet its more immediate needs and also serve the longer range imperative of providing the knowledge and discoveries that will enable the U.S. semiconductor industry to lead the world a decade in the future.*

*This is a demanding challenge that requires radical changes in the research establishment. The SRC must search for the means to catalyze the required changes, recognizing that this requires cooperation with the many organizations participating in this mission.*

# Technology Competitiveness

*The SRC's focus is on research and education, and these are important to the third leg of the mission: technology competitiveness. Technology competitiveness is much more than just a research and education issue. Its achievement requires more in the way of resources and capabilities than the SRC or any other single organization can muster. For this reason, the SRC agenda includes cooperating with other organizations and with the federal government and seizing opportunities as they occur to promote the cause of semiconductor technology competitiveness.*

*To this end, the SRC has ties and working relationships with industry associations and consortia, with government and national laboratories, and with committees and councils concerned with technology and competitiveness. During 1990, the SRC participated in the new Technology Committee of the Semiconductor Industry Association, supported the planning effort of the National Advisory Committee on Semiconductors for a long-range national technology initiative known as Micro Tech 2000, established closer ties with two of the Department of Energy's national laboratories, and became more closely integrated with the SEMATECH and MCC consortia.*

*The SRC Competitiveness Foundation, formed by the SRC in 1988, continued to expand its education agenda. Both the Graduate Fellowship Program and the Microelectronics Manufacturing Engineering Education curricula development program, which were developed by the SRC, were transferred to the Foundation early in 1990. In addition, the Foundation's innovative summer program for high school math and science teachers grew from a pilot program in 1989 to successful projects at three sites*

***Robert M. Burger***
***Vice President***
***and Chief Scientist***

*in 1990. The importance of education at ail levels to the competitiveness of the semiconductor industry dictates the continuing close coordination of the program, resources, and people associated with both the SRC and the Foundation.*

*The challenge to the semiconductor research community of the United States continues. The members of this community must continue to evolve from competing among themselves for limited resources to joining together to address common goals that support the nation's best interests. The SRC accepts this challenge.*

# *Toward 2001*

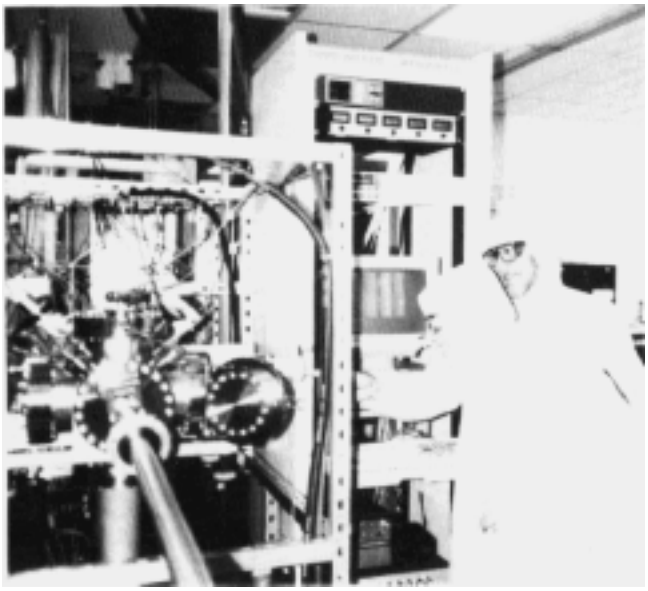
*Ten years ago, forecasts did not prepare us for the workstation-on-a-chip, one-half micrometer optical lithography, trench technology, or prospects of a billion-dollar fab. Yet all of these are with us today. As we move along our current trend lines, we must be constantly aware that a majority of significant advances follow from deviations from the trend, which some call paradigm shifts.*

*Many of the most successful industry products have resulted from bootlegged projects as opposed to those that survived the endless round of reviews and second guessing built into the system. Nowhere is the pressure to avoid high-risk projects greater than in a cooperative research environment when decisions are made by consensus.*

*Looking to the future, the greatest challenge to the SRC is to provide sufficient direction to its research to maintain relevance while providing sufficient freedom to encourage exploration off the trend line. By doing this we may find how to get information into and out of single atom memory cells, to convert electron energy to photons controllably and efficiently, to fabricate the programmable interconnection substrate on which to applique our active chips, or to design systems that are not replications of 50-year-old relay logic.*

*In ten years, we almost surely will have rapid keyboard access to everything we need to know — at least about semiconductors — and will be free to do more creative work instead of literature searches. And probably we will have a less-costly way of making chips, a/though we must recognize the probability of limits beyond which the costs of greater complexity exceed the benefits of further integration.*

*Today, as it has every year since it was founded, the SRC is changing its research agenda in response to semiconductor progress and the search for the more ideal. It is seeking to provide sufficient utilizable product to maintain short-range viability while exploring the frontiers of knowledge for the paradigm shifts — and all the while remaining very much aware that the momentum of an enormous industry makes changes very difficult.*



### *Members as Mentors*

***In 1990, nearly 500 scientists and engineers who work for companies belonging to the SRC participated in the cooperative research program as Industrial Mentors. Mentors establish direct contact with the faculty and students who carry out SRC research. They contribute guidance, expertise, and resources to the research effort and transport new technology generated by the universities to practical applications in industry.***

***Shown above with rapid thermal processing equipment at North Carolina State University are SRC Mentor David Abercrombie of Harris Corporation (foreground) and Professor J.J. Wortman, an SRC contract Principal Investigator. Mr. Abercrombie, who recently received an SRC Outstanding Mentor Award, first became involved with SRC research as a graduate student. When joining the Harris staff, he was enthusiastic about continuing his association with SRC research through the mentor program. He describes mentoring as being personally and professionally rewarding, of major benefit to his company, and of critical importance to the overall success of the SRC.***

# *Industry Members and Government Participants*

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## Members

AT&T
Advanced Micro Devices, Inc.
Alcoa
Control Data Corporation
Digital Equipment Corporation
E.I. du Pont de Nemours & Company
E-Systems, Incorporated
Eastman Kodak Company
Eaton Corporation
Etec Systems, Inc.
General Electric Company
General Motors Corporation
Harris Corporation
Hewlett-Packard Company
Honeywell Incorpora ted
IBM Corporation
lntel Corporation
LSI Logic Corporation
Micron Technology, Inc.
Motorola, Incorporated
NCR Corporation
National Semiconductor Corporation
Rockwell International Corporation
Texas Instruments Incorporated
Union Carbide Corporation
Varian Associates, Incorpora ted
Westinghouse Electric Corporation
Xerox Corporation

## Associate Members

Los Alamos National Laboratory
Microelectronics and Computer Technology Corporation (MCC)
Sandia National Laboratories
SEMATECH, Incorporated

## Affiliate Members

Advanced Technology Applications, Inc.
Analogy Inc.
Dawn Technologies, Inc.
Epic Design Technology, Inc.
Hestia Corporation
lntegrated Silicon Systems, Inc.
Intersonics, Incorporated
Jamar Technology Co.
Mission Research Corporation
nChip, Inc.
Peak Systems, Incorporated
QuanScan, Inc.
Rapro Technology Inc.
Sienna Technologies Inc.
SlLVACO Data Systems
Solid State Equipment Corporation
Technology Modeling Associates, Inc.
Techware Systems Corporation
Tyecin Systems Inc.
Unit Instruments, Inc.
WYKO Corporation
XMR Inc.

## Participating U.S. Government Agencies

Defense Nuclear Agency (DNA)
National Institute of Standards and Technology (NIST)
National Science Foundation (NSF)
National Security Agency (NSA)
Office of Naval Technology (ONT)
Wright Laboratory

***Research Reviews***

***The SRC had more than 700 contracts with research organizations in 1990. The studies being performed under these contracts included approximately 250 research tasks. Contract renewal is contingent upon the results of annual research assessments performed by SRC corporate staff and the industrylgovernment representatives who make up the committees of the Technical Advisory Board. For efficiency and cost-effectiveness, the SRC has been holding an increasing number of multiple-contract reviews. The photo above shows a review team at MIT as they were assessing research results presented by faculty and graduate students from several single-task and multiple-task contracts.***

# *Corporate Development and Government Relations*

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## Membership

*Semiconductor industry organizations based in the United States and Canada can join the SRC in one of three categories: Members, Associate Members, and Affiliate Members.*

*Members are semiconductor manufacturers and users with semiconductor-related sales greater than $30-million/year. The number of Members has grown from 11 founding companies in 1982 to 28 companies in 1990, including almost all of the largest manufacturers and users.*

*Associate Members are organizations that participate in semiconductor R&D but do not have a product for sale.*

*Affiliate Members are small companies that manufacture or supply equipment, materials, and software to the industry.*

*In 1990, seven teen organizations joined the SRC: two Members (Alcoa and Etec Systems), two Associate Members (Sandia National Laboratories and Los Alamos National Laboratory) and 13 Affiliate Members (Advanced Technology Applications, Analogy, Hestia, Integrated Silicon Systems, Intersonics, Jamar Technology, Mission Research, nChip, QuanScan, Sienna Technologies, Techware Systems, Tyecin Systems, and WYKO). Affiliate membership reached an all-time high this year.*

*The working body through which member organizations and participating government agencies influence the direction of SRC research is the SRC Technical Advisory Board (TAB).*

***D. Howard Phillips***
***Senior Director,***
***Corporate Development and Government Relations***

## Government Relations

*U.S. Government organizations have participated in the SRC since 1986 through a Memorandum of Understanding between the SRC and the National Science Foundation.*

*A Government Coordinating Committee (GCC) serves as an advisory body to the SRC Board of Directors. Members of this committee include, but are not limited to, the federal agencies that fund SRC research.*

### Government Coordinating Committee

| | |
|---|---|
| ***Chairperson:*** | |
| *K. Speierman* | *National Security Agency* |
| ***Secretary:*** | |
| *Richard D. LaScala* | *SRC* |
| *Ray M. Bowen* | *National Science Foundation* |
| *Robert M. Burger* | *SRC* |
| *Edwin B. Champagne* | *Wright Laboratory* |
| *Lewis M. Cohn* | *Defense Nuclear Agency* |
| *William J. Edwards* | *Wright Laboratory* |
| *C. Edward Ho//and, Jr.* | *SRC* |
| *Harold L. Hughes* | *Naval Research Laboratory* |
| *Norman Kreisman* | *U.S. Department of Energy* |
| *Frank F. Oettinger* | *N/ST* |
| *D. Howard Philips* | *SRC* |

### *Technology Exchange*

***The SRC Research Program fosters inter-departmental and interdisciplinary cooperative research within universities and provides opportunities for researchers to meet with their off-campus colleagues from other research organizations. In the photo above (left to right), Professors J.J. Wortman of NC State, A.F. Tasch of Texas at Austin, and J.D. Plummer of Stanford are sharing an informal discussion at an SRC event on the Stanford campus.***

# *Research Organizations*

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# Research Organizations

*University of Arizona*
*Arizona State University*
*Auburn University*
*Boston University*
*University of California at Berkeley*
*University of California at Irvine*
*University of California at Los Angeles*
*University of California at Santa Barbara*
*University of California at Santa Cruz*
*California Institute of Technology*
*Carnegie Mellon University*
*Case Western Reserve University*
*Clemson University*
*University of Colorado at Boulder*
*Colorado State University*
*Columbia University*
*Cornell University*
*David Sarnoff Research Center*
*Duke University*
*University of Florida*
*Florida Institute of Technology*
*Florida State University*
*Georgia Institute of Technology*
*University of Illinois at Urbana/Champaign*
*Lehigh University*
*Louisiana State University*
*University of Maryland*
*University of Massachusetts at Amherst*
*Massachusetts Institute of Technology*
*Massachusetts Microelectronics Center*
*University of Michigan*
*Microelectronics Center of North Carolina*
*University of Minnesota*
*New Jersey Institute of Technology*
*University of New Mexico*
*University of North Carolina at Chapel Hill*
*University of North Carolina at Charlotte*
*North Carolina State University*
*Northeastern University*
*The Ohio State University*
*Princeton University*
*Purdue University*
*Rensselaer Polytechnic Institute*
*Research Triangle institute*
*University of Rochester*
*Rochester Institute of Technology*
*Rutgers, The State University*
*Sandia National Laboratories*
*University of South Florida*
*University of Southern California*
*Stanford University*
*State University of New York at Albany*
*Stevens Institute of Technology*
*University of Texas at Austin*
*The Texas A&M University*
*Vanderbilt University*
*University of Vermont*
*University of Virginia*
*University of Wisconsin*
*Yale University*

## *University Advisory Committee (UAC)*

*The SRC University Advisory Committee is an independent body of university faculty that provides counsel on issues relative to the university community. This body has an important role in recommending policy for the research program.*

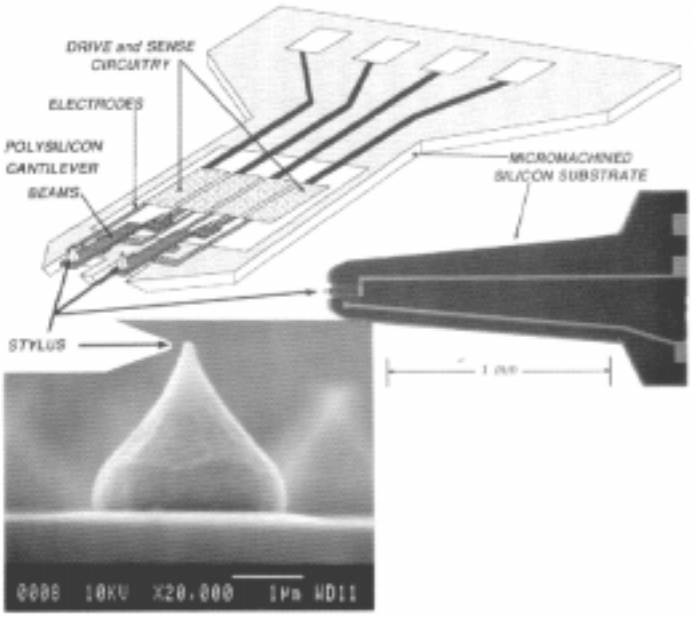
***Chairperson:***

| | |
|---|---|
| *Kensall D. Wise* | *Michigan* |

***Secretary:***

| | |
|---|---|
| *Cynthia L. Grotz* | *SRC* |

| | |
|---|---|
| *Jacob A. Abraham* | *Texas/Austin* |
| *James F. Freedman* | *SRC* |
| *Paul Gray* | *UC/Berkeley* |
| *David V. Kerns, Jr.* | *Vanderbilt* |
| *W. W. Lindemann* | *Minnesota* |
| *Noel C. MacDonald* | *Cornell* |
| *Nino A. Masnari* | *NC State* |
| *Carlton Osborn* | *MCNC* |
| *R. Fabian Pease* | *Stanford* |
| *John L. Prince III* | *Arizona* |
| *L. Rafael Reif* | *MIT* |
| *Ronald A. Rohrer* | *Carnegie Mellon* |
| *Al F. Tasch, Jr.* | *Texas/Austin* |




### *Chocolate Drop?*

***This iridium-coated polysilicon stylus, with a tip diameter of about 0.1 μm, was produced using precision micromachining as part of a multi-channel surface profilometer being developed at the University of Michigan. Such scan tips can be used in both contacting and non-contacting modes and can be read out either optically or electronically using on-chip circuitry. In the non-contacting mode, the polysilicon beam is driven at resonance; and the resonance shift produced by surface forces is used in a closed feedback loop to essentially implement an atomic force microscope. The tip shown here was produced using a completely dry etching process in an RIE whose performance these scan tips will eventually monitor. Additional research in machine vision is attempting to enhance the images such tips produce by deconvolving the stylus tip shape against the measured surface profile to extract the true surface shape. These profilometers promise to allow the accurate determination of sub-0.1 μm surface features for the rapid feedback of information intended to assist in optimizing future VLSI etching processes.***

***Professor Ken D. Wise***
***University of Michigan***

*The*

*SRC*

*Research*

*Program*

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# Research Integration: The SRC Strategic Goals

*The SRC Research Program is goal oriented. Goals are established through a close working relationship between senior members of the SRC corporate staff and committees of the Technical Advisory Board.*

*The strategic plan is used to guide, focus, and prioritize the projects and to provide a basis for measuring progress. The intent is to fund those technology areas that are most important to the international competitive strength of the industry and that are appropriate candidates for university research.*

*The research is executed principally in the U.S. university system; and the SRC has been able to foster a high degree of cooperation among industry, government, and academia. Since most of the research requires the skills of several fundamental disciplines, the SRC has also catalyzed interdisciplinary research within the university system.*

*To provide a research strategy that reflects industry requirements for a 10-year time span, the SRC conducts technology trend assessments. The SRC employs two approaches to increase the confidence level of projections defining the technology vision. The first approach identifies the technology trends over a period of the past, and extends these trends monotonically into the future ("technology push"). An alternate method involves envisioning the product applications of the future and the technical requirements to produce these products ("product pull"). An examination of the results of these two approaches identifies areas where technology projections fall short of meeting product requirements. This, in turn, identifies those research areas where new approaches are necessary.*

***James J. Freedman***
***Vice President,***
***Research Integration***

*Technology assessments resulted in the specification of the SRC 2001 Technology Goal Set. Since the SRC is only one of several elements in the total technology chain, the SRC must coordinate its research efforts with the other links in the chain. The SRC 2001 Strategy accomplishes this linkage.*

***Executive Committee***
***of the Technical Advisory Board (TAB)***

***Co-Chairpersons:***

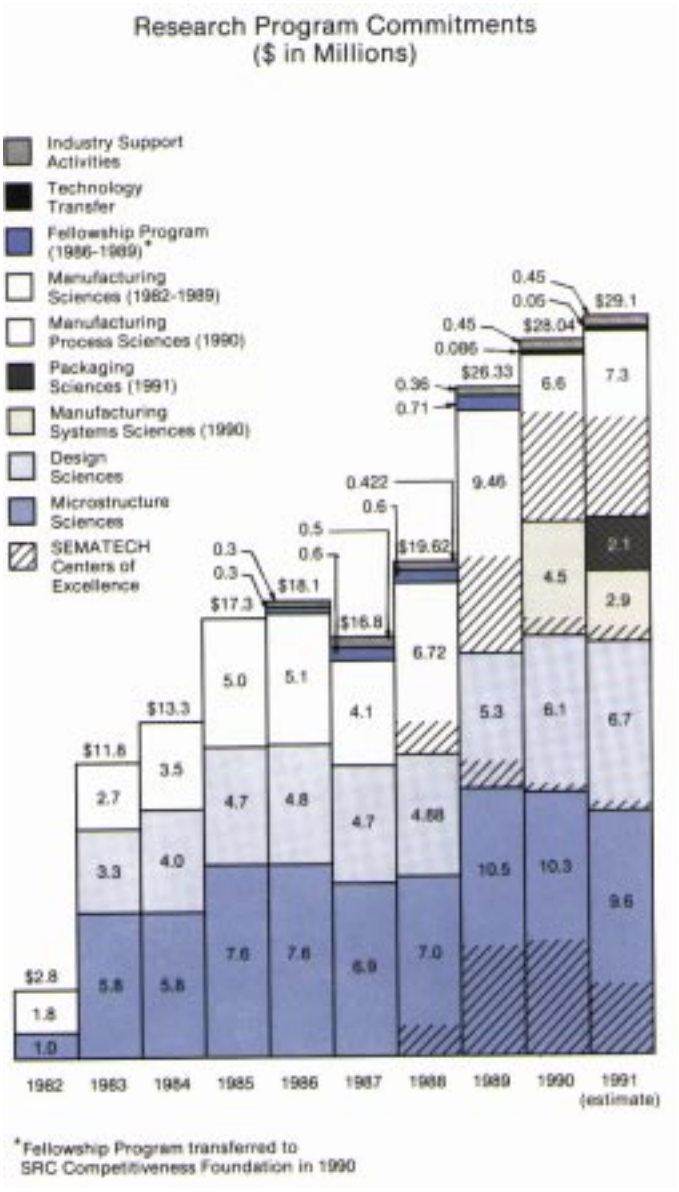
| | |
|---|---|
| James F. Freedman | SRC |
| Edward L. Hall | Motorola, Incorporated |

***Secretary:***

| | |
|---|---|
| Cynthia L. Grotz | SRC |

| | |
|---|---|
| John D. Bastian | Rockwell International Corporation |
| John R. Carruthers | Intel Corporation |
| Pallab Chatterjee | Texas Instruments Incorporated |
| James M. Daughton | Honeywell Incorporated |
| Lowell D. Deckard | NCR Corporation |
| Richard C. Donovan | AT&T |
| James Duley | Hewlett-Packard Company |
| Eugene D. Feit | SEMATECH |
| William R. Griffin | IBM Corporation |
| Sam Harrell | SEMI/SEMATECH |
| Thomas L. Haycock | Harris Corporation |
| Randall Isaac | IBM Corporation |
| Stephen Knight | AT&T |
| Tyler Lowrey | Micron Technology, Inc. |
| John M. Pierce | National Semiconductor Corporation |
| Llanda M. Richardson | Digital Equipment Corporation |
| Court Skinner | National Semiconductor Corporation |
| James N. Smith | Motorola, Incorporated |
| Jack Solomon | Union Carbide Industrial Gases, Inc. |
| K. Speierman | National Security Agency |
| William E. Starks | Varian Associates, Incorporated |
| Barry B. Whalen | MCC |
| Kensall D. Wise | University of Michigan |
| Donald L. Wollesen | Advanced Micro Devices, Inc. |

# *Research Operations*




*The U.S. semiconductor industry depends on the SRC to conduct university-based research that is forward-looking yet relevant to industry's needs. As long-term industry research has been reduced, university research has become increasingly important.*

*The SRC is the first research cooperative in a high technology industry and is exceptionally beneficial to all participants. Universities benefit from the knowledge contributed by the SRC's industry partners. Industry benefits from the increased relevance of the research. Students benefit from the higher quality of their educational experience. The U.S. infrastructure benefits from a successful cooperative paradigm. The U.S. Government benefits from the availability of more advanced technology.*

*SRC-funded projects address challenges in integrated circuit design, in device and circuit technology related to microstructure science, in manufacturing processes and systems, and in packaging. The division of effort is shown in the bar chart.*

*The objective of SRC Design Sciences research is to strengthen the international competitiveness of the United States in design technology leading to unsurpassed quality, minimum cost, and minimum time to market for technology-driven integrated circuit and electronic system products. The aim is to achieve a 30-fold increase in designer productivity within the next decade while applying a methodology of single-pass designs and a philosophy of correct-by-construction. Emphasis is currently shifting from chip design to multichip modules and system design principles and to the exploration of new algorithms supporting concurrent engineering philosophies.*

*Microstructure Sciences research is focused on a 0.15 micron minimum feature size technology. This will enable the production of single-chip integrated circuits with over 100 million active devices operating at clock rates exceeding 500 megahertz. To this end, emphasis is on device technology that overcomes problems associated with the "shrink path," alternate process architectures for high yields, and circuit elements that are tolerant of defects and variances.*

*Manufacturing Process Sciences research emphasizes process technologies with sufficient flexibility to produce the diversity of circuits required for future products. Objectives are a reliability of 0.1 FIT, a placement accuracy of 30 angstroms, and a manufacturing environment where particle sizes are less than 300 angstroms with less than 0.05 killer defects per square centimeter. Advanced lithography, deposition, and etch tools are key elements. X-ray lithography, feed forward processing tools operating in clusters, and configurations for minimum costs of manufacturing in a flexible environment are the elements of the research.*

*Manufacturing Systems Sciences deals with factory environment and operations. Factory management systems with SQC analysis and feedback, utilizing automated tools with in-situ sensors and based on physically derived process models, are envisioned. Models are being developed to maximize factory throughput for all loadings while operating at minimum unit cost.*

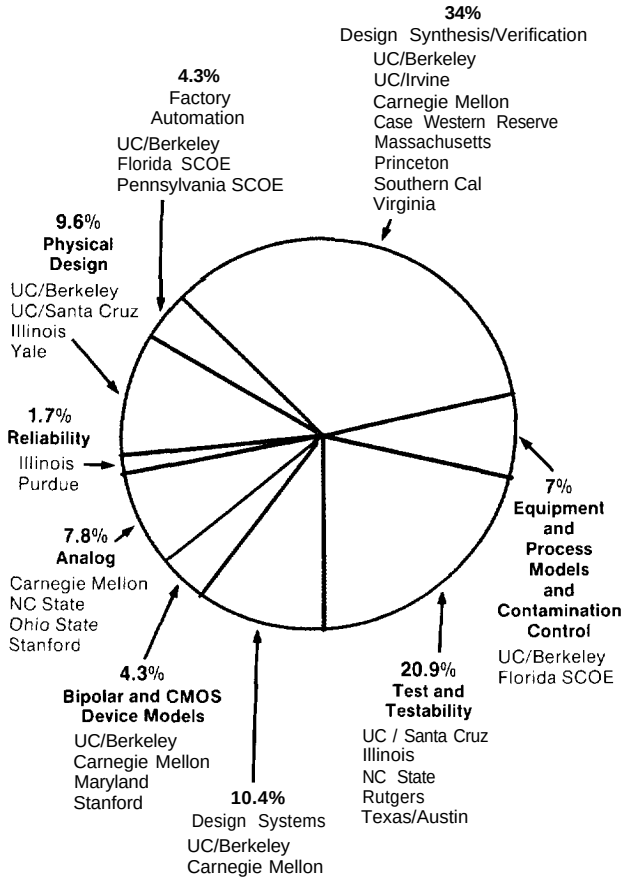
*Packaging research is focused on low-cost packaging while also investigating innovative system-level multichip concepts. Objectives are to provide at least 60-watt power dissipation while maintaining a rise time performance of 150 picoseconds with an input/output of 2000. Steps are underway to organize Packaging Sciences as a major research area in the SRC program.*

***William C. Holton***
***Vice President,***
***Research Operations***

***C. Edward Holland, Jr.***
***Director, SEMATECH***
***Centers-of-Excellence Program***

*An important and productive part of the SRC research program is funded through SEMATECH. Although the eleven SEMATECH Centers-of-Excellence (SCOEs) are focused strongly on technologies supporting wafer fabrication, their research is integrated with the broader SRC research agenda in supporting industry needs. SCOEs are identified in the budget pie charts that follow.*

# SRC Research in Design Sciences




*The 1990 budget for research in Design Sciences was $6.1 million. The pie chart shows the percentage of this budget that was allocated to each major technology area.*

*The Design Sciences segment of the SRC Research Program focuses on the issues that will enable designers of products to exploit the ULSI technologies being developed in Microstructure Sciences, Manufacturing Process Sciences, and Manufacturing Systems Sciences.*

*In the near term, Design Sciences focuses on synthesis of digital and analog circuitry, generation of comprehensive test sequences for digital products, innovative circuit design techniques, advanced design methodologies, and product development environments. In the medium term, today's capabilities will be enhanced to comprehend large, multichip systems consisting of complex analog and digital subsystems. On the farther horizon, Design Sciences research strives for full automation of the development of complex, system-level products.*

*The relative funding levels for the various segments of the Design Sciences agenda are based on priorities suggested by the Design Sciences Committee and on the unique strengths of the various institutions.*

*New thrust areas and updated priorities in support of the 2001 goal set have been developed in cooperation with the Design Sciences Committee. In addition to their efforts in developing the new goal set, members of this committee evaluated each of the research projects during formal Research Reviews and assessed a large number of new proposals.*

## 1990 Key Research Results

- *The ACACIA system has been improved significantly. Synthesized analog functions were demonstrated to occupy one-third of the area previously used.*
- *A functional interface allowing different Technology CAD tools to access wafer data was released.*
- *Major enhancements to the TimberWolf physical design system were completed, including analog placement features and major performance and layout quality improvements.*
- *A system generated complete test sets for a 100,000 transistor video processor chip design supplied by an SRC member.*
- *An oversampling modulator demonstrated 12-bit resolution at a Nyquist Rate of 2 MHz.*

## 1990 Events

*The following events were sponsored by Design Sciences in order to further the research agenda and to disseminate results.*

*Topical Research Conference on the Synthesis of Testable Designs*

*Workshop on System-Level CAD*

*Workshop on Designing for Quality*

*Technology Transfer Course on the iSPLICE3 Mixed Analog/Digital Simulator.*

*Technology Transfer Course on ACACIA Analog Synthesis System.*

*Technology Transfer Course on the MIS-II Logic Synthesis System.*

***Jeffrey L. Hilbert***
***Director,***
***Design Sciences***

## Industrial Residents

***Justin E. Harlow III***
*National Semiconductor Corporation*
*Program Manager, Design Sciences*

***Kenneth L. Pocek***
*Intel Corporation*
*Program Manager, Design Sciences*

## Design Sciences Committee of the Technical Advisory Board (TAB)

***Chairperson:***
*William R. Griffin* — *IBM Corporation*

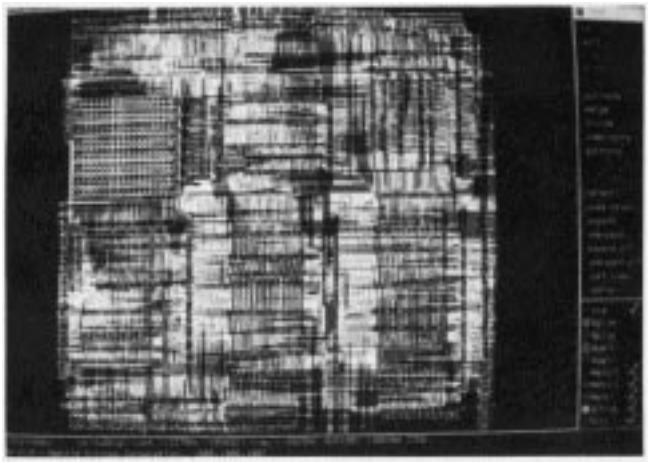
*Vice-Chairperson:*
*Jack Mullins* — *NCR Corporation*

| | |
|---|---|
| *Anil Agarwal* | *Alcoa Electronic Packaging, Inc.* |
| *Paul J. Ainslie* | *Delco Electronics Corporation* |
| *Larry Bashaw* | *Honeywell Incorporated* |
| *Herbert S. Bennett* | *NIST* |
| *Henry Blume* | *Intel Corporation* |
| *Char/es T. Brodnax* | *E-Systems, Incorporated* |
| *Basant Chawla* | *AT&T* |
| *Bernie Chern* | *National Science Foundation* |
| *Lewis M. Cohn* | *Defense Nuclear Agency* |
| *W. Terry Coston* | *Harris Corporation* |
| *Manuel A. d'Abreu* | *General Electric Company* |
| *Antun Domic* | *Digital Equipment Corporation* |
| *James Duley* | *Hewlett-Packard Company* |
| *David Franco* | *Xerox Corporation* |
| *Ian Getreu* | *Analogy Inc.* |
| *Dennis Heinbuch* | *National Security Agency* |
| *John W. Hines* | *Wright Laboratory* |
| *William Johnson* | *Texas Instruments Incorporated* |
| *Robert P. Larsen* | *Rockwell International Corporation* |
| *Teh-Hsuang Lee* | *Eastman Kodak Company* |
| *William E. Moss* | *Advanced Micro Devices, Inc.* |
| *Joseph A. Muslin* | *Hughes Aircraft Company* |
| *Kenneth Ray* | *Motorola, Incorporated* |
| *Bill Read* | *MCC* |
| *Greg Roberts* | *Micron Technology, Inc.* |
| *James Rutledge* | *SEMATECH* |
| *Peter W.J. Verhofsfadt* | *National Semiconductor Corporation* |
| *Vincent Zagardo* | *Westinghouse Electric Corporation* |

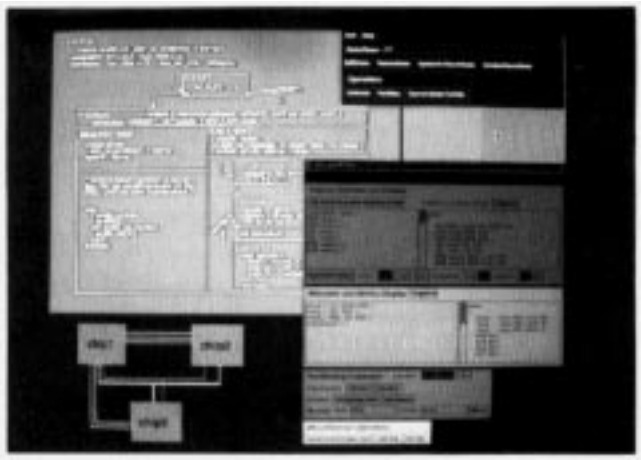
## *The 48-Hour Chip Layout*

*Product introduction cycles must become shorter each year, even as the complexity and performance requirements of the products increase exponentially. This project has demonstrated what future design technologies may offer. The research team undertook the layout of a ten-point Fourier Transform processor chip in under 48 hours, using USC's developmental ADAM synthesis system in conjunction with a commercial Silicon Compiler. Starting with a behavioral specification of the processing algorithms, the team debugged the design and produced a layout in two working days. This effort resulted in a chip just over 5 mm square that will produce a new result every 210 nanoseconds. The group has also developed a robot arm controller in less than a week and is continuing to push the synthesis technology toward "The 48 Hour Chip Layout" needed in future designs.*

*Professor Alice C. Parker*
*University of Southern California*



*This chip, synthesized by the ADAM system, implements a novelalgorithm which produces a new Fourier transform result every 210 nanoseconds. Specified in the VHDL language, the synthesis and layout took only 48 hours.*



*Workstation image of the SpecSyn tool thatprovides for formal, yet simple, system behavior specification and possesses a variety of capabilities for rapid exploration of alternative chip implementations.*

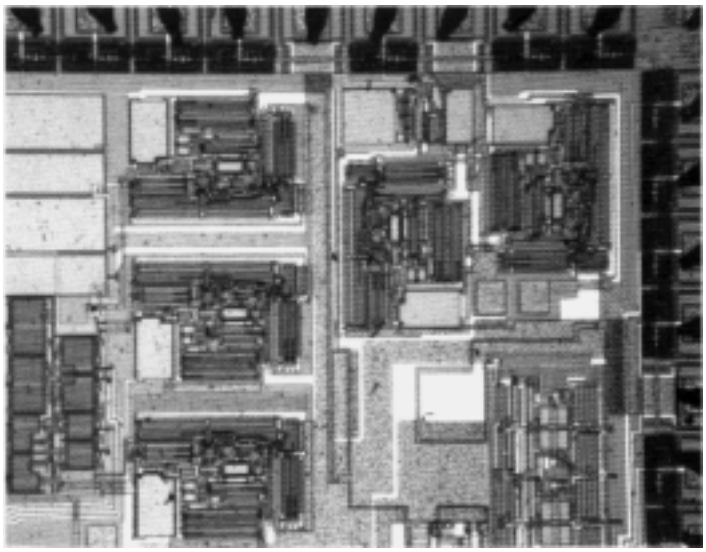
## *The SpecSyn Tool*

*High-level system specifications are very abstract about such information as communication protocols and transaction response rates. Traditionally, this information has been captured in the English language and translated to various computer representations during system design. This research effort aims to capture the design knowledge of a complete system, potentially consisting of many chips, in an Executable Specification. The SpecSyn tool, currently in development, provides powerful system planning capabilities that can automatically partition the specification into chips, determine a good busing scheme, and synthesize interfaces for different communication protocols with the goals of meeting constraints on chip cost and performance.*

*Professor Daniel D. Gajski*
*University of California at Irvine*

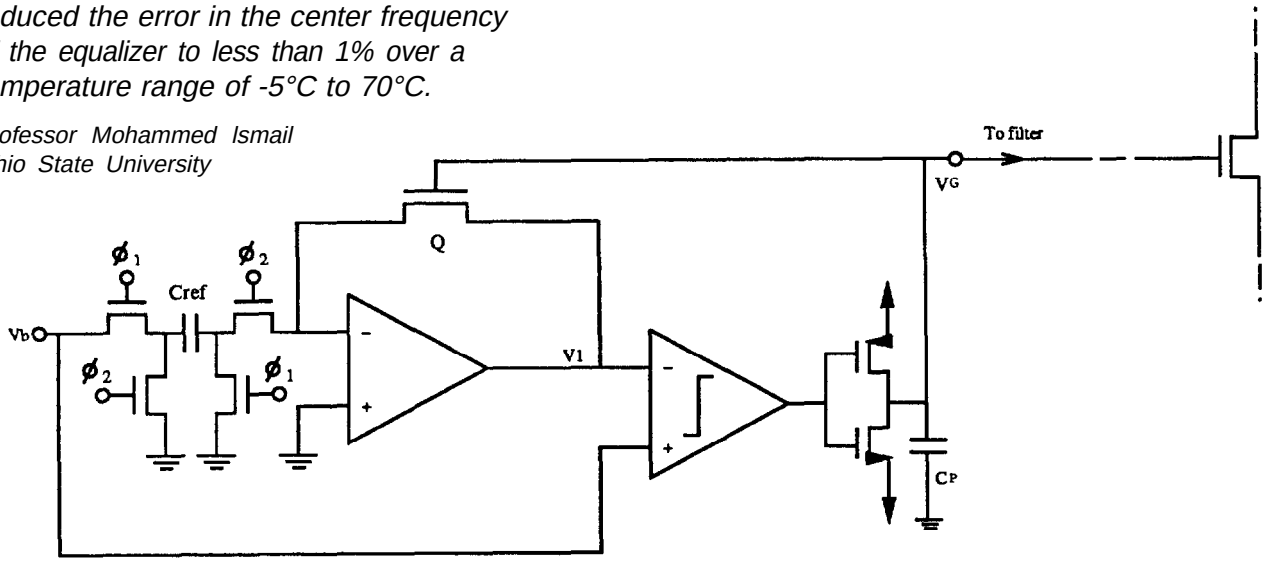
# *On-Chip Automatic Tuning for Analog MOS ICs*

*Continuous-time analog ICs are naturally suited for high-speed applications in mixed analog/digital MOS VLSI systems. A crucial design issue in many high-performance analog ICs is the accurate on-chip implementation of circuit RC time-constants. Although these analog ICs use voltage-controlled MOS resistors, it is difficult to achieve accurate time-constants due to random variations in process parameters. A subtle circuit design solution to this problem is to use "master-slave" on-chip automatic tuning. The circuit shown in the schematic is a novel on-chip automatic tuning circuit "master" based on a switched-capacitor resistor in a gain control loop. It is used to automatically adjust the time-constants of many analog ICs "slaved" on the same chip as long as they are at a close proximity to the tuning circuit. The circuit* was *built on a 2 μm CMOS p-well process to tune an amplitude equalizer filter. The photomicrograph shows the equalizer (left half of the picture) and the tuning circuit (upper right-hand corner). It significantly reduced the error in the center frequency of the equalizer to less than 1% over a temperature range of -5°C to 70°C.*



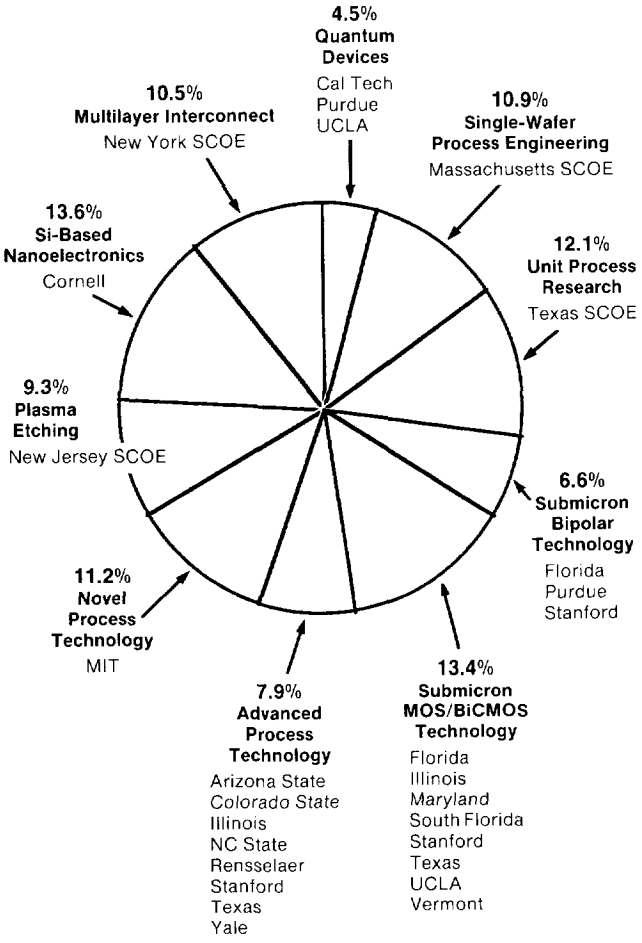
*Photomicrograph of the equalizer circuit with on-chip automatic tuning.*

*Professor Mohammed Ismail*
*Ohio State University*




*The automatic tuning circuit.*

# SRC Research in Microstructure Sciences




*The 1990 budget for research in Microstructure Sciences was $10.3 million. The pie chart shows the percentage of this budget that was allocated to each major technology area.*

*Microstructure Sciences is concerned with the phenomena, structures, materials, and processes used to fabricate semiconductor devices and integrating these devices into ULSI circuits. The mission is to realize ICs of increased density and performance, utilizing new active devices, submicron structures, new materials, and novel processes.*

*Major near-term priorities include gate oxide processes and reliability, multilevel metal enhancements, modeling of devices and processes, improved understanding of physical and chemical phenomena, and CVD/epitaxial processes. Extended-term priorities include selective deposition, 3D device and 2D process simulators, power ICs, SOI, and Si-Ge processes and structures. Longer range priorities include 3D structures, quantum structures, low-temperature operation, and interconnect paradigms. Exploratory concepts include atomic layer doping, optoelectronics-on-Si, neural network structures, and quantum device functional blocks.*

*The Microstructure Sciences Committee strongly supported SRC research in 1990 by their participation in several strategic planning sessions and in nine muitiple-contract reviews. In addition, 150 highly appreciated Industrial Mentors contributed guidance, samples, and equipment to Microstructures research.*

### *1990 Key Research Results*

- *A self-limiting oxynitride gate dielectric produced by rapid thermal processing in $N_2O$ ambient, with a large charge-to-breakdown, less charge trapping, and significantly reduced interface state generation.*
- *A power modulation technique that can be applied directly to industrial reactors to determine dominant chemical reactions, including intermediates, and reaction rates.*
- *A novel tungsten-containing DUV photo-resist which, after development and subsequent oxidation and reduction treatments, produces a W seed layer for selective CVD or electroless plating.*
- *A universal electron inversion layer mobility model for SPICE circuit simulation, without requiring refitting of the model parameters for any new or modified process sequences.*

### *1990 Events*

*The following three 1990 SRC events were sponsored by Microstructure Sciences. The total attendance for these three events was 190.*

*Technology Transfer Course on Integrated Technology Modeling for Integrated Circuit Process and Device Design*

*Topical Research Conference on Interconnect Technology*

*Workshop on Integrated Semiconductor Representations for Technology CAD*

***William T. Lynch***
***Director,***
***Microstructure Sciences***

***Industrial Residents***

***John E. Gragg***
*Motorola, Incorporated*
*Program Manager, Microstructure Sciences*

***Peter Verhofstadt***
*National Semiconductor Corporation*
*Program Manager, Microstructure Sciences*

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| *Brooke Jones* | *Rockwell International Corporation* |
| *William J. Lautenberger* | *E.I. du Pont de Nemours & Company* |
| *David L. Losee* | *Eastman Kodak Corporation* |
| *Gayle Miller* | *NCR Corporation* |
| *David E. Moss* | *Delco Electronics Corporation* |
| *Yoshio Nishi* | *Hewlett-Packard Company* |
| *Timothy R. Oldham* | *Harry Diamond Laboratories* |
| *A.L. Rivoli* | *Harris Corporation* |
| *James Rutledge* | *SEMATECH* |
| *Larry Schmitz* | *Hughes Aircraft Company* |
| *Robert A. Stehlin* | *Texas Instruments Incorporated* |
| *Clarence J. Tracy* | *Motorola, Incorporated* |
| *James C. Vesely* | *Xerox Corporation* |
| *Nancy Welker* | *National Security Agency* |
| *Robert M. Werner* | *Wright Laboratory* |

# PISCES Program Enhanced

*Two-dimensional device simulation using Stanford's PISCES program now provides enhanced usability and flexibility. The SIMPL-IPX interface (see Figure 1a) has been modified to incorporate PISCES dialog commands and thereby initiate device analysis automatically. New PISCES utilities support generalized auto-gridding (see Figure 1b) so that the user is relieved of this complex and often tedious task. Interactive bias specification is provided so that the user interacts with the program in a way that emulates a real measurement system (i.e., the HP 4145). In order to achieve efficient "curve tracer" mode simulations, PISCES now includes new bias projection capabilities so that the program automatically and efficiently chooses bias points to obtain smooth I-V curves.*

*In contrast to simulators that are device specific, PISCES accommodates general bias conditions (dc, ac and transient) and complex and non-planar geometries. New capabilities are being developed for multi-material systems, both silicon- and compound-based heterojunction devices. Using a layout-based approach, PlSCES can quick/y extract key technology dependencies of a wide variety of IC devices (bipolar, MOS and parasitic effects such as latchup). Such flexibility is invaluable both to technologists and IC circuit designers.*

*Professor Robert W. Dutton*
*Stanford University*

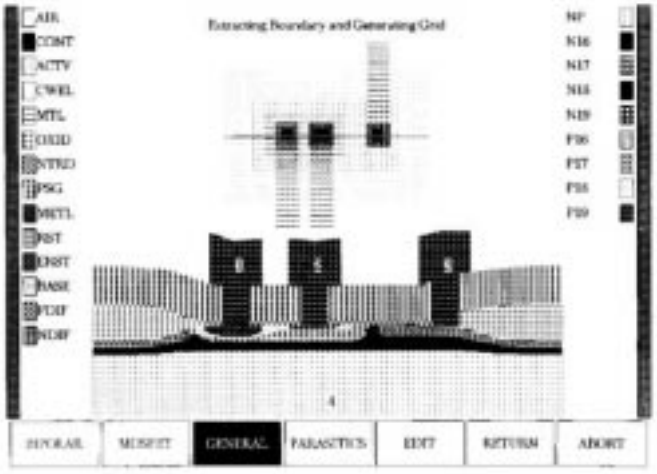



*Figure 1a. Cross section of device after process simulation*

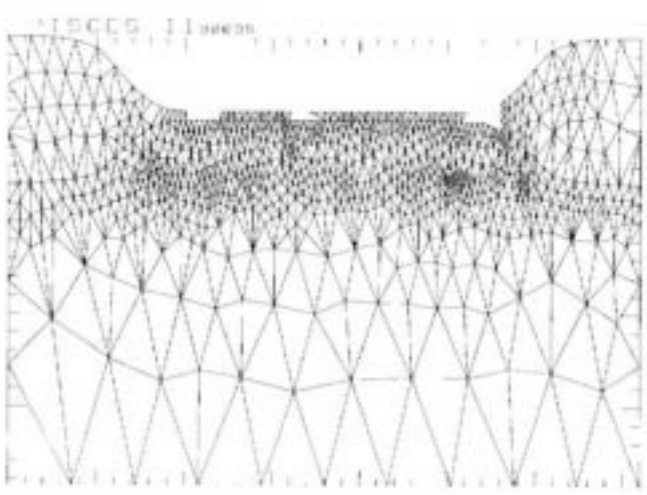


*Figure1b. PISCES grid*

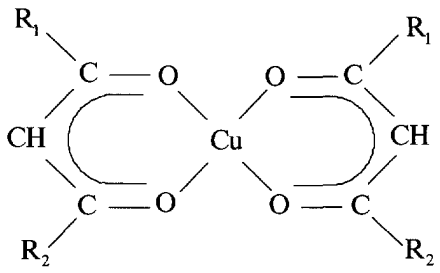
# Blanket and Selective Copper CVD Program

*This project is developing a manufacturable chemical vapor deposition (CVD) process for selective and blanket copper for one-half micrometer and smaller generations of devices.*

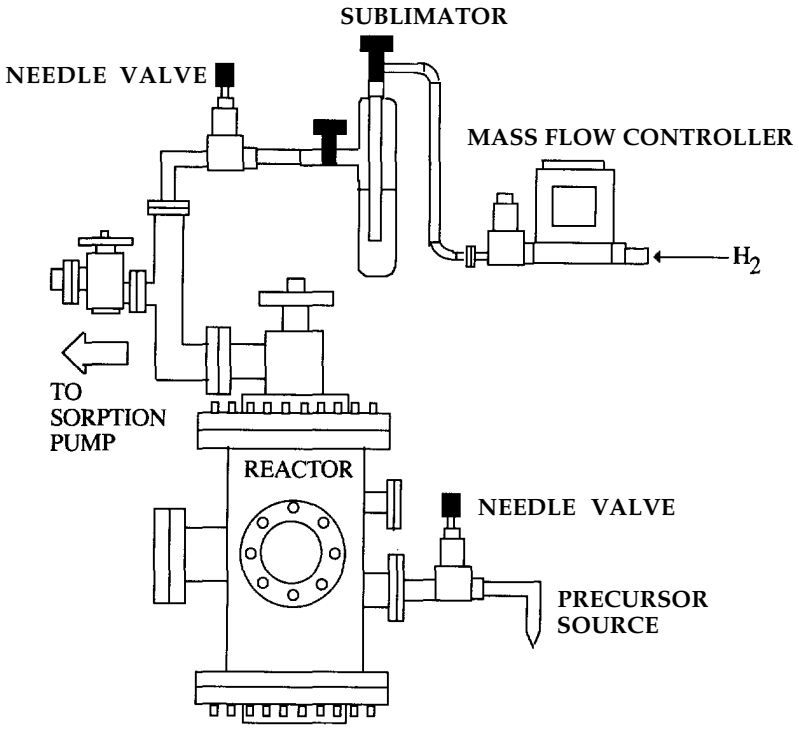
*In 1990, CVD of high purity copper was achieved at low temperatures (150-350°C), using β-diketonate precursors in a cold wall reactor with deposition rates greater than 100 Å/s and with uniformities of ±1% across a 125 mm wafer. High quality films with resistivities of 1.7 μΩcm have been demonstrated. This chemical process is practical and environmentally friendly.*

*Demonstrating the feasibility of selective copper CVD and its dependence on substrate type, morphology, and degree of interaction with hydrogen has led to identifying a mechanism for selectivity. This is being investigated, and a "four-step" process for selective growth is being developed and tested.*

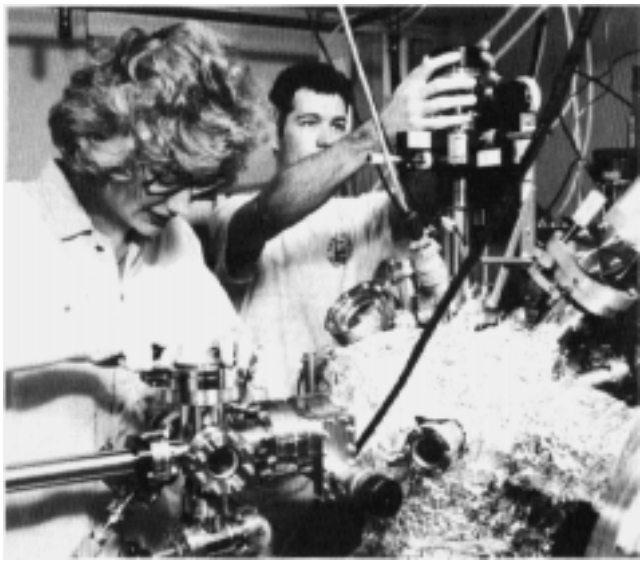
*Professor Alain E. Kaloyeros*
*State University of New York at Albany*




*Chemical structure of the β-diketonate precursors. $R_1$ and $R_2$ represent radicals such as $CH_3$ or $CF_3$.*

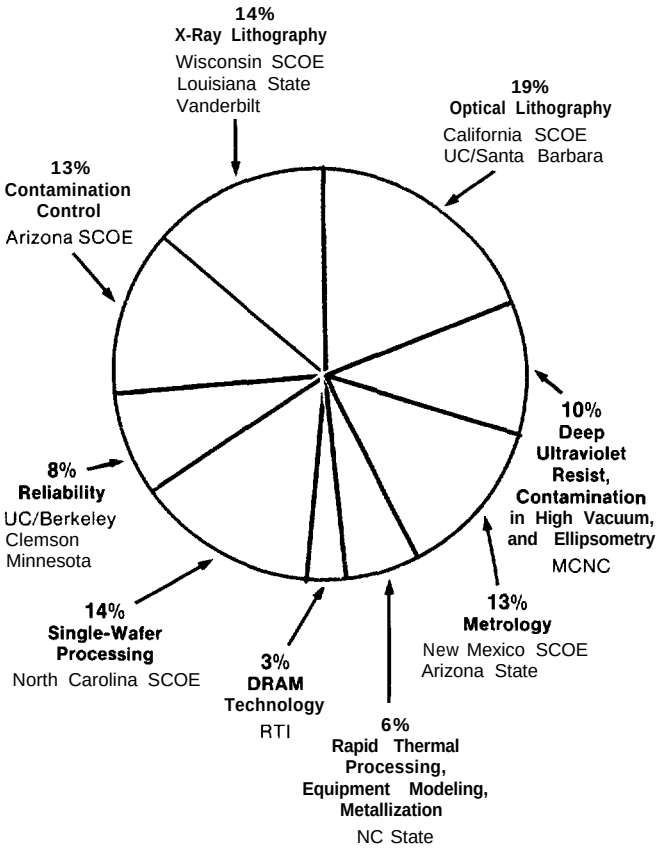



*Schematic drawing of the customized 5" wafer cold-wall CVD reactor used for copper deposition.*



*Research students Kirsten Belles and Chris Dundon setting up a CVD reactor for copper deposition.*

# SRC Research in Manufacturing Process Sciences




*The 1990 budget for research in Manufacturing Process Sciences was $6.6 million. The pie chart shows the percentage of this budget that was allocated to each major technology area.*

*The Manufacturing Process Sciences mission is to provide a basis for improved understanding, control, and application of semiconductor fabrication processes and to extend their capability to the 0.15 micron devices of the next decade. Current emphases include both optical and X-ray lithography, etching, and deposition and supporting efforts in metrology, contamination control, and reliability.*

*Optical lithography research focuses on new sources, system design to extend resolution, novel resist concepts, and dry development approaches for surface imaging resists. X-ray lithography addresses the capabilities of proximity printing.*

*Etching explores excitation schemes that give the highest etch rate, maximum anisotropy and uniformity, and minimum damage from ion bombardment.*

*Deposition research deals with processes and tools for the cluster environment.*

*Metrology encompasses techniques for temperature measurement, critical design dimensions, pattern wafer profiles, film composition, and properties in real time.*

*Contamination Control addresses the detection, removal, or elimination of particles throughout the fabrication operation and the understanding of the relationship between contamination concentrations and electrical defects.*

*Reliability studies relate to accelerated testing and modeling of major failure modes and to modeling the influence of design parameter and process variance on the aging of circuit performance.*

### *1990 Key Research Results*

- *An optical technique to measure temperature change with a resolution better than 0.5°C.*
- *An optical technique to measure latent image during photoresist exposure.*
- *Implementation of a solid-state deep ultraviolet (DUV) source for lithography*
- *Development of a 3D model of a simulation of X-ray proximity mask distortions that would result from construction, mounting, and irradiation.*
- *An $O_2$ plasma-robust, DUV-sensitive, Novolac-based photoresist.*
- *Low temperature remote plasma CVD oxides with properties superior to thermal oxides.*

### *1990 Events*

*Four SRC events were sponsored during 1990 to bring together participants from the SRC community. These included the following Workshops and Topical Research Conferences (TRC):*

*TRC on High Reliability Gate Dielectrics*

*Workshop on Temperature Measurement in Single- Wafer Processing*

*TRC on Metrology for Semiconductor Manufacturing*

*TRC on Lithography*

***J. Richard Burke***
***Director,***
***Manufacturing Process Sciences***

### *Industrial Resident*

***Syed Rizvi***
*Texas Instruments Incorporated*
*Program Manager, Manufacturing Process Sciences*

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***Vice-Chairperson:***

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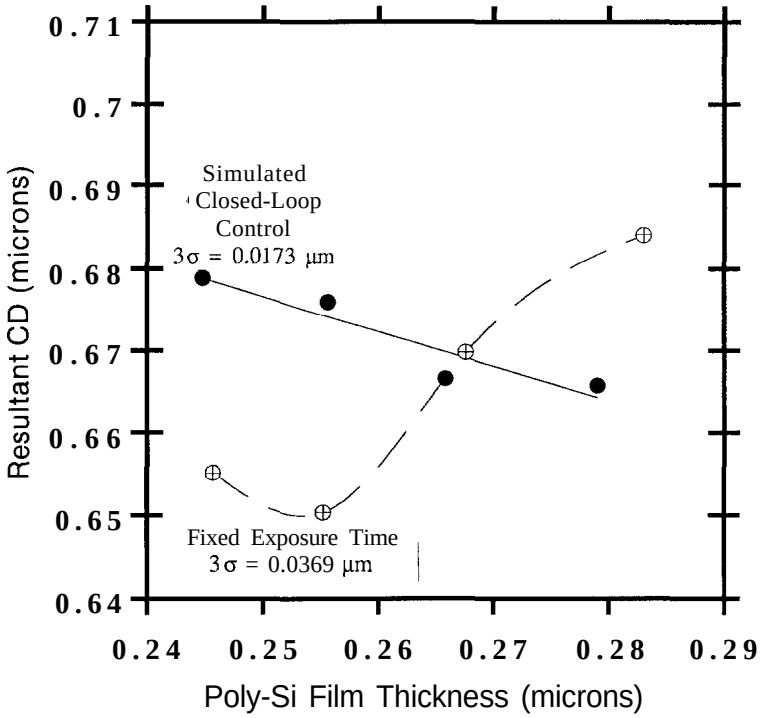
| *Albert Wang* | *Hewlett-Packard Company* |
| *Douglas Weaver* | *Sandia National Laboratories* |

# Photoresist Exposure Control

*Light scatter (diffraction) techniques have been used to directly monitor the dose in undeveloped photoresist resulting from exposure. The latent image of a periodic structure in the photoresist is illuminated with a laser, and the diffracted light is indicative of the resulting critical dimension (CD) in the subsequently developed photoresist. The technique is useful for controlling exposure when the optical properties of the substrate change, such as from variations in film thickness resulting from wafer processing. The graph shows the improvement in CD control provided by the diffraction technique (indicated by "Simulated Closed-Loop Control") compared to the present control technique ("Fixed Exposure Time"). CD variation is reduced by more than 2X for 0.7 μm lines and more than 3.7X for 1.0 μm lines. The technique has been applied to several photoresist types, including a chemically amplified deep UV resist. The technique can be applied to periodic structures 150 μm or smaller.*

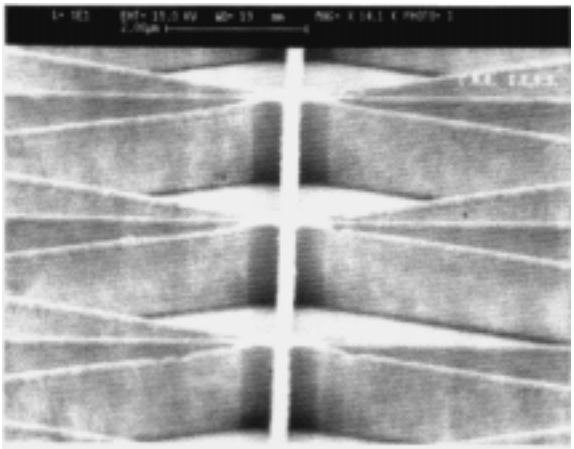
*Professor J. Robert McNeil*
*University of New Mexico*




*Critical Dimension (CD) Uniformity for Nominal 0.7 μm Lines*

# X-Ray Lithography

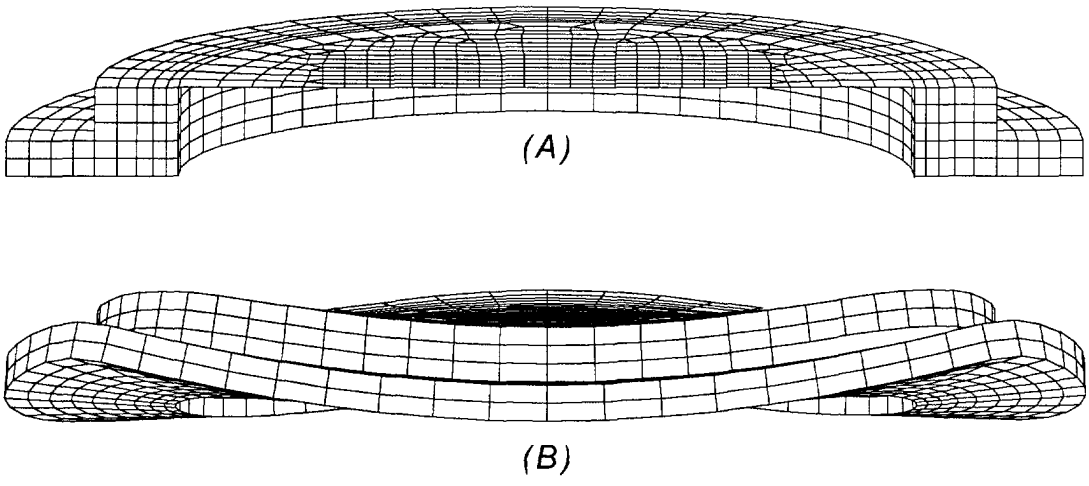
*The Wisconsin Center for X-ray Lithography (CXrL) is using radiation from the electron storage ring, Aladdin, as a source of intense, well-collimated X-rays to develop a synchrotron-radiation X-ray lithography baseline process for submicron feature sized ICs. CXrL research encompasses the design of manufacturing tools, X-ray mask standards, process-modeling CAD too/s, and X-ray-sensitive photoresists. The goal is to develop the technology base for <0.25 micron technology and to demonstrate devices having these features sizes.*



*SEM micrograph of 0.10 μm lines on silicon exposed at CXrL. Height of lines is 1.0 μm.*

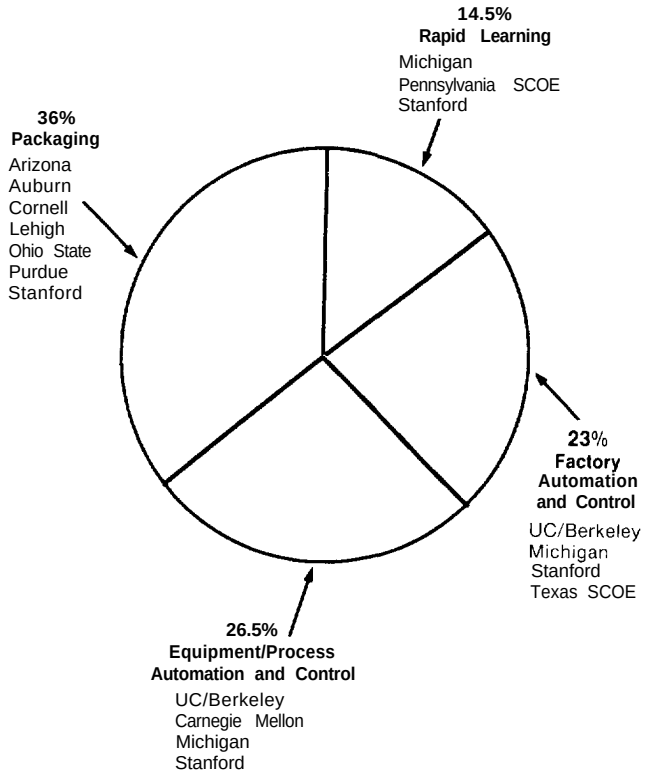
*Research on understanding and controlling the microscopic deformations occurring in masks during normal use has led to NIST proposals for improved mask designs for use by U.S. industry. CXrL has designed with the University of Minnesota a test chip for a six-level NMOS process that includes process control monitors, parametric test devices, and enhancement and depletion mode transistors in a ring oscillator circuit. This chip also uses a novel submicron alignment scheme. Processing this chip is intended to be the first step toward identifying any barriers impeding the use of X-ray lithography.*

*Professor Franco Cerrina*
*University of Wisconsin*




*Mask modeling. Figure (A) is a cross sectional view of the finite element model of an X-ray lithography mask. Figure (B) is a side view of a kinematically mounted mask support ring displaced by gravity.*

# SRC Research in Manufacturing Systems Sciences




*The 1990 budget for research in Manufacturing Systems Sciences was $4.5 million. The pie chart shows the percentage of this budget that was allocated to each major technology area.*

*Manufacturing Sciences was divided into two new Science areas in 1990: Manufacturing Process Sciences and Manufacturing Systems Sciences. The division was made to accommodate the increase in the manufacturing program resulting from the infusion of funds from SEMATECH and the importance of the systems and packaging aspects of the semiconductor manufacturing enterprise.*

*Manufacturing Systems Sciences is largely focused on the software support and associated hardware required to manage an efficient semiconductor manufacturing operation. The research falls naturally into two major segments: (1) the monitoring and control of the direct wafer manufacturing process, and (2) the management of the manufacturing enterprise as a who/e, including lot scheduling and other factors affecting wafer cost and throughput time.*

*Research in semiconductor packaging was included under Manufacturing Systems Sciences in 1990, and was increased by more than 30% in recognition of its breadth and scope. Packaging research is divided into two segments: (1) the software aspects of package design, analysis, and simulation, and (2) the aspects of materials, process, and measurements.*

*The distribution of the $4.5 million funding in Manufacturing Systems Sciences for 1990 is shown in the pie chart by the major thrust areas described above. These major thrust areas and more detailed subdivisions have been identified and defined through a sequence of interactions with members of the TAB Manufacturing Systems Sciences Committee and Packaging Subcommittee who have contributed greatly to the management of the program.*

### *1990 Key Research Results*

- *First version of the SPEEDIE plasma deposition and etch process model completed.*
- *Diagnostic system demonstrated for low-pressure chemical vapor deposition (LPCVD) equipment.*
- *A new generic cell controller devised.*
- *New techniques demonstrated for analyzing correlations within test results.*
- *Highly sensitive microflow sensors demonstrated.*
- *New techniques for in-process process monitoring demonstrated.*
- *System-level package partitioning and analysis system enhanced.*
- *Package electrical simulation software expanded and demonstrated.*
- *New transmission line thin film interconnect structures characterized.*

### *1990 Events*

*The fifth annual Workshop on Computer-Integrated Manufacturing (CIM) for the IC Industry was held in August. This event is jointly sponsored by the SRC and DARPA. The workshop encourages close and cooperative interactions among university research groups and provides a forum for industry and university researchers to exchange views on the applicability of the research in meeting the industry's needs.*

***Norman F. Foster***
***Director,***
***Manufacturing Systems Sciences***

***Industrial Resident***

***John H. Kelly***
*IBM Corporation*
*Program Manager, Manufacturing Systems Sciences*

***Manufacturing Systems Sciences Committee of the Technical Advisory Board (TAB)***

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| *Dennis Herrell* | *MCC* |
| *Joseph E. Johnson* | *Westinghouse Electric Corporation* |
| *Mary E. Kinsella* | *Wright Laboratory* |
| *Ray Kjar* | *Rockwell International Corporation* |
| *Dennis Krausman* | *E-Systems, Incorporated* |
| *Loren W. LInholm* | *NIST* |
| *Pravin Parekh* | *Honeywell Incorporated* |
| *Robert B. Reams* | *Harry Diamond Laboratories* |
| *John T. RobInson* | *Texas Instruments Incorporated* |
| *James Rutledge* | *SEMATECH* |
| *Anthony Scribani* | *Eastman Kodak Company* |
| *Steven Shaw* | *National Semiconductor Corporation* |
| *Marlin Shopbell* | *Digital Equipment Corporation* |
| *William E. Starks* | *Varian Associates, Incorporated* |
| *Dean Toombs* | *Intel Corporation* |
| *Branimir von Turkovich* | *National Science Foundation* |
| *Albert Wang* | *Hewlett-Packard Company* |

# *Thermally Induced Strains in Electronic Packages*

*Due to the mismatch of thermal expansion coefficients in the components of an electronic package, mechanical strains are induced in the silicon chip under thermal load on the package. For determination of thermally induced strains in an electronic package, this research team has been applying an experimental methodology called Fractional Fringe Moiré Interferometry, which is enhanced by Digital image Processing.*

*Packages with chips of different sizes, both coated and uncoated, have been investigated. The packages were sliced along a plane selected to expose the chip and the lead frame. Crossed gratings with a frequency of 1200 lines/mm were replicated on the specimen surface and the specimen was placed into a special cooling device. To secure a virtual grating frequency of 2400 lines/mm, corresponding to a sensitivity of 0.417 $\mu m$ per fringe order, the apparatus and specimen were adjusted for proper optical alignment and orientation. After its null field patterns for each displacement component had been recorded, the specimen was cooled down to -50°C while fringe patterns were continuously recorded. Selected frames (typical example shown in the figure), representing deformation fields at selected temperatures, were analyzed by image processing software. The net mechanical strains in the chip, which were due to the inequality in thermal expansion coefficients of the different materials in the package, can be obtained after subtraction of the free expansion strains.*

*Moire interferometry fills the gap in capabilities of other techniques, since it can be used for measurements in both the macromechanic and micromechanic domains. Full displacement fields in the chip in electronic devices subject to uniform cooling were rendered measurable by the method. The strains were computed from these field data. The effect of the chip sizes and coating on strain /eve/s were successfully investigated. The experimental data obtained may provide an important reference for package design.*

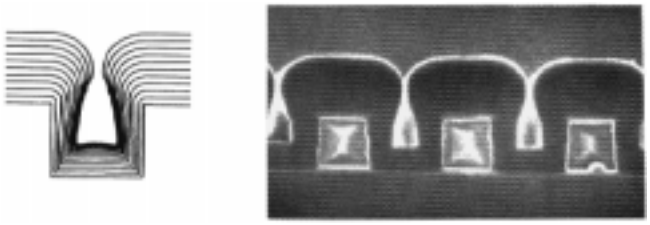
*Professor Arkady S. Voloshin*
*Lehigh University*

*A typical moiré pattern of IC package deformation (fringes are contours of constant axial displacements).*

## SPEEDIE: A Profile Simulator for Etching and Deposition

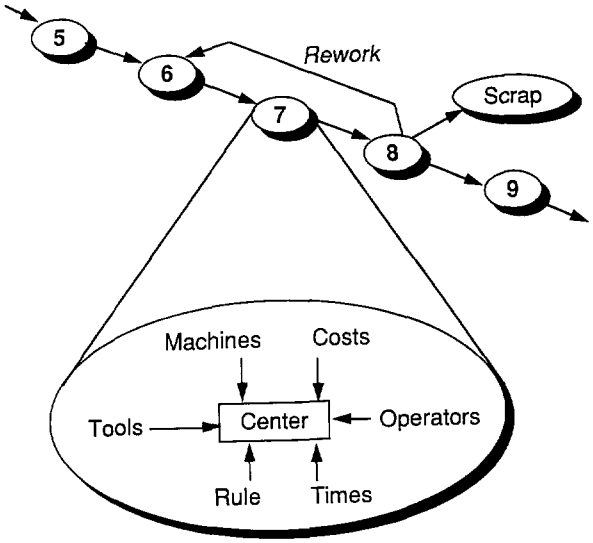
*A new physically based profile simulator has been developed for plasma etching and CVD processes. SPEEDIE calculates angular and energy distributions of ions and fast neutrals using a Monte Carlo (MC) simulator for ion sheath transport. Fluxes at each point on the profile can be calculated using either MC or analytical methods which consider 3-D transport by molecular flow, surface diffusion and adsorption/r-e-emission. Etch rates are determined using a choice of etch models, while LPCVD and PECVD use a sticking coefficient model. A modified string algorithm, which allows simultaneous etching and deposition, is used to move the surface. The first version of SPEEDIE has been recent/y released to SRC member companies.*

*Professors J.P. McVittie and K.C. Saraswat*
*Stanford University*



*Simulation of LPCVD Of $SiO_2$ from silane on metal lines*

## Coherent Integrated Planning System (CHIPS)




*An analysis and planning workstation called CHIPS (Coherent Integrated Planning System), is being constructed to a/low diverse analysis tools to be brought to bear on the difficult problems associated with the processing, analysis, and implementation of new semiconductor manufacturing technologies. CHIPS is a cohesive, data-driven modeling system for predicting factory performance. The manufacturing process flow is modeled as a sequence of "centers" with associated queues, operators, process machines, and tools (e.g. masks) required for the process. A portion of a sequence of "centers" (process steps) is illustrated in the figure with allowance made for rework loops and scrapped product.*

*Professor Don Phillips*
*Texas A&M University*

### *Intellectual Property*

***In 1990, the SRC added to its intellectual property portfolio in packaging, sensors, metallization processes, and advanced technology devices. Forty SRC Inventor Recognition Awards were conferred to recognize faculty and graduate students participating in research leading to pa tent applications and significant software development.***

***Gerold W. Neudeck (photo above) is a Professor of Electrical Engineering at Purdue University and a three-time, award-winning SRC inventor for quasi-dielectrically isolated bipolar transistors, self-aligned IC bipolar transistor with monocrystalline contacts, and high performance SOI bipolar transistor structure. With SRC support, Professor Neudeck secured patent #4,829,016 for Bipolar Transistor by Selective and Lateral Epitaxial Overgrowth and has four additional patents currently pending at the U.S. Patent Office.***

# *Technology Transfer*

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# Technology Transfer

*The Industrial Mentor Program continues to be one of the SRC's most valuable communication links. Harris Corporation has one of the most active mentoring teams among the SRC membership and has helped to design an effective SRC mentoring course for presentation on site at other companies. Harris Semiconductor Sector President Jon E. Cornell describes the benefits Harris derives this way, "The SRC is ... the best investment we have in terms of dollars in research and development; in terms of what we get back. It's an effective vehicle for transferring information technology out of academe and into the industrial process to help Harris be more competitive."*

*In the area of technology transfer, twenty-nine case histories of attempts to transfer SRC research results to practical application in industry were analyzed. Findings of the study were compiled in a white paper to promote transfer efficiency and motivate the membership to make greater use of SRC research products. In addition, a "Best Practices" Workshop focused on improving the Industrial Mentor Program, student activities, internal company issues, and communications channels.*

*The largest SRC-sponsored event in 1990 was TECHCON '90, a general conference showcasing SRC research and bringing together more than 550 industry/ government/university participants. Three other SRC events were broadcast over the National Technological University network.*

*Nearly 900 new technical documents generated from SRC research were catalogued into the SRC library in 1990, and more than 12,000 copies of library documents were distributed on request to membership and government agency personnel. Tapes added to the SRC's Video Library expanded the resources for acquainting industry audiences with the products of SRC research.*

***Richard A. Lucic***
***Director,***
***Technology Transfer***

*The information Central database and electronic mail facility continues to promote communications throughout the SRC community.*

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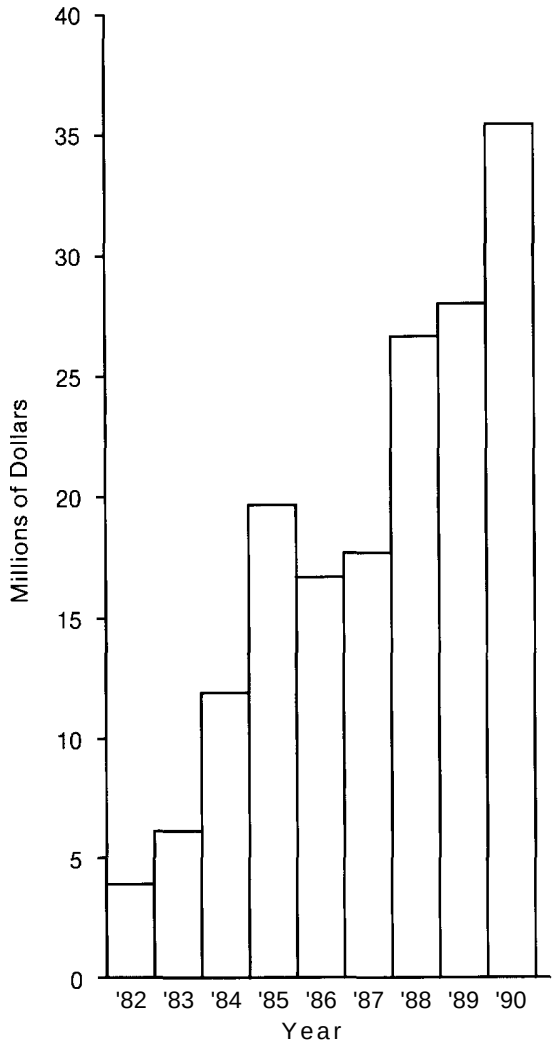
# Financial Report




*Revenue History*

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*Mr. Sumney and Dr. Schwettmann fielding questions from the Plenary Session audience at TECHCON '90.*

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*The Annual Report of the Semiconductor Research Corporation is published each June to summarize the directions and results of the SRC Research Program, present the formal financial report, and provide information on activities and events of the SRC industry/government/university community for the previous calendar year. The highlight material contained in the research section and most of the illustrations used in this publication are provided by the faculty and graduate students conducting SRC-sponsored research. The remaining text is written by the technical staff of the SRC.*

*Marian Regan, Editorial Coordinator*

*This report is available to any interested person by requesting SRC Publication Number S91014.*

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