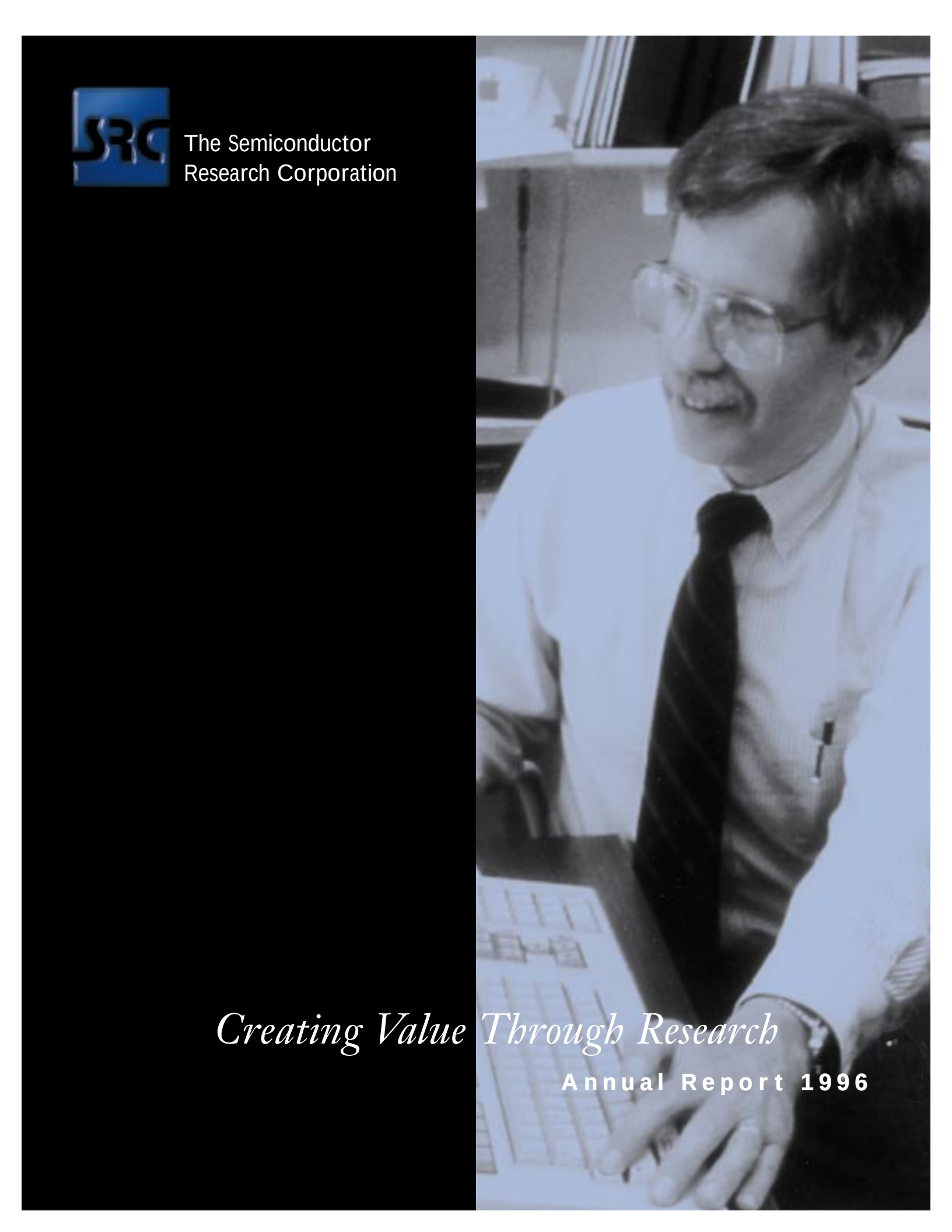

The Semiconductor
Research Corporation

Creating Value Through Research

Annual Report 1996

Vision

The Semiconductor Research Corporation (SRC) will be the world's premier research management consortium for providing university-based research results in semiconductor science and technology to its members.

Mission

As the research arm of the Semiconductor Industry Association (SIA), the SRC is a not-for-profit, tax-exempt research management consortium that helps solve the North American semiconductor industry's technical challenges, focusing on long-range university research.

Charter

The SRC manages a low-overhead, industry-driven, pre-competitive research program that addresses the research needs of the SIA's National Technology Roadmap for Semiconductors. Funding for this research is derived primarily from member fees. The SRC is not a government contractor; however, it does encourage government participation and funding support of key research programs.

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About the Cover

Dr. Stephen W. Director, recipient of the SRC's first Aristotle Award, is pictured at work. A magnified representation of the intricate art on the award is also shown. Formerly dean of engineering at Carnegie Mellon University, Dr. Director is now dean of the college of engineering at The University of Michigan.

Through superb teaching, mentoring and administration, as well as significant research activities of his own, Dr. Director has helped to create value in SRC-sponsored research. "By instilling his students with the creativity and technical skill necessary to succeed, and by exposing them to industry-relevant research, Dr. Director has helped shape future industry leaders," said Larry W. Sumney, SRC president and CEO.

The Aristotle Award was created by the SRC Board of Directors to recognize faculty whose deep commitment to the educational experience has had a profound and continuing impact on the professional performance of students who carry out SRC-funded research.

The Annual Report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC Research Program, present the formal financial report and provide information on activities and events of the SRC industry/government/university community for the previous calendar year.

This report is available to any interested person by requesting SRC Publication Number S97005.
A copy of this report and additional information about the SRC are accessible on the World Wide Web at http://www.src.org.

What is the SRC?

Titled "Hypothesis," the design of the Aristotle award is based on symbols derived from physics, chemistry, calculus and geometry that create the illusion of a complex three-dimensional scientific diagram. According to designer Robert Cassetti, "This is a window into the creative mind at work, where fragments of concepts and remembered phrases are recombined to form entirely new ideas."

As a consortium of nearly 50 North American companies and participating government agencies, the Semiconductor Research Corporation plays a crucial role in planning, directing and funding the semiconductor industry's pre-competitive, long-term research.

The SRC directs an integrated program of applied research, conducted by the faculty and graduate students at dozens of leading universities and research institutions across the United States and Canada. This program invests in research to benefit the entire industry and is funded by member organizations that view participation as a critical component of their long-term commercial success. The SRC program is the result of the vision, commitment and stewardship of many thousands of individuals over the history of the SRC and has proven to be an excellent and enduring model for cooperative research.

Value

Since its formation by the Semiconductor Industry Association (SIA) in 1982, the SRC has invested and managed more than $340 million in semiconductor industry funds for research. Throughout the 15 years of its existence, the SRC has made significant contributions that have yielded many benefits to member companies, including:

- High-quality university research on mainstream semiconductor technology carried out by hundreds of faculty members and several thousand students. The research, in turn, has created a strong university infrastructure on which member companies rely for a continuous source of new ideas and experts.
- Graduate students educated in areas relevant to the industry, a key objective of the SRC-sponsored research program. Through their research, as well as exposure to the scientists and engineers of member companies facilitated by the SRC Industrial Mentor Program, between 150 and 200 graduates enter the work force each year with strong backgrounds in microelectronics. These highly qualified professionals begin contributing to their companies' products almost immediately. The SRC accounts for approximately 10 percent of all electrical and computer engineering Ph.Ds granted in the U.S.
- Unified research goals addressing industry needs, incorporated into the SIA National Technology Roadmap for Semiconductors (NTRS).
- Timely and effective transfer of research results to SRC participants for further development and commercialization.
- Publication and archiving of more than 8,000 research reports created by SRC-sponsored researchers.
- More than 1,000 SRC-sponsored technical conferences and workshops in which new technologies and concepts are communicated.

In all of its endeavors, the SRC strives to maximize the *value* to the collective membership by being a world-class research consortium. Member companies derive maximum value from the consortium by tailoring the impact of SRC outputs and results to members' own business parameters and critical success factors. These value parameters may include one or more of the following:

- Lower R&D costs (and, therefore, improved profitability) due to leveraged research programs, in which the cost of the research programs is shared among the members, redundant funding of early research is avoided and low-overhead, cost-effective research management is achieved through the SRC and the associated advisory boards.

SRC university research develops human capital for the semiconductor industry.

- Acceleration of internal technology roadmaps due to early and easy access of SRC-sponsored research results and hiring of the relevantly educated students. This, in turn, allows member companies to execute their own internal new products in an accelerated manner, and, hence, enjoy strong market shares.
- Minimization and prudent management of risks through collective research management (portfolio effect) within the framework of the consortium.
- The university infrastructure has created a pool of strong faculty members, knowledgeable in industry's current and future needs. This pool provides a cost-effective source of expertise for solving the member companies' unique and specific problems through consultations and other interactions.
- The myriad of interactions at multiple levels that occur naturally through the participation in the SRC and its activities provide member companies opportunities for networking. This results in the infusion of new and different perspectives, both at the R&D and business levels, which is vital for the business health of members.

Robert Sumners (left), a graduate fellow at the University of Texas at Austin, talks with current SRC board of directors chair Don Wollesen (right) of AMD at the TECHCON '96 awards banquet.

Message from the President

Larry W. Sumney

The semiconductor industry is poised to realize growth again, while its products and challenges become ever-more complex. Global competition... economic pressures... work force shortages... compressed product life cycles... and shrinking transistors: The industry is grappling with major challenges as it hurtles toward the 21st century.

At the SRC, we're helping to find solutions to technology roadblocks that lie ahead for our industry. While some issues, such as the need to reduce expenses, must be confronted by almost every industry today, issues like whether the laws of physics will one day halt the advancement of transistors are unique to our business.

Research undoubtedly plays a critical role, not only in breaking through roadblocks but also in finding ways to extend current technology to meet nearer-term needs. SRC's research is directed toward both types of research, and in this annual report, you will find many examples of how the SRC is *creating value through research* for its members and the entire industry.

Value in Member Services, Science Areas and Student Support

The SRC added value for members through a number of programs and events during 1996. For example, we altered our budget processes to allow higher fee-paying members to allocate a portion of their SRC fees to specific research programs or areas. This customization option is a major step toward increasing customer satisfaction.

We continue to refine the strong, collaborative research program that reaps cost-effective, practical rewards for the industry. For example, Professor Bill Oldham's lithography work at Berkeley saved the industry millions of dollars in equipment purchases. Highlights of our 1996 research results can be found in the research management section of this report. For complete details of all SRC research projects, see our Research Catalog on the World Wide Web (www.src.org).

Last year, we also presented the first Aristotle Award to Dr. Steven Director. This award recognizes outstanding teaching in its broadest sense, especially during the research project. Some members tell us that educating students is one of the most important benefits the SRC offers. Through inspiring educators like Dr. Director, the SRC is developing the human resources of our industry.

Value in New Research Undertakings: MARCO

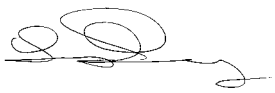
As we celebrate our 15th year in 1997, the SRC has entered a new era with the formation of an SRC subsidiary: the Microelectronics Advanced Research Corporation, or MARCO. The concept of MARCO was realized in 1996. Last year, the SIA, SEMI/SEMATECH, the federal government and the SRC decided to create this new U.S. university research organization that will initiate and manage long-range silicon research to address technology gaps articulated in the National Technology Roadmap for Semiconductors.

It is intended that MARCO conduct a "Focus Center" research program to undertake applied research at U.S. universities in key areas of semiconductor technology; enhance the capabilities of selected universities to conduct such research; and facilitate the dissemination of the research results to MARCO participants in the Focus Center program and the U.S. semiconductor industry.

Focus Centers will be expected to generate new options and ideas. Part of the role of the SRC will be to narrow and direct research on those options. Continuing the technology-transfer process when appropriate, SEMATECH will begin pre-commercialization.

Clearly, the SRC cannot celebrate its 15th year by becoming complacent. It is important, though, to recognize our advancements as the research arm of the semiconductor industry. Please take a few minutes to read the details of the SRC's 1996 events and accomplishments. I think you will find that we are truly *creating value through research.*

Sincerely,



Larry W. Sumney
President & CEO

1996 SRC Accomplishments

SRC Initiates New Information Avenues and Research Centers

"TECHCON '96 offers a forum for experiencing the synergy between the wide range of disciplines that constitute the semiconductor industry — from materials and processes to computer-aided design, to modeling and simulation, to packaging and interconnects — with a focus on long-term needs as defined by the National Technology Roadmap for Semiconductors (NTRS)."

Charles Carinalli
1996 Chairman, Board of Directors and Honorary Conference Chair, TECHCON '96

TECHCON '96 Receives Rave Reviews

TECHCON '96, the SRC's fourth national research conference, was rated by participants as "the best ever." In post-conference evaluations, participants gave the event held in Phoenix, Arizona, high marks for the valuable information presented, as well as for opportunities to network and interact with other semiconductor scientists and engineers. More than 500 scientists and engineers from industry, university and government attended TECHCON '96 in mid-September.

Dr. Pallab K. Chatterjee, president of Personal Productivity Products at Texas Instruments Inc., delivered the keynote address, titled "Start Doing Extraordinary Things with Mobile Computing on Gigachips Digital Signal Processing Solutions." Dr. Chatterjee described future opportunities offered by technologies to be gleaned from the research presented at TECHCON. He emphasized "mobile technology" and its impact on society. Gigachips Digital Signal Processing Solutions, and mobile technology in general, depend on research in semiconductor technology for their rapid evolution and assimilation.

TECHCON '96 organizer Jim Freedman (right), SRC's vice president, research integration and technology transfer, recognizes Ashok Kapoor (left) of LSI (now with National Semiconductor) for co-chairing the Executive Technical Advisory Board (ETAB).

Jim Duley of Hewlett-Packard judges posters entered in the Design Sciences area competition at TECHCON '96.

For the first time, the SRC sponsored "Jobs-Fair" after the official closing of TECHCON conference sessions. Fourteen company booths provided backdrops as industry representatives matched highly qualified students with specific opportunities. "Usually at a recruiting fair we have 500 students, and we will be interested in only five or 10," commented one recruiter. "Here, we have 150 students, and we're interested in all of them."

TECHCON's technical sessions, which covered the seven SRC science areas, featured 128 presentations by SRC-funded graduate student researchers. Continuing as a major highlight of the conference, TechFair offered approximately 150 poster sessions and several software demonstrations. TechFair also included well-attended birds-of-a-feather discussion sessions that covered SRC and the World Wide Web, intellectual property, mentoring and student needs and services.

Because of the strong positive feedback TECHCON '96 received, the SRC is going to sponsor this event every two years, instead of every three years. The fifth TECHCON is planned for 1998 in Las Vegas.

The SRC Goes Online

The SRC World Wide Web site debuted in 1996 at www.src.org. Far beyond a simple corporate home page, the SRC web site is a robust presentation of substantive information about research progress and results. Whether users enter the site from the table of contents, via the Research Catalog, or through a search query, they soon discover valuable technical information in the form of journal pre-publications, reports, event schedules and participant profiles.

In keeping with SRC tradition, the web site focuses on technology transfer. As a result of this emphasis, the 1996 Research Catalog became the centerpiece of the integrated SRC web site. The web-enabled Research Catalog summarizes research plans and activities and serves as a pointer to details about research results in progress, as well as the people involved in the research.

While member company engineers are its primary audience, the SRC web site attracts others as well. The general public, government officials and executives at potential new member companies can all use the public-level information from the site. Visitors can access overviews, historical information and targeted feature articles.

The SRC is developing ways to use the web site to improve SRC's interaction with university researchers. Also in the plans are links to the web sites of the larger member companies to provide mirrored web sites for internal corporate access. SRC continually looks for new ways to expand the depth and scope of the Internet information offered and to enhance the technology transfer provided to the SRC community.

New Programs Address Technical Challenges

In 1996, the SRC launched several initiatives to address some of the technical challenges members must overcome to sustain the National Technology Roadmap for Semiconductors (NTRS) schedule. Mindful of maximizing value to members, the SRC enlisted the joint sponsorship of federal and state agencies to leverage membership benefits in each initiative described here.

Yates Sorrell, a N.C. State University professor, accesses SRC's World Wide Web site at TECHCON '96.

Center for Advanced Interconnect Science and Technology (CAIST)

The semiconductor product and technology evolution is increasingly encountering performance limitations caused by the interconnection parasitics. Significant and discontinuous changes in the interconnect material system are mandated in order to continue on the path of the NTRS. In recognition of this need, the Center for Interconnect Science and Technology (CAIST) was launched in 1996. Based at the Rensselaer Polytechnic Institute, Troy, N.Y., this new five-year joint venture with the state of New York coordinates research conducted in cooperation with the following universities: Clarkson University, Cornell University, Georgia Institute of Technology, State University of New York at Albany, University of North Texas and University of Texas at Austin. The center is aimed at addressing the critical new interconnect material systems needs of SRC members (and of the semiconductor industry) through:

- Development of scientific underpinnings of the technologies, models and the material systems required to support the NTRS
- Educating relevantly trained scientists and engineers who will help implement these technologies in the industry.

The CAIST is primarily engaged in research in two categories: (a) improvements in electron transport in existing, as well as new conductors and associated field effects in nearby dielectrics, and (b) early, critical exploratory work in advanced non-electron transport realization of interconnections. The research thrusts include thin-film processes for low-resistivity; low-cross-talk multi-level interconnect material system; modeling and simulation; performance and reliability; metrology; and innovative concepts for new interconnect technologies.

SRC/NSF ERC in Environmentally Benign Semiconductor Manufacturing (CEBM)

The National Science Foundation (NSF) and the SRC initiated the Engineering Research Center (ERC) for Environmentally Benign Semiconductor Manufacturing, a unique partnership to study the environmental, health and safety aspects of the semiconductor manufacturing process. The NSF/SRC center is at the University of Arizona and coordinates research conducted cooperatively at the following universities: Arizona, Massachusetts Institute of Technology, Stanford University and the University of California at Berkeley.

The research is focused on two of the most critical challenges faced by the industry in the manufacture of advanced integrated circuit products: (a) reduction of large amounts of high purity water and (b) alternative chemistries to eliminate or reduce hazardous materials. Research in these areas is targeted to arrive at cost-effective, competitive and environmentally benign approaches to meet these challenges. CEBM research thrusts include plasma processes (PFCs, CVD and Sensors), non-plasma processes (removal, clean, and etch), water conservation (recycling and reuse), exploratory work in chemical mechanical polishing (CMP) and resists. The center emphasizes an interdisciplinary approach to education. ERC graduates will be a part of a new generation of engineers, capable of integrating environmentally-conscious concepts in the design of manufacturing processes.

SRC/DARPA Advanced Lithography Initiative and Network

This four-year joint venture with the Defense Advanced Projects Agency (DARPA) seeks to identify promising approaches to lithography for the generations of devices requiring feature sizes below 100 nm. Members may be able to use the results to reduce risks associated with prototype decisions.

The initiative is exploring new breakthrough research to enable step function advances in manufacturing and interfacing infrastructure technologies. Research thrusts include extreme ultraviolet (EUV) lithography, E-beam lithography, maskless lithography, precision wavefront metrology, sub-100 nm alignment and placement, resist synthesis and modeling, and CAD and Simulation Tools.

Center for Semiconductor Modeling and Simulation (CSMS)

CSMS develops modeling and simulation tools that will shorten process and product development cycles. Cycles are shortened through a highly accurate modeling and simulation hierarchy that reduces the need for experimental confirmation for devices with a minimum feature size below 100 nm. The center is a partnership among 10 SRC-member companies, Los Alamos National Laboratory (LANL), Sandia National Laboratory (SNL), Lawrence Livermore National Laboratory (LLNL) and 12 universities.

Launched in mid-1995, CSMS expanded operations in 1996. Among new developments, LANL released X3D, a powerful adaptive gridding code, to participating member companies. Members are already applying the research to current generation process modeling. In addition, Professor Al Tasch's work at the University of Texas resulted in improvements to the ion implantation modeling software UT MARLOW. Also, Professor Timothy Cale, Arizona State University, developed enhancements to the popular wafer topography simulator EVOLVE V.

Customization Program

Also in 1996, the SRC initiated a program to enhance member benefits by allowing qualified SRC members to allocate a fraction of their dues to the direct support of research projects selected exclusively by that member. These "customized projects" are managed by the SRC on behalf of the entire membership in accordance with standard procedures; all research results are shared by the membership. The program is being implemented in 1997.

SRC Members and Participants

The SRC's strength is its ability to bring industry relevance to university research and to transfer research results quickly from universities and research organizations to the industry for commercialization. The SRC's participating companies, organizations and government agencies make technological advances possible. About 50 companies and government agencies fund the SRC's work to leverage their research and development dollars and to obtain substantial returns on their investment.

Members

Advanced Micro Devices, Inc.
Digital Equipment Corp.
Eastman Kodak Co.
Harris Corp.
Hewlett-Packard Co.
IBM Corp.
Intel Corp.
LSI Logic Corp.
Lucent Technologies
Motorola Inc.
National Semiconductor Corp.
NORTEL
Northrop Grumman
Texas Instruments Incorporated
Westinghouse Electric Corp.

Science Area Members

Alcoa
Cadence Design Systems
E-Systems, Incorporated
E. I. du Pont de Nemours & Co.
ETEC Systems
Eaton Corp.
Ford Motor Co.
Novellus Systems Inc.
Shipley Co.

Associate Members

Lawrence Berkeley National Laboratory
Lawrence Livermore National Laboratory
Los Alamos National Laboratory
Microelectronics & Comp. Tech. Corp.
Oak Ridge National Laboratory
SEMATECH
Sandia National Laboratories
The MITRE Corp.

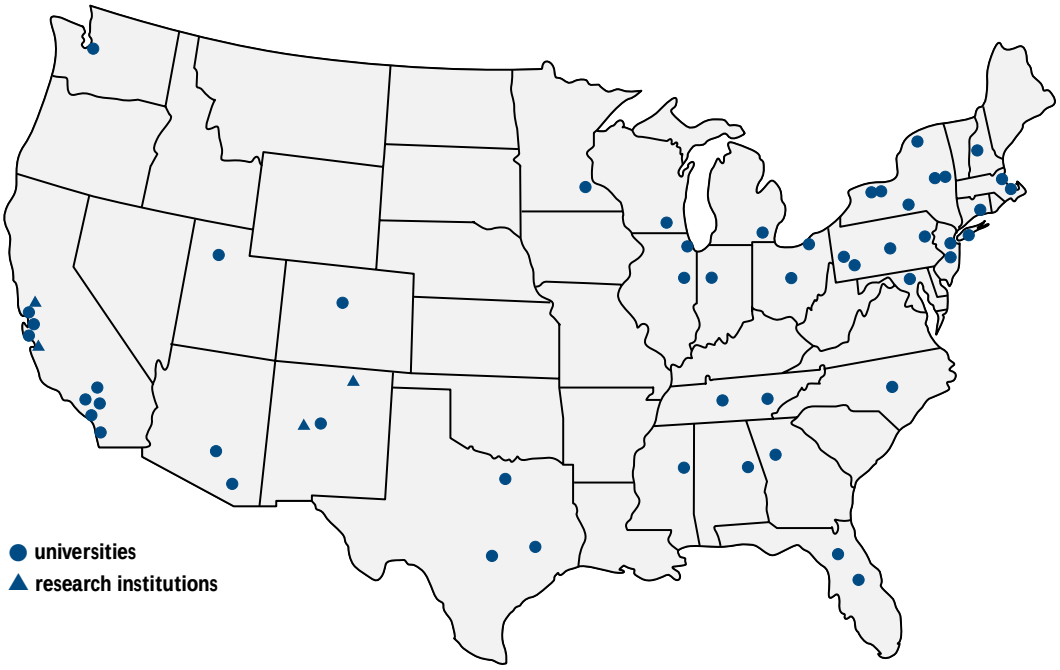
Affiliate Members

AG Associates
ANACAD Electrical Eng. Software
BTA Technology, Inc.
CVC Products, Inc.
Dawn Technologies, Inc.
DesignAid, Inc.
Emergent Technologies Corp.
Famtech/Speedfam Corp.
Hestia Technologies, Inc.
Ibis Technology Corp.
Integrated Electronic Innovations
Integrated Silicon Systems, Inc.
IntelliSense Corp.
LV Software, Inc.
Meta-Software, Inc.
MicroUnity Systems Engineering, Inc.
Mission Research Corp.
OEA International, Inc.
OMNIVIEW, Inc.
PDF Solutions, Inc.
Process Technology Ltd.
Q-metrics, Inc.
SILVACO Data Systems
SiBond, L.L.C.
Solid State Measurements, Inc.
Solid State Systems, Inc.
Technology Modeling Associates, Inc.
Techware Systems Corp.
Tyecin Systems, Inc.
Verity Instruments, Inc.

U.S. Government Participants

National Institute of Standards and Technology
National Science Foundation
National Security Agency
Office of Naval Research
U.S. Army Research Office
Wright Laboratory

SRC Participating Universities and Research Institutions



Arizona State University
Auburn University
Boston University
California Institute of Technology
Carnegie Mellon University
Case Western Reserve University
Clarkson University
Cornell University
Duquesne University
Georgia Institute of Technology
Lawrence Livermore National Laboratory
Lehigh University
Los Alamos National Laboratory
Massachusetts Institute of Technology
Mississippi State University
Monterey Institute for International Studies
North Carolina State University
Northwestern University
Polytechnic University
Princeton University
Purdue University
Rensselaer Polytechnic Institute
Rochester Institute of Technology
Rutgers University
Sandia National Laboratories
Stanford University
State University of New York at Albany
Texas A&M University
The Ohio State University
The Pennsylvania State University
The University of Michigan
University of Arizona
University of California at Berkeley
University of California at Irvine
University of California at Los Angeles
University of California at San Diego
University of California at Santa Cruz
University of Central Florida
University of Colorado at Boulder
University of Florida
University of Illinois at Urbana-Champaign
University of Maryland
University of Minnesota
University of New Hampshire
University of New Mexico
University of North Texas
University of Rochester
University of Southern California
University of Tennessee
University of Texas at Austin
University of Utah
University of Washington
University of Wisconsin
Vanderbilt University
Yale University

Research Management

SRC Research Portfolio Yields Technological Advances

A recap of 1996 would be incomplete without mention of the retirement of Robert M. Burger.

"Bob Burger has been a driving force behind the establishment and growth of the SRC, and his many achievements have helped bolster the North American semiconductor industry as a whole," said Larry W. Sumney, SRC president and CEO. "Bob's expertise will be missed, but the legacy of his actions on behalf of the SRC and the industry continues to resonate. Under his steady leadership, the SRC's program of university-based cooperative research has grown from a seminal idea into a network of world-class research, laden with technology-transfer opportunities."

Shortly after joining the SRC as its third employee in 1982, Burger organized the first Technical Advisory Board (TAB) to involve industrial members in guiding and directing SRC-funded research. Today, the SRC's many TABs give scientists and engineers from industry and government a chance to work closely with SRC science area directors and senior staff. Together they plan research and direct it to areas of industry need.

SRC members are accelerating the time line articulated by the 1994 National Technology Roadmap for Semiconductors (NTRS). The SRC has played an important role in supporting the success of its members by creating and maintaining a vibrant university research program. This research base is becoming even more critical because maintaining the future progress at the Moore's Law cadence, as articulated by the NTRS, will require sweeping changes in the technology base of the IC industry.

En route to the 100 nm technology node, industry will require new material systems for interconnect lines, for interlevel dielectrics and for transistor-gate dielectrics. A post-optical patterning capability must be developed for future technology nodes. Increased levels of integration in products will demand substantial improvements in design productivity and effectiveness to meet product development cycle time challenges. Cost containment is essential for capital and operation of future generations of IC factories. New device structures, innovative high performance circuit architectures that operate at low voltages with reduced power, low-cost and low-volume fabrication technologies, and design and fabrication of system-level packaging architectures are some of the challenges that must be met as the industry progresses to 100 nm and finer technology nodes.

By judiciously managing the research portfolio, as well as exploiting opportunities for cross-disciplinary synergism, the SRC helps to ensure that challenges to advance technology are met in a cost-effective manner. While the industry has de-emphasized research in light of financial constraints, the SRC has continued to provide research and technology transfer to help members face the considerable challenges of global competition. The foreshortening of research horizons has made it even more important for its members to participate in the SRC program.

Program Overview

The SRC manages research in seven science areas: (1) Design, (2) Packaging, (3) Process Integration and Device, (4) Materials and Bulk Processes, (5) Interconnect, (6) Lithography and (7) Factory. A Science Area Technical Advisory Board (STAB) advises each of the science areas, and an Executive Technical Advisory Board (ETAB) oversees the entire research program.

Design Sciences provides research leadership in electronic design and design automation for silicon micro-systems. The design landscape is highly dynamic due to the greatly increased complexity of emerging products and the concomitant need to define a design within an increasingly constrained design space. Integrated circuits must meet specified levels of functional and performance requirements, reliability requirements, and requirements of manufacturability and testability.

Packaging Sciences research program deals with challenges posed by the stringent requirements for the package to remove heat generated by higher-speed and increased-density ICs while maintaining high reliability at operating temperatures. It seeks to provide the information, tools and methodologies for the design and fabrication of packaging structures to satisfy the electrical, thermal/mechanical and reliability requirements of future packages.

Process Integration and Device Sciences is concerned with the semiconductor device itself, as well as the physics and chemistry of novel processes. Its strategies are to (a) shift the focus of device technology from a lithography-dependent, standard shrink approach by introducing creative structures and process architectures; (b) provide improved predictive modeling; (c) conceive circuit elements that are yield-tolerant of manufacturing defects and parameter variations; (d) seize the opportunities for paradigm shifts to circumvent current technology limitations.

Materials and Bulk Processes Sciences includes the front-end of the fabrication process and starting materials for mainstream integrated circuit manufacture. Included are the tools and processes used to fabricate the structure up to the active silicon surface and the thermal processes and depositions of active films above the surface, such as gate electrodes, elevated source/drain materials and silicidation. Research in this science area focuses on: (a) materials characterization and analysis; (b) gate dielectrics and field oxides; (c) bulk processes; (d) gate-stack cluster tools; and (e) modeling and simulation.

Interconnect Sciences focuses on research programs that address (a) reduction of parasitic via integrated copper/low dielectric permitivity insulators and chemical mechanical polishing (CMP); (b) new types of dry-plasma etching sources, processes and plasma diagnostic methods; (c) improvement in interconnect reliability; (d) surface and interface materials science; and (e) advanced modeling and process simulation.

Lithography Sciences manages research that will enable the production of robust lithographic materials, processes, control methodologies and process tools with the capability to produce integrated circuit patterns through the early part of the next century. The primary goal of lithography is to transfer patterned features reproducibly. Orders-of-magnitude improvement in metrology capability are required to provide nondestructive, *in situ*, real-time measurements at the dimensions specified in the NTRS.

Factory Sciences research focuses on the continued evolution of advanced integrated circuit manufacturing, with a paramount goal of maximum competitive advantage through reduced manufacturing costs and cycle times.

1996 Research Highlights

Following are a few sample SRC research projects that directly benefited members in 1996. These projects illustrate the comprehensive scope of the SRC research program and range from detailed improvements in materials and device structures to processes and equipment control and IC and package design. Members can find full descriptions of all SRC research projects in the Research Catalog on the SRC World Wide Web site.

Design

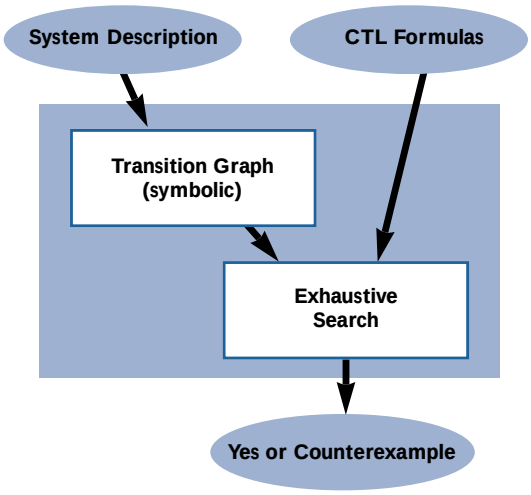
Verification Interacting with Synthesis (VIS): This new system, developed by Professor Robert Brayton and his University of California at Berkeley team, integrates sequential logic synthesis with formal verification in a consistent tool environment. Using these tools, designers can manipulate complex hierarchical designs and efficiently explore implementation options while maintaining consistency and correct design. The combination of verification and synthesis results in more efficient designs that are verifiably correct. An important benefit of the open structure of VIS is that new tools and algorithms can be developed and studied in an existing tool environment. Several universities are working with the Berkeley team to transfer new ideas to the design community rapidly through VIS.

Word-Level Model Checker (WSMV): Prior to this research, it was difficult to prove the correctness of arithmetic operations. The inability of debugging techniques like simulation to find all errors resulted in delays in getting new products to market, as well as failure of devices already in use.

This prototype tool, released late in 1996, extends the reach of symbolic model checking to encompass arithmetic data types, rather than simply Boolean data. Developed by Professor Edmund Clarke's team at Carnegie Mellon University, the tool has been used to provide formal verification of complex CPU modules in commercial environments.

Members now using the tool enjoy significant cost and risk avoidance in product development. In addition, many companies are investigating the possibility of internal use in the development and debugging of microprocessors.

Figure 1: SMV Model Checking System



Colorado University Decision Diagrams (CUDD): Professors Gary Hachtel and Fabio Somenzi at the University of Colorado-Boulder developed this new package of support software. CUDD provides fundamental building blocks for many CAD tools in synthesis, verification, test generation and layout. As the most advanced decision diagram manipulation routines available anywhere, CUDD is being used by leading electronic design automation (EDA) vendors and universities alike (including the VIS system noted above).

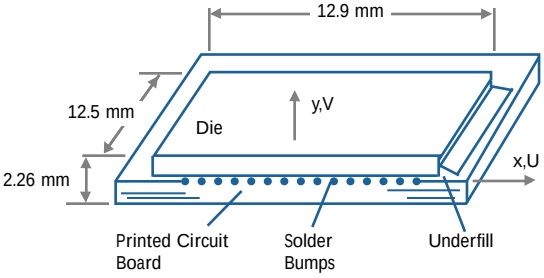
Taken as a class, formal verification tools like VIS, WSMV and CUDD represent a major paradigm shift in design technology. Using them increases the assurance that complex designs will achieve their specifications without error, thereby reducing iterations and improving design productivity. Ultimately, these tools will help decrease time to market and improve profitability.

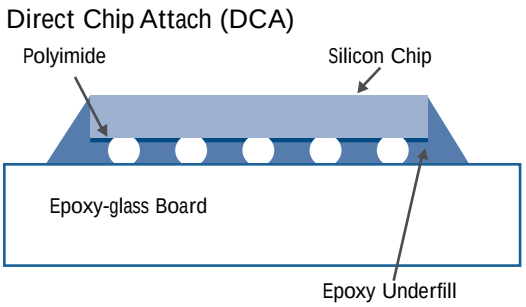
Illinois Thermal-Electrical Modeling (iTEM): Professors Steve Kang and Elyse Rosenbaum at the University of Illinois-Urbana/Champaign found that iTEM can estimate the interconnect temperature rise due to Joule heating and heat conduction from the substrate, using a newly developed lumped thermal model. By including temperature effects, iTEM greatly improves electromigration reliability diagnosis compared with existing tools. Because of the efficiency of the algorithms, it can analyze circuit layouts containing tens of thousands of transistors, using only a desktop workstation. As process technologies rapidly move to deep submicron levels, interconnect reliability will become a crucial factor limiting design density. Tools like iTEM promise to increase confidence in design calculations and allow maximum use of process technology without compromising product reliability.

Packaging Sciences

Thermal and Mechanical Characterization of Thin-Film Polymer Packaging Materials: Much of the SRC packaging research has focused on methods and tools for the thermal and mechanical characterization of the packages and the effect of material variation on package strain in normal-use conditions. One of the most visual methods, developed by Professor Paul Ho and his team at the University of Texas at Austin, is the analysis of horizontal (U) and vertical (V) deformation displacements as they are displayed using Moire Interferometry. The package format analyzed is direct chip attach (DCA). The Moire analysis yields the U and V displacement under the influence of thermal change. The package is shown schematically in Figure 2.

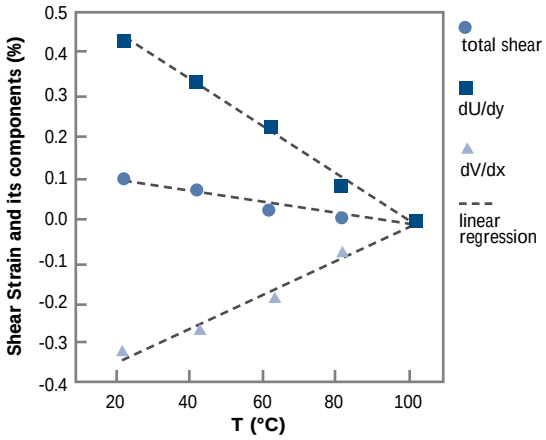
Figure 2: Schematic Drawing of the Underfilled Flip Chip on Board Package





The team investigated the effect of the underfill material on the total shear strain that is realized at the interface between the die and the substrate (the polymeric printed wiring board). To ensure package reliability, the net stress on the solder interconnects must be as low as possible to avoid solder fatigue. The researchers found that the shear component dU/dy (derived from the U displacement) caused by thermal mismatch between the die and the substrate is canceled by the shear component dV/dx due to the bending of the package induced by the underfill. This cancellation leads to a significant reduction of the total shear strain shown in Figure 3.

Figure 3: Total Shear Strain and Its Components across the Rightmost Solder Bump as Functions of Temperature



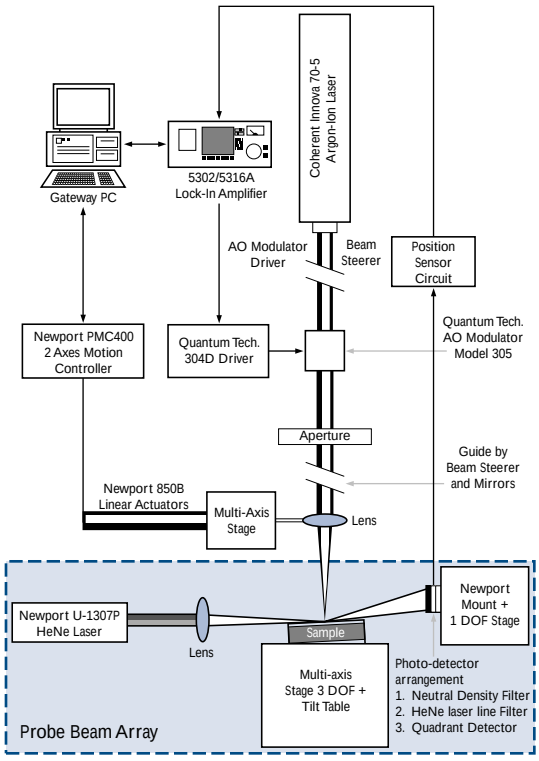
This work is significant because it displays deformation displacement of material within an actual package. Using this analysis, researchers determined the impact of polymer underfill characteristics and the fraction of fill material on package reliability. This analysis technique will be extended to new materials and new configurations within the DCA package.

Interface Adhesion of Packaging Materials: The DCA package is a series of interfaces; good bonding of these interfaces is critical to the reliable performance of electronic systems incorporating them. Lehigh University investigators, led by Professor Ray Pearson, characterized adhesion between material when subjected to thermal and environmental stresses. Several member companies are applying the results of this work.

Thermal Measurements with Photothermal Deflection Spectroscopy (PDS): The measurements of thermal properties of packaging materials has grown increasingly important as the thermal dissipation of chips has become more severe. The thermal properties of many currently used packaging materials and thermal management techniques are inadequate for use with a high-wattage (60 W) chip. Professor Thomas Avedisian and his team at Cornell University have developed a method for measuring thermal diffusivity in a non-intrusive, easily-implementable manner. This method, called photothermal deflection spectroscopy (PDS), is illustrated in Figure 4.

The Cornell team has worked with the National Institute of Standards and Technology (NIST) to validate the method, using national standards. Using this analytical method, Dr. Avedisian is working with several member companies on design of high-efficiency, high-performance heat spreaders.

Figure 4: Schematic of Photothermal Deflection Spectroscopy (PDS)

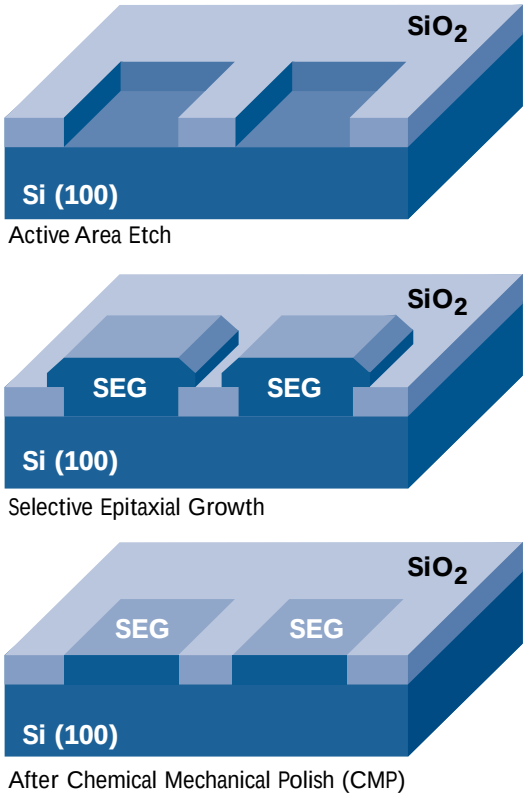


Process Integration and Devices

Cost-of-Ownership Models for Selective Epitaxial Growth: Devices fabricated by selective epitaxial growth (SEG) into dielectrically isolated wells and the eventual epitaxial lateral overgrowth (ELO) along the surface offer the following advantages: improved isolation, better self-alignment, increased packing, and novel structures and applications. To improve mainstream business operations, however, these processes must also have high yield and produce an equivalent, or lower, "cost of ownership" (COO) when compared with standard options. Professor Gerold Neudeck's research at Purdue University has addressed the yield issues associated with stress. More recently, independent assessments by SRC-member companies have shown that SEG/ELO also provides costs savings. Savings result from the elimination of standard processes associated with "well" formations and reduced equipment utilization. The COO model provides a green light for introducing these processes into the mainstream.

Order-of-Magnitude Reduction in Source-Drain Specific Contact Resistances: A critical issue in all device structures is the paths by which current is supplied to and extracted from the device. Between materials (e.g., metal or metal silicide with silicon) there is an interface, and this interface barrier can be represented by a parameter designated as the "specific contact resistance," with units of Ohm-cm^2. The interface resistance increases if the overall interface area is decreased. As devices shrink, the available contact area decreases, as does the on-resistance of the device.

Figure 5: Illustration of SEG



By using an intermediate region of selective SiGe between the metallization and the silicon, research conducted by Cornell University, and co-aligned with previous research at N.C. State University, has demonstrated low leakage, shallow (raised) junction depths of 30 nm, as well as lowered interface barriers that reduce the specific contact resistance by more than an order of magnitude.

This research can help SRC-member companies reduce risks associated with high contact resistance and improve overall performance of their devices.

Materials and Bulk Processes

Jet Vapor Deposited (JVD) Silicon Nitride Films as Gate Dielectrics: Silicon oxide has been the mainstream choice for the control-gate oxide dielectric since the birth of the silicon MOSFET. As devices have shrunk, silicon oxide has continued to meet reliability, quality and performance specifications. Today, reliability issues related to oxide defects, dopant (boron) diffusion from the gate and leakage associated with the thinness of the dielectric are prompting research into alternative processes and materials. A Yale University team led by Professor C.T. Ma has explored one of these processes, known as jet vapor deposition (JVD).

Employing a supersonic jet flow, JVD provides columnar deposition; compositionally adjustable films; avoidance of normal chemical vapor deposition (CVD) products (such as the insertion of excess H, OH, or H_2O); and low temperature with additional bonding provided by He bombardment. Silicon nitride films are easily deposited by JVD and show electrical characteristics significantly superior to CVD. The dielectric constant for silicon nitride is higher than silicon oxide, so that even thicker films give better device performance. Leakage currents are low, while boron diffusion is undetectable. SEMATECH is now advancing the technology transfer.

This research provides considerable cost savings to SRC members by avoiding certain contaminants and providing higher quality films. It also offers improved quality/reliability and a significant reduction in risk associated with future technology.

Ultra-Shallow Junctions by Means of Low-Energy Implants: The lowest energies of today's standard ion implantation machines cannot provide needed shallow junctions. While the industry has considered various alternatives, the best option is to extend today's technology to lower energies. Research directed by Professor Sanjay Banerjee at the University of Texas at Austin is exploring the unique process control issues associated with lower-energy implants, as well as the physics of dopant and point-defect interactions with the silicon surface. These surface interactions also affect the subsequent Technology Computer-Aided Design (TCAD) modeling of the dopant and the dopant-defect pair diffusion.

The value of this research to member companies is cost avoidance, guidance to ion implant vendors and improved TCAD models for the device/process engineer.

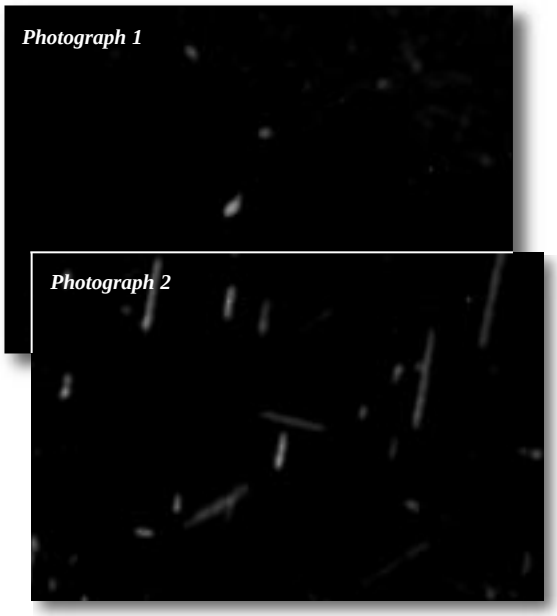
TCAD (Technology Computer-Aided Design) Portfolio for TED (Transient-Enhanced Diffusion) Modeling: This portfolio represents an aggressive, synergistic, cooperative plan among seven professors, with a shared "roadmap" for attacking both near- and long-term TCAD issues associated with Transient-Enhanced Diffusion (TED). The professors who cooperated in the research are Professors Mark Law and Kevin Jones of the University of Florida; Professor James Plummer of Stanford University; Professor Dim-Lee Kwong of the University of Texas at Austin; Professors Paulette Clancy and Michael Thompson of Cornell University; and Professor Scott Dunham of Boston University.

TED is one of the most critical process-control issues for the industry because it affects junction depths, channel lengths, thresholds and sub-threshold and leakage performance. An original implant of dopant produces point defects (interstitials and vacancies) that may either directly recombine, or mate with dopant atoms in a pairing reaction, or eventually coalesce into extended crystalline "{311}" or "loop" defects. Depending on the species, the original point defect-assisted diffusion coefficients may be 10,000 times greater than in an equilibrated bulk. These point defects rapidly disappear, but the coalesced loops gradually dissolve and can result in effective diffusion coefficients that are 100 times greater.

The final TED effects depend not only on dopant type, energy and concentration, but also on the existing dopants in the substrate (dopant-dopant pairing), temperature and dose rate at implant, dwell time at temperature and transition time (ramp rate) between temperatures.

The TCAD also defines and models optimum processes. Multiple dependencies require the assemblage of much data, special test structures and detailed diagnostics that confirm the models. Through use of these models, member companies can optimize the process parameters through simulations, thus avoiding excessive costs associated with experimentation (achieving lower development costs). The models can also help improve process control and therefore yields (reducing manufacturing costs).

photographs by Susan Earles, graduate student



The photographs show Transmission Electron Microscope Images {311} silicon defects. Both samples received an implant of 10^{14} cm^{-2} 80keV silicon and were annealed for 740°C for 40 minutes. **Photograph 1** is after a subsequent eight-hour anneal at 680°C, and **Photograph 2** is for a 15-hour anneal at 680°C. These defects decay and release interstitials, which give rise to transient enhanced diffusion of doping profiles.

Interconnect

Advanced Theoretical Characterization of Helicon Plasmas: A University of California at Los Angeles team directed by Professor Frank Chen has performed highly rigorous theoretical characterization of key phenomena in the physics of large-area helicon plasmas. The research impacts both tool and chip manufacturers that deploy helicon plasmas in low-damage manufacturing regimes. These calculations provide detailed numerical results on helicon-wave effects, energy and momentum transport of charges associated with the plasma, and evolution of the densities of reactant species. The team confirmed the calculations with experimental plasma-probe data.

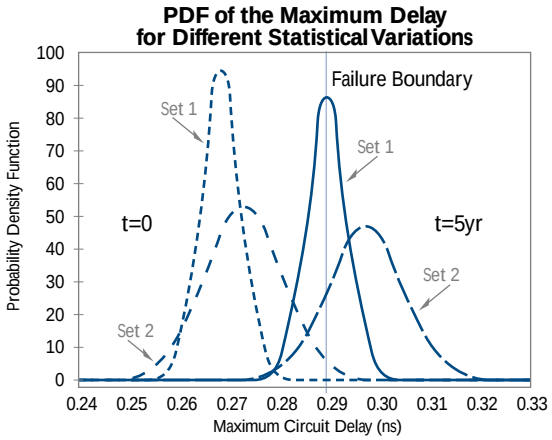
Key relations between plasma variables, tool configurations and process conditions derived in this work will enhance the efficiencies of tool and process control (important for tool makers), as well as lower probability of plasma damage to the chips etched with helicon plasmas and, hence, superior reliability of the products (important for chip makers).

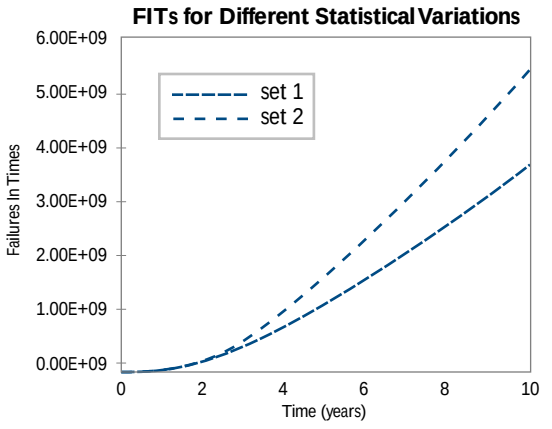
Soft Metal Chemical Mechanical Polishing: While the primary focus of the research agenda in the Center for Advanced Interconnect Science and Technology (CAIST) is on the copper family of technologies, discoveries have also been made in the chemical mechanical polishing (CMP) of aluminum. CAIST Director Professor Shyam Murarka and the team at Rensselaer Polytechnic Institute have produced research findings that will lead to scratch-free CMP of the rather soft aluminum, which is the current industry standard for metal interconnects. As the industry implements its various strategies to transition to the copper/low k generations of interconnects, it may take various interim steps with aluminum damascene structures. In such interconnect structures, scratch-free CMP of aluminum will be an important and indispensable processing capability. The results of this significant research will allow implementation of the interim steps, resulting in cost avoidance and improved reliability of products made with these steps.

Reliability Modeling and Forecasting: Professors Sherra Kerns and Bharat Bhuva at Vanderbilt University are leading a research team to address urgently needed advancements in reliability modeling with statistical circuit forecasting that effectively takes into account: a) the degradation of the devices exposed to plasma processing and subsequently exercised statistically by their ambient circuits; b) the unique contributions to reliability from interconnect modalities; c) the input "test" vectors; and d) the reliability failure criteria.

Figure 6: Forecast Failures in Time (FITS) for Different Mobility Statistics for a Specified Failure

Parameter Varied: Statistical Information
Parameters Sets: Set 1 (o(Vt) = o (Mobility) = 5%
Set 2 (o(Vt) = o (Mobility) = 10%





Statistical variation for device-level parameters is crucial in determining circuit reliability.

This work relies on an effective interaction with Sandia National Labs for advanced ultra high-frequency testing. While the work has been developed primarily for devices interconnected with aluminum/oxide dielectric structures, it could play a very important role in providing early reliability forecasts and assessments for contemplated copper/barrier/low k interconnect structures. This role could be a significant value-adding aspect of the research as the industry embarks on the challenging transition to the copper family of interconnect technologies. Indeed, by working closely with the research team conducting the copper-based research at the CAIST, Vanderbilt researchers have been able to evaluate their approaches to comprehend as early as possible the critical reliability features (e.g. reliability models of the barriers and liners and polymer permitivities) of copper-related interconnects.

Lithography

193 nm Optical Materials Damage Studies: Researchers at the University of California at Berkeley, led by Professor William Oldham, have demonstrated that prolonged exposure to 193 nm radiation causes damage to fused-silica optical elements by color-center formation, which reduces transmission, and by altering density (compaction). Their pioneering research in the area of optics metrology yielded a uniquely sensitive technique for measuring compaction at a level of 10 ppB. This discovery has resulted in significant savings of between $10 million and $100 million. Members have been able to avoid premature equipment purchases and have gained time to consider alternative development strategies for initial passes of 250 nm and 180 nm manufacturing.

This research continues to yield fundamental insights into the primary damage mechanisms in fused silica, which are dependent on the chemistry and annealing history of the glass, its temperature and the intensity of the irradiation source.

More recently, the research is relating compaction damage to imaging performance degradation. Another goal is to understand the structural form of compaction and mechanisms. Data from MIT Lincoln Labs support University of California at Berkeley's findings by observing macroscopic void and tunnel formation in optical materials induced by exposure to 193 nm radiation. The

scaling of damage rates to intensity levels in lithographic optics, requiring improvements in sensitivity (to the few ppB range), is considered by some members to be the most important task in the portfolio.

Advanced-Resist Materials Research: Professor Grant Willson and researchers at the University of Texas at Austin demonstrated the feasibility of single-layer and novel-top surface imaging options for 193 nm lithographic applications. Specific results include:

- the utility of cycloaliphatic addition polymers as a platform from which to design chemically amplified, single-layer 193 nm resist materials with etch resistance comparable to current I-line resists and
- a more fundamental understanding of the potential of a novel-top surface imaging process that allows pattern-wise introduction of silicon-bearing reagents into resist films without image distortion due to swelling.

The research thrust into the design of novel structures for single-layer 193 nm applications provides a balance of optical transparency etch resistance. The discovery of a top-surface imaging scheme for 248 nm and 193 nm applications may greatly improve process control. This research has aroused considerable interest within the supplier community and resulted in a 1996 SEMATECH award of $750,000 to accelerate and facilitate timely commercialization.

EUV Wavefront Metrology: A research team headed by Professor Jeff Bokor at the University of California at Berkeley is developing metrology options that will enable members to evaluate extreme ultraviolet (EUV) optics and the impact of defects, as well as to gate the progress and performance of developments in EUV optics technology. This team builds upon Sommargren's contribution to visible phase-shifting interferometry by exploring the feasibility and limits of making measurements in the EUV regime. This exploration is necessary to account for any wavelength-dependent effects, such as the phase-shift effects inherent in multilayer reflection coatings. The team's goal is to develop metrology necessary for characterizing wavefront aberrations in short-wavelength lithography optics at the operational wavelength from 193 nm down to 13 nm. Researchers are continuing to develop point diffraction interferometry with an accuracy target of lambda/1000, and interferometers will be constructed at both 193 nm and 13 nm wavelengths.

Resist Materials with Low Environmental Impact: Researchers at the University of Texas at Austin, led by Professor Grant Willson, and at Cornell University, led by Professor Jean Frechet (now at University of California at Berkeley), collaborated on studies of resist materials with low environmental impact. Their task was to design and demonstrate the feasibility of novel aqueous castable and aqueous developable resist systems with sub-micron resolution. In lithographic processing, all of the solvents and 98 percent of the solids in the resist become part of the waste stream. The traditional organic solvent-based resist formulations present serious waste disposal problems. This waste load could be reduced to a minimum if resist materials were formulated from water-soluble materials and developed using pure water.

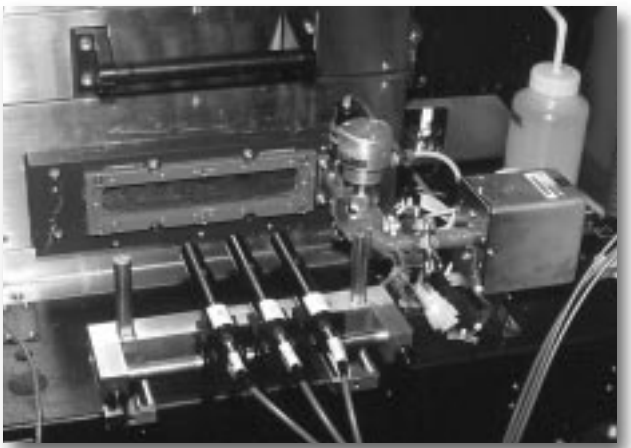
The researchers have designed and synthesized water-soluble and water-developable resist materials. They have demonstrated sub-micron DUV imaging using water as both the casting solvent and the developer. The Strategic Technologies and environment, safety and health (ESH) Focus Technical Advisory Boards (FTABs) have awarded funds to facilitate the transfer of this knowledge from researchers at the University of Texas at Austin to a domestic resist supplier and SRC-member. The supplier is exploring the commercialization potential of these research options for high volume/low lithographic performance applications.

Factory

Integrated Sensors for IC Manufacturing Applications: Professor Ken Wise and his team at The University of Michigan developed sensors for temperature measurement, flow-rate and pressure measurement, and gas analysis. These sensors help workers monitor the process environment more closely and therefore improve process control.

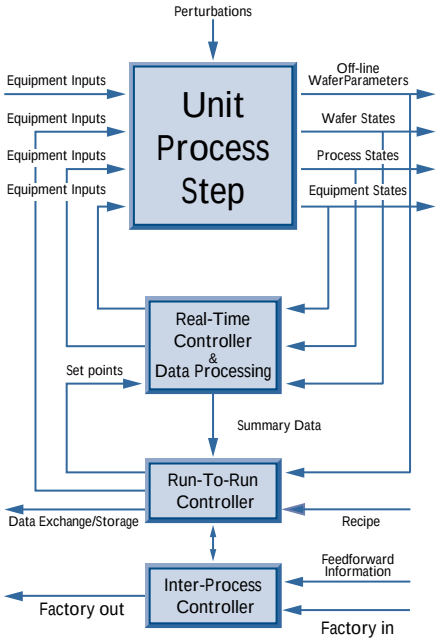
Equipment and Process Control: Professor Jessy Grizzle's team at The University of Michigan developed general control methods for improving overall equipment effectiveness. The team integrated real-time, model-based feedback control with run-to-run control and process optimization. The control philosophy was embodied in a hierarchical controller structure: Wafer data obtained via post-process measurements were used to adjust equipment set-points with a run-to-run control algorithm, while wafer and process variables obtained online were used to adjust equipment inputs in real-time.

This layered control architecture allows diverse control algorithms to be readily added and/or compared. The approach led to specific improvements in the real-time control of reactive ion etching (RIE), where real-time loops significantly reduced sensitivity to common process variations.



A spatially resolved, three-point OES sensor is installed on a polysilicon plasma etch chamber in the Berkley Microfabrication Laboratory.

Figure 7: Hierarchical Control Architecture Producing Real-Time Model-Based Feedback



Plasma Control: Professor Costas Spanos and other researchers at the University of California at Berkeley developed statistically-based techniques to model and control run-to-run process variations. Results indicate that ion bombardment-based etching is more easily monitored by optical emission samples (OES) than by chemically-based etching, where links to easily observable OES signatures are more complicated. As a result of this research, factories can easily monitor oxide etch through OES. However, aluminum is difficult to monitor, while polysilicon etching appears to present medium difficulty.

Researchers found that they could use the real-time profile of several optical emission traces for quality control purposes, specifically for identifying wafers with high CD non-uniformity. The team also developed algorithms for long-term compensation for window clouding during OES monitoring.

SRC Student Services

Education Pays Tech-Transfer Dividends

Andrew M. Abo, UC, Berkeley
Daniel B. Bergstrom
University of Illinois
Paul L. Bergstrom
The University of Michigan
Michael F. Booth, Cornell University
Arthur T. Bradley, Auburn University
Stephen M. Cea, University of Florida
Roawen Chen, UC, Berkeley
Jason P. Chin, Northwestern University
Jonathan C. Doan, Stanford University
Brian M. Dugan, Yale University
AMD/SRC Fellow
Cheryl G. Faltermeier, SUNY, Albany
Timothy S. Fisher, Cornell University
Mark J. Fordham, NC State University
J. Lawrence Goodby, UC, San Diego
J. Matthew Hankinson
The University of Michigan
Jennifer M. Havard, Cornell University
AMD/SRC Fellow
Brian E. Hornung
NC State University
Gregg N. Hoyer
University of Washington
Frederick Y. Huang
University of Illinois
Anna M. Ison, UC, Berkeley
Motorola/SRC Fellow
Simon M. Karecki, MIT
Motorola/SRC Fellow
Jean E. Kelsey, SUNY, Albany
Marline Manassian, UT, Austin
Bruce W. McGaughy, UC, Berkeley
George H. McMurray, UC, Berkeley
Katherine E. Mueller, UT, Austin
Shipra Panda, Carnegie Mellon
National Semiconductor/SRC Fellow
John G. Pellerin, UT, Austin
Charles M. Perkins, Stanford University
NIST/SRC Fellow
William P. Pinello
University of Arizona
Eric J. Shero, University of Arizona
Thomas R. Shiple, UC, Berkeley
Jeffrey M. Snodgrass
Stanford University
Robert J. Socha, UT, Austin
National Semiconductor/SRC Fellow
Robert Sumners, UT, Austin
AMD/SRC Fellow
Ronald D. Sutcliffe
University of North Texas
Bassam Tabbara, UC, Berkeley
Todd E. Takken, Stanford University
Gregg S. Talbert, Duke University
Robert M. Burger Fellow
Martin O. Tanner, UCLA
Nerissa S. Taylor, University of Illinois
Shawn G. Thomas, UCLA
Peter J. VanDerVoorn
Cornell University
Steven V. Walstra, University of Florida
Xin Y. Zhang, Stanford University

Relevantly educated students with leading-edge research experience are a primary product of the SRC research program. SRC Student Services seeks to attract top candidates to this pool of talented students. Through student internships and possible employment by members, these graduate students provide a viable means of technology transfer. This reservoir of high-quality, talented individuals serves to ensure member company access to the next generation of leaders for the semiconductor industry.

Graduate Fellow Kevin Kline (left), who worked with Professor Al Tasch (right) at the University of Texas at Austin, is now employed by Motorola.

A key program for cultivating excellence within the superior talent pool of students is the SRC Graduate Fellowship Program (GFP) for U.S. students. In 1996, the GFP was expanded to 36 fellowships with the addition of six company-named fellowships, two each from AMD, Motorola and National Semiconductor. The SRC fellows exemplify those qualities of dedication, intellectual curiosity, technical ability, motivation and creativity that are required for productive university scientific and technical research.

Also in 1996, the SRC began a new venture with the National Institute of Standards and Technology (NIST)/SRC Fellowship at Stanford University. This fellowship, valued at $75,000 a year, pays expenses for one student and includes an internship at NIST. In addition, the fellowship provides a gift in support of research related to metrology for thin-dielectric films.

The SRC initiated a restricted web site in 1996. An important function served by this web site is the delivery of student resumes. By the third quarter, over 200 student resumes were linked to the Research Catalog through the electronic version of the Graduate Student Directory. Member companies also received resume files on diskettes for downloading to internal resume systems.

JobsFair at TECHCON '96 provided a new avenue of industry access to the SRC students, with 13 companies and 200 students participating. Company representatives, which included hiring managers and recruiters, reported exceptional value from this event because it showcased students of extraordinarily high quality and specific interest to the industry.

Over 700 students participated in SRC research in 1996. Also, nearly 200 new graduates joined the 2,000 graduates hired by the semiconductor industry and university community from SRC research programs since 1983. These students facilitate the transfer of new science and technology to supporting organizations and stimulate new research activities that encourage yet another generation of students to enter semiconductor-related fields.

During JobsFair, a student talks with Mike Sampogna from National Semiconductor while Justin Harlow, an SRC assignee from National Semiconductor, looks on.

SRC Technical Excellence Award

Rewarding Groundbreaking Research

Established in 1991, the SRC Technical Excellence Award recognizes research of exceptional value to SRC members. So far, 12 technologies and 40 researchers have earned the Technical Excellence Award.

The award is presented annually for research that significantly enhances the productivity and competitiveness of the North American semiconductor industry. Awards are based on the following criteria:

- Creativity and innovation;
- Relevance to the research objectives of the SRC and the semiconductor industry (as reflected by the National Technology Roadmap for Semiconductors);
- Value or impact on industry in relation to internal program acceleration, research integration, person-year(s) of effort saved and strategic direction; and
- Technology transfer success.

In 1996, the SRC selected two research teams to receive the 1995 Technical Excellence Award. Both were recognized at an awards luncheon and poster session held in conjunction with the SRC's June 1996 board of directors meeting.

Professors Randal Bryant and Edmund Clarke and former graduate student Dr. Kenneth McMillan were honored for their work at Carnegie Mellon University (CMU) on formal verification techniques. Their research led to the development of a mathematical verification technique for integrated circuits.

From left, Professor Edmund Clarke, Dr. Kenneth McMillan and Professor Randal Bryant receive the Technical Excellence Award for their work at Carnegie Mellon.

With CMU's new symbolic model verifier (SMV) software, design engineers can test, analyze and detect errors in ICs under all possible operating conditions. Researchers can achieve verification results with SMV in a reasonable time — minutes instead of years of simulation time. The most successful method to date of formally verifying today's complex ICs, SMV has proved particularly effective in dealing with the complexities of modern, high-concurrent systems, such as shared memory multiprocessors.

From left, Professor Kang L. Wang, Martin Tanner and Dr. Timothy Carns share an award for their work at UCLA.

The second team to receive the award was UCLA Professor Kang L. Wang, post-doctoral researcher Dr. Xinyu Zheng, former student Dr. Timothy Carns and current students and SRC Graduate Fellows Martin Tanner and Shawn Thomas. Their research focused on properties and device applications of innovative post-shrink silicon device structures.

As new designs further shrink the feature sizes on today's semiconductors, it becomes possible to produce devices that operate on quantum mechanical principles. At UCLA, researchers are factoring in quantum effects to create new silicon devices with reduced feature sizes. These smaller feature sizes will extend operational abilities beyond the physical limits of conventional complementary metal-oxide semiconductor devices. The researchers have invented and demonstrated a bistable-tunneling, static random-access memory, which will increase the benchmark density close to that of dynamic RAM with the same feature size.

SRC Industrial Mentor Program

Industry Mentors Facilitate Technology Transfer and Recruiting

Cooperation between industry and educational institutions is a key ingredient for success in scientific or engineering research and development. In 1983 the SRC established the Industrial Mentor Program to assist its community in teaming up with university researchers for mutual benefit. Mentors are scientists, engineers or managers from member companies or government agencies who maintain active, constructive relationships with the faculty/student research teams of specific SRC-funded university projects. Through the mentor relationship, member companies gain early access to key technology and provide guidance to ensure that emerging technology is relevant to their industry needs. Mentors also facilitate the transfer of research products from university labs to commercial applications.

In 1996, 616 individual mentors from 33 SRC-member companies and organizations were involved in SRC research tasks. To recognize and honor the significant contributions made by individual mentors, the SRC presents its annual Outstanding Industrial Mentor Award. Seven mentors received this award in 1996:

Dr. Erik Egan of Motorola, Inc. (Austin, Texas) has been a mentor to Professor Klavs Jensen and his team of graduate students at the Massachusetts Institute of Technology since 1993. In addition to regular visits to MIT, Dr. Egan invites students and faculty to Motorola. He works closely with several SRC students, offering them feedback on their modeling efforts and opportunities for industrial experience, as well as facilities at Motorola to serve as a beta test site during model development.

Dr. Avtar S. Jassal of SEMATECH (Austin, Texas) has been a mentor to both Professor Gregory Raupp at Arizona State University and Professor Grant Willson at the University of Texas at Austin for several years. At Arizona State, Dr. Jassal gave continuous feedback data from his laboratory to researchers that helped them scale-up to a pilot test unit. In his interactions with Professor Willson's group, Dr. Jassal assisted the researchers in their aqueous resist development work. Dr. Jassal also gave guidance and financial support to ensure that the project was showcased at several important environment, safety and health (ESH) review meetings and SEMICON.

Dr. Paul Packan of Intel Corporation (Beaverton, Ore.) has been a mentor for Professor Mark Law's diffusion research project at the University of Florida since 1994. A strong advocate for Florida's program, he has assisted researchers to define and gain approval for an enlarged joint effort with the SRC and SEMATECH. Dr. Packan's close collaboration with the university researchers has facilitated an early transfer of technology to the industry. This technology contributed a new interpretation of transient enhanced diffusions mechanics, which is applicable to the development of state-of-the-art process technologies.

Dr. Karl Puttlitz of IBM Corporation (Hopewell Junction, N.Y.) has been a mentor to Professors Leon Keer and Morris Fine at Northwestern University since they began conducting SRC research. He provides the researchers with significant advice on the technological implications of their work. He has also helped the team hone their lifetime prediction strategy for solders. With his guidance, researchers have now found a way to predict the failure of thermo-mechanical solders earlier than was previously possible. Dr. Puttlitz conducted a thorough survey throughout IBM to obtain recommendations on new solders — information that was essential to the project's success.

Mario Pelella of IBM Corporation (Hopewell Junction, N.Y.) has been a mentor for Professor Jerry Fossum at the University of Florida since 1994. Not only does Pelella facilitate strong collaboration between the university and IBM, but he also helps initiate interactions with other companies and universities. These interactions have resulted in widespread transfer of SOISPICE and an IBM/Meta-Software agreement to develop an SOI interface for the SOISPICE modes, ultimately supporting the public-domain release of the models.

Rob Ramage of Intel Corporation (Hillsboro, Ore.) has been a mentor to Professor Grant Willson and his team of researchers at the University of Texas for the past several years. Ramage has shown a particular interest in the team's dissolution rate and modeling projects. Upon hearing that the team's capabilities were limited for measuring high dissolution rates, he played a key role in obtaining the donation of an SC Technologies multi-wavelength, thickness/dissolution rate measurement tool owned by Intel. As a result of Ramage's efforts and interest in the group last year, one student earned a summer internship at Intel.

Deo Singh of Intel Corporation (Santa Clara, Calif.) has been a mentor to Professor Massoud Pedram of the University of Southern California since the project's inception in 1994. One problem on vector compaction for complex systems that Singh brought to the attention of the university research team resulted in a solution not only for Intel but for the industry in general. He has arranged on-site summer job opportunities for the students at Intel that have enabled them to try out their ideas and tools on industrial data with real-life constraints. Through Singh's efforts, the students gain a better understanding of the industry and a learning experience that assists them in their Ph.D. research.

Mentor award recipients are honored at the June 1996 board meeting. From left, they are Paul Packan, Intel Corp.; Rob Ramage, Intel Corp.; Erik Egan, Motorola Inc.; Karl Puttlitz, IBM Corp.; Mario Pelella, IBM Corp.; and Deo Singh, Intel Corp. Avtar Jassal, SEMATECH, is not pictured.

SRC Intellectual Property

Preserving Options for the Future

Another value of SRC membership is protection of technology and intellectual property assets that are developed as a result of SRC support. The SRC has a world-wide, non-transferable, royalty-free, non-exclusive license right to inventions and works of authorship resulting from SRC-funded research. The SRC may sub-license such inventions and works of authorship, as appropriate, to SRC members.

Notable portfolio additions in 1996 included key technical advances developed in the areas of water-soluble photoresists, semiconductor-on-insulator (SOI) advanced devices and IDDQ testing. Eleven new U.S. patent applications were filed in 1996 from invention disclosures resulting from the SRC research program. Overall, the SRC added 18 new U.S. patents to its intellectual property portfolio, with an additional six patents formally allowed (will issue in first quarter 1997), bringing the SRC's total number of U.S.-issued patents to 138. The table on page 24 lists SRC U.S. patents issued in 1996.

In addition, 27 alpha releases of software programs were developed in 1996 with SRC support. Other significant official releases included the VIS (Verification Interacting with Synthesis); CUDD (Colorado University Decision Diagrams); WSMV (Word-Level Model Checker); and iTEM (Illinois Thermal-Electrical Modeling).

SRC U.S. Patents Issued in 1996

1996 SRC Patents	Inventor Institution	Filing Date	Issue Date	Patent Number
Single Crystal Contacted Double Self-Aligned Bipolar Junction Transistor with Vertical Seeded Selective Epitaxial Growth	G. Neudeck, et al. Purdue University	9/27/94	1/2/96	5,481,126
Silicon-On-Insulator Transistors Having Improved Current Characteristics and Reduced Electrostatic Discharge Susceptibility	C-M Hu, et al. University of California at Berkeley	4/7/94	2/6/96	5,489,792
Method of Forming Semiconductor-On-Insulator Electronic Devices by Growing Monocrystalline Semiconducting Regions from Trench Sidewalls	G. Neudeck, et al. Purdue University	9/27/94	2/27/96	5,494,837
Digital Auto-Calibration of Pipeline A/D Converters	H-S Lee, et al. Massachusetts Institute of Technology	2/24/94	2/27/96	5,499,027
Oxidizing Methods for Making Low Resistance Source/Drain Germanium Contacts	D. Ast, et al. Cornell University	11/30/94	5/14/96	5,516,724
Integrated Circuit Having Clock-Line Control and Method for Testing Same	W. Rogers, et al. University of Texas at Austin	12/2/93	5/21/96	5,519,713
Test Pattern Generation for an Electronic Circuit Using a Transformed Circuit Description	W. Maly, et al. Carnegie Mellon University	1/18/95	6/18/96	5,528,604
Positive-Tone Photoresist Containing Novel Diester Dissolution Inhibitors	J. Frechet, et al. Cornell University	8/31/94	7/2/96	5,532,106
Modification of Polyvinylidene Fluoride Membrane and Method of Filtering	S. Raghavan, et al. University of Arizona	7/7/94	7/2/96	5,531,900
Photoresists Containing Water Soluble Sugar Crosslinking Agents	J. Frechet, et al. Cornell University	9/21/95	7/2/96	5,532,113
Stress-Free Mount for X-Ray Lithography Masks	F. Cerrina, et al. University of Wisconsin	11/22/94	7/16/96	5,536,559
Photoresists Containing Water Soluble Sugar Crosslinking Agents	J. Frechet, et al. Cornell University	9/21/94	7/16/96	5,536,616
Quantum Bridges Fabricated by Selective Edging of Superlattice Structures	K. Wang, et al. University of California at Los Angeles	2/6/95	7/23/96	5,539,214
MOS Transistor Having Improved Oxynitride Dielectric and Method of Making Same	D-L Kwong, et al. University of Texas at Austin	11/10/94	7/30/96	5,541,436
Dynamic Threshold Voltage MOSFET for Ultra-Low Voltage Operation	C-M. Hu, et al. University of California at Berkeley	8/30/94	9/24/96	5,559,368
Ultra Thin-Dielectric for Electronic Devices and Method for Making Same	D-L Kwong, et al. University of Texas at Austin	9/18/95	11/26/96	5,578,848
Positive-Tone Photoresist Containing Novel Diester Dissolution Inhibitors	J. Frechet, et al. Cornell University	4/17/96	12/17/96	5,585,223
Apparatus and Process for Producing High Density Axially Extended Plasmas	J. Cecchi, et al. Princeton University	6/16/94	12/24/96	5,587,038

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