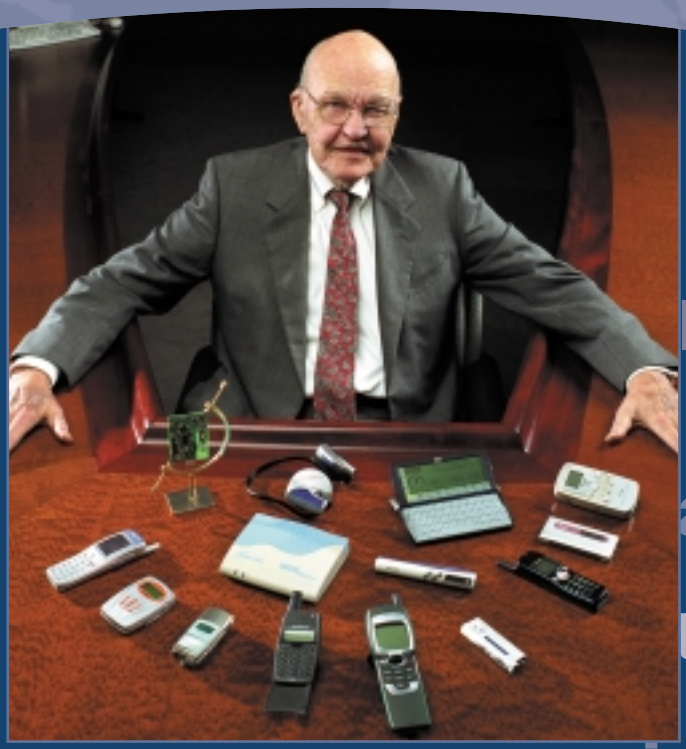
2000 Annual Report

two-thousand

Pioneers in Collaborative Research

The Semiconductor Research Corporation

Jack Kilby Dedication



There are few living men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men.

There are few living men whose insights and professional accomplishments have changed the world. Jack Kilby is one of these men. His invention of the integrated circuit — the microchip — some 30 years ago at Texas Instruments (TI) provided the conceptual and technical foundation for modern microelectronics. This was the key breakthrough that enabled the high-speed computers, large-capacity semiconductor memories, network appliances, and complex controllers that characterize today's information age. On December 10, 2000, Mr. Kilby was awarded the Nobel Prize in Physics for his pioneering and revolutionary work.

Jack Kilby has been an integral part of SRC's evolution. He participated actively in SRC's summer studies in which he provided key perspectives in debates on strategic organization directions and seminal insights on semiconductor technology issues. Jack also played a key role in the development of SRC's intellectual property policies by guiding their formulation and participating in their implementation. More recently, he proposed the Landmark Innovation Award the first of which was presented by Mr. Kilby to Prof. Farhang Shadman at TECHCON 2000. More importantly, Jack has made himself available to consult and guide SRC throughout its nineteen-year existence. He has been, and is, an important part of the successful development of cooperative research in semiconductor technology.

In recognition of his lifetime of accomplishments, of the recognition of his achievements through award of the Nobel Prize, and his contributions to cooperative research in semiconductors, the Semiconductor Research Corporation dedicates this annual report to Jack S. Kilby.

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Vision

Semiconductor Research Corporation (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

Mission

SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the ITRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research.

The annual report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program, present the formal financial report and provide information on activities and events of the SRC community for the previous calendar year.

A copy of this report and additional information about SRC are accessible on the World Wide Web at **http://www.src.org.**

Message from the President/CEO

The year 2000 was a great one for SRC, and our June board retreat provided pivotal guidance for SRC as it evolves into a fully global research management consortium.

It seems that each SRC board retreat gets better, but last June's retreat was clearly our best ever. SRC is an organization where its owners are its customers. The Board, to be most effective, needs to examine policy issues from the standpoint of both owners — where the Board is a "steward" of SRC; and as a customer — where each Board member wants to see its company receive maximum value for each dollar invested in its member fee.

As SRC's customers, our board reiterated the importance of maximizing benefits to each SRC member company. In that spirit, SRC began to examine new programmatic structures and more flexible research program participation. Our goal is to enable member companies to optimally customize their research choices according to each company's interests, while maintaining a strong, viable core research program with high value for all members.

We also committed new resources, staff and priority status to the SRC Education Alliance to help address the projected shortfall of talented scientists and engineers throughout the world. We instituted an undergraduate research program in cooperation with the Semiconductor Industry Association (SIA) and we recommitted our efforts to increase the number of SRC-supported graduate students who become employed by member companies.

As stewards, our board recognized the necessity for a much stronger SRC to tackle the increasingly complex demands of the International Technology Roadmap for Semiconductors. The board recognized the importance of not only expanding SRC's international membership to increase our research budget and reduce the "research funding gap" in addressing the major global technology challenges and barrier issues, but also to better enable a broader collaboration to include the best researchers in the world. Through a broad globalization effort, to include new member companies, university researchers worldwide, enhanced coordination with global consortia, and potential leveraged funding from governments in other regions of the world, the SRC Board of Directors has clearly outlined a broad globalization strategy for SRC. This strategy will not only enable SRC to keep pace with the internationalization efforts of its members but to continue to be a leader among other research consortia throughout the world.

Sincerely,

Larry W. Sumney

About SRC

PIONEERS IN COLLABORATIVE RESEARCH

Pictured left to right during a press conference at UMC: **Ralph Cavin**, **Dinesh Mehta** and **Larry Sumney** of SRC and **Robert Tsao**, **John Hsuan** and **Fu-Tai Liou** of UMC.

More than 18 years ago, leaders of the semiconductor industry, decided to launch SRC to establish and nurture North American University research capability in semiconductor technologies. This was an important decision to address several critical issues such as the weakened competitive position of the U.S. semiconductor companies in market and technology; inability of these companies to invest significantly in long-term research individually; lack of U.S. government support for research in silicon-based technologies; and resulting lack of university research capability. Since formation, SRC has consistently produced excellent research results and trained more than 3000 scientists and engineers who have helped make the semiconductor industry a strong and vital part of the electronic revolution.

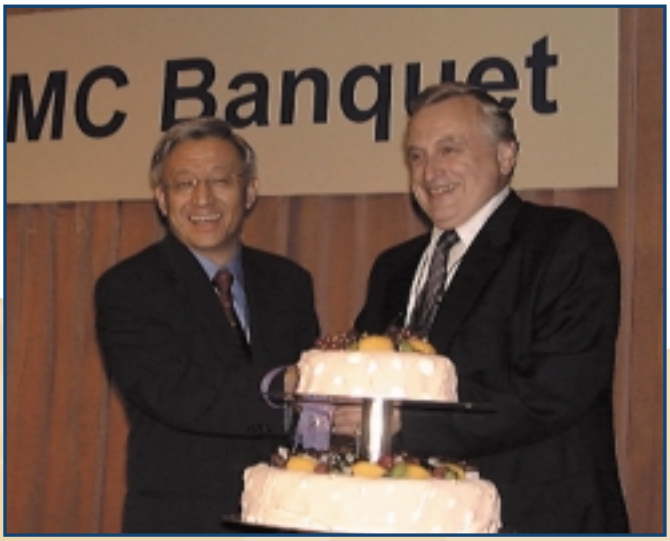
The semiconductor industry has become global. In addition to establishing distributed marketing and manufacturing capability, semicondutor companies are also creating global R&D presence. Semiconductor companies from many regions of the world have decided to cooperate in the development of the International Technology Roadmap for Semiconductors (ITRS), which identifies the technologies needed to maintain the aggressive pace of Moore's Law. Recent editions of the ITRS point out that the "red" areas — technical challenges for which there are no known solutions — are increasing in number and are encroaching in time. In addition to the technological challenges, the semiconductor industry also faces a potentially critical shortfall in scientists and engineers in the future. These challenges are global and require collaboration among semiconductor companies worldwide. SRC has developed core competencies and a model of collaborative research that position the consortium to address these challenges. In response to these challenges and based on SRC capabilities, the SRC Board decided to expand its membership to non-U.S. companies starting in the year 2000. At their annual Board Retreat in June 2000, the SRC Board authorized SRC to expand the research performer base to non-North American universities. Thus, we have begun the process of complete globalization of SRC.

In the broader context of a global SRC, we have continued to focus on the creation of four "products." These are Research Results, Relevantly Educated Talent, Integrated University Research Capability, and Networking. We have also continued to hone processes and tools associated with the delivery of SRC value to the member companies. Mechanisms and support are also provided to facilitate our member companies' ability to extract maximum value in a most cost-effective manner. Finally, we work with the representatives of our member companies on the Board of Directors and various advisory boards to continuously revitalize our products, programs, processes and systems to enhance value for our members. Several examples of the dynamic nature our business and the value that the community of our consortium has brought about in the year 2000 are

About SRC

presented in various sections of this report. Some of the key accomplishments, major initiatives and important events of the year 2000 which demonstrate the value, the strength and agility of the consortium include:

- A strong research program which is aimed at addressing major technological challenges the industry faces for technology nodes (pages 5-13).
- A highly beneficial and productive set of student programs and a high rate of assimilation of the graduates in the year 2000 within the SRC community (pages 18-19).
- Successful completion of the Pilot phase of the first two Focus Centers managed by MARCO (a subsidiary of SRC) and the decision to initiate two new Focus Centers in the year 2001 (page 28).
- A phenomenally successful TECHCON 2000, our biennial technical conference which showcased the best of our research and students performing the research (page 14-17).
- Some of the highly coveted awards that recognize the contributions of various constituents of the SRC community (pages 16-17). One of these awards, the Landmark Innovation Award, presented by Mr. Jack Kilby, who was selected to receive the Nobel Prize in 2000 (inside front cover).
- Culmination of "Cu Design Contest," conducted in collaboration with UMC, Novellus, SpeedFam-IPEC, with outstanding results (page 22).
- A very productive set of workshops conducted in Taiwan for the technical community of UMC and Taiwan Universities.
- Strong participation by the member companies in the Industry Assignee Program (page 24-25).
- Launching of a completely redesigned Web site which has many more features such as online collaboration capability, etc. (page 23).
- Creation of a database of the Intellectual Property portfolio (page 26-27).
- A set of three new initiatives to increase the pool of undergraduate engineering students in semiconductor technology related disciplines. These initiatives, approved and funded by SIA, are managed through the SRC Education Alliance, an arm of SRC (page 18-19).



Robert Tsao, Chairman, UMC (left) and **Larry Sumney**, President and CEO, SRC at a banquet to celebrate the Taiwanese company's recently announced SRC membership

Research Contributions

SRC'S RESEARCH AGENDA

The SRC university research program is focused on the critical technology barriers to the continued exponential performance-cost cadence of Moore's Law as identified by the 2000 International Technology Roadmap for Semiconductors (ITRS). In addition, SRC is conducting several exploratory programs that seek to obtain radical solutions to ITRS challenges. In the following, perspectives are given on the response of the highly productive SRC research program to pacing technology challenges. SRC acknowledges its excellent partnerships with NSF, DARPA, International SEMATECH and the State of New York in support of some of the programs described herein.

EXTENDING CMOS

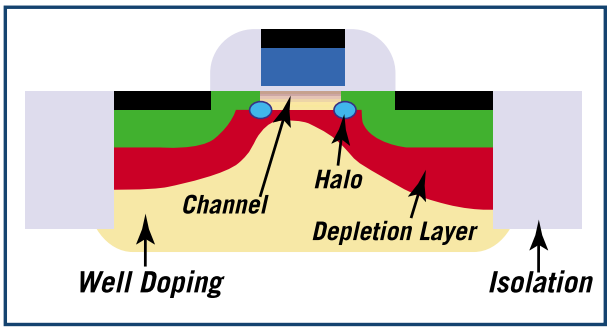
SRC Research is directed toward:

- Extensions of bulk MOSFETs and their associated materials and processes;
- Continued scaling of non-bulk MOSFETs gate lengths less than 10 nm;
- MOSFET modeling and simulation.

Challenges to the continued scaling of CMOS transistors include the ability to:

- Maintain a constant threshold voltage as MOSFETs scale to nano-scale dimensions (short channel effect);
- Develop hyper-abrupt lateral and vertical doping profiles, with super metastable doping concentrations;
- Provide extremely shallow source/drain extensions with low sheet resistance;
- Mitigate the effects of channel dopant fluctuation;
- Develop materials for thin, low-leakage gate dielectrics; and for high-conductivity gate electrodes.

Bulk CMOS may extend to 35 nm (physical gate length) with new gate stack materials and source/drain process technologies. Non-bulk MOSFET structures may extend CMOS to physical gate lengths of 10nm.



Prototypical MOSFET

BULK CMOS

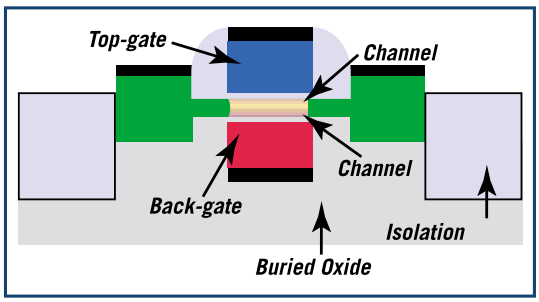
Bulk CMOS research focuses on new gate stack materials and ultra-shallow source/drain junction structures that extend scaling to the 70 nm technology node and beyond. The Front End Processing Research Center (FEP-RC) at North Carolina State University addresses formation and properties of ultra-thin high-k gate stack dielectrics and their interfaces, and alternative high-conductivity gate materials to replace poly-silicon gates and solve the poly-silicon depletion problem related to ultra-thin gate dielectrics.

Research Contributions

Promising replacements for n+-poly-silicon include Ta, TaN_x, and $TaSi_xN_y$, and for p+-poly-silicon, Ru and $Ru0_2$. Initial studies at University of California/Berkeley show that Mo and N implanted Mo are viable gate electrode candidates.

NON-BULK CMOS

Complementary non-bulk CMOS approaches to a viable double-gate MOSFET platform structure are being investigated to reduce short channel effects in the 10 nm regime. MIT is investigating wafer bonding and self aligned ion-implantation; University of California/Berkeley uses e-beam lithographic alignment and selective processing; and Purdue University, selective epitaxy and epitaxial lateral overgrowth to achieve self alignment. The potential of strained Si and SiGe (MIT) and graded, strained SiGeC (University of Texas/Austin) for enhancing channel mobility in advanced MOSFET structures is also being examined. These different approaches to a double-gate MOSFET provide very different platform structures to study experimentally the properties of structures and materials.



Prototypical double-gate MOSFET

NANO-SCALE CMOS: MODELING AND SIMULATION

The device modeling and simulation research agenda includes:

- Quantum confinement and quantum transport in heterostructure channels;
- Direct and Fowler-Nordhiem carrier tunneling through ultra-thin gate dielectrics;
- Strain effects on band structures;
- Incorporation of quantum effects into semi-classical models; and
- Computational techniques for 3-D simulators.

Approaches include:

- 2-D atomic level quantum mechanical approaches (Purdue University);
- Efficient 3-D Monte Carlo semi-classical techniques (University of Illinois/Urbana-Champaign);
- Combined analytical expressions for tunneling with a unique numerical 2-D Poisson solver that places the source, drain and gate on an equal footing to the channel (SUNY/Stony Brook).

These studies are showing, for example, that MOSFETs with sub 10 nm physical gate lengths provide good performance (if a channel mobility up to 400 cm^2/sec can be realized) and that quantum transport along the channel is primarily related to tunneling through the source/drain barrier.

Research Contributions

INTERCONNECT SOLUTIONS FOR FUTURE GENERATION IC SYSTEMS

The 1997 ITRS identified global interconnects — where signals often cannot propagate for long distances without unacceptable delays, cross-coupling, and/or clock skew as a critical problem. At and beyond the 70 nm node, die sizes and frequency requirements are incompatible with even the most optimistic design, packaging, and technology projections. Radical changes in the approaches to IC design, processing and packaging are required.

DESIGN SOLUTIONS

Near-term approaches include techniques to optimize interconnect routing, minimize crosstalk, and analyze signal and power bussing. Longer-term research addresses system and device design methodology and architectures. For example, the University of Minnesota is developing hierarchical power network analysis methods for handling power grids with 20 million nodes and the University of California/Los Angeles is focused on interconnect planning and wire width optimization.

PACKAGING SOLUTIONS

Advanced packaging and interconnect systems using capacitive and RF coupling into the package, reducing pin count, and improving system performance are being investigated at North Carolina State University and the University of California/Los Angeles. Novel inter-chip and intra-chip communications and signaling protocols are being developed at the Universities of Massachusetts and Toronto for noise reduction, efficient power delivery, and high system throughput.

TECHNOLOGY SOLUTIONS

The Back-End Processes Thrust seeks technology solutions to the interconnect challenge through innovations in copper-low K, and non-contact interconnect using optical or RF/microwave links, 3-D devices and chip stacking, and radical alternatives such as nanotubes and nanowhiskers. These projects are defining fundamental limits for copper-low K technologies and resolving issues involved in other advanced technologies.

COST-EFFECTIVE NANOSCALE PATTERNING

SRC supports foundational research in semiconductor patterning to enable:

- MOSFET scaling at and beyond the 50 nm ITRS technology node;
- Radical high performance, high throughput, low-cost alternatives to conventional IC patterning technology;
- Increased functional density both on the chip and within nanostructures.

Patterning research anticipates future manufacturing requirements and addresses strategic technology challenges.

Research Contributions

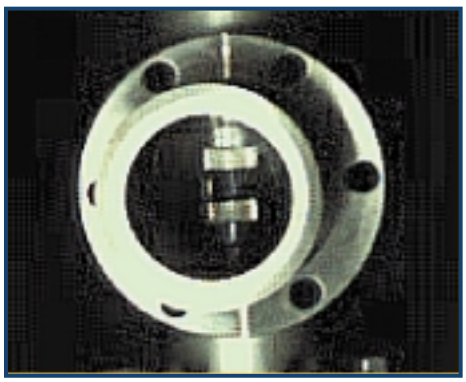
OPTICAL LITHOGRAPHY

SRC research in 193 nm wavelength lithography has removed the perceived barrier at the 100 nm node for optical patterning. Today's challenge is to extend optical lithography below the 65 nm node. Current research addresses sources, optical components, masks, resists, predictive pattern transfer models, and trade-offs for 193 nm, 157 nm, and 127 nm wavelengths for patterning beyond 65 nm ITRS technology requirements.

NEXT GENERATION LITHOGRAPHY (NGL)

The current strategy is to replace optical lithography for critical layers beyond the 65 nm ITRS node. Two candidates for the sub-65 nm domain are Extreme-Ultra Violet (EUV) and Electron Projection Lithography (EPL).
Noteworthy results include:

- **Capillary Discharge:**
  University of South Florida has developed this leading candidate for future lithography.



Prototype EUV discharge source developed under SRC support. This source was transferred to the EUV LLC.

- **EUV Lithography and Actinic Wavefront Metrology:**
  University of California/Berkeley has developed an EUV interferometer with unprecedented accuracy for EUV lithography as well as techniques to counter carbon contamination
- **Image Formation Modeling and Verification:**
  University of Wisconsin has noted that thick EUV masks have unique influences on image formation and were the first to carry out the complicated modeling of such effects.
- **E-Beam Lithography:**
  Stanford University research has demonstrated that global space charge effects represent a significant technical challenge for electron projection lithography.

MASKLESS AND NON-LITHOGRAPHIC PATTERNING

Increasingly complex mask challenges require high throughput, high performance, and low-cost patterning options, such as maskless or step-and-flash patterning. SRC/DARPA cooperative research addresses five maskless patterning options, each requiring delivery of a tremendous amount of information in real time to individual pixels. Consequently, research focuses on managing the flow of data, and enabling delivery of a terabyte of information per second. Step-and-Flash patterning exploits capillary processes that enable nanoscale injection molding.

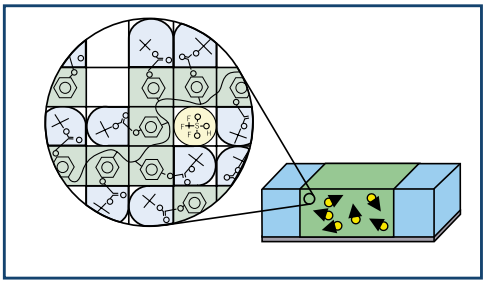
SRC research is continuing to explore other low-cost enabling material and technology options; functional dendrimers, defect tolerant patterning, heterogeneous self assembly, e.g., controlled directed nanotube growth.

Research Contributions

RESISTS

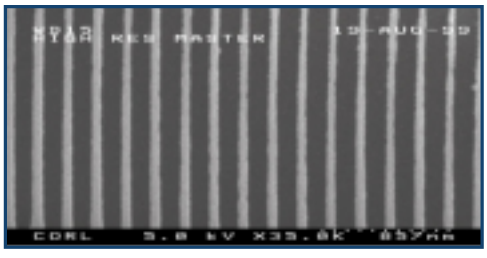
Recent significant resist-related results include:

- **Molecular Level Simulation of the Lithographic Process:** University of Texas/Austin foundational research on resist chemistry is resulting in a potentially comprehensive probabilistic model for the formation of imaged features during development, based on the design and structure of individual components.



Predictive model of image information based on designed resist components.

- **Photoresist Material Process:** University of Wisconsin has investigated the problem of the collapse of high aspect ratio photoresist features, documented the reasons for collapse, and presented techniques for avoiding it.
- **Dendrimer-Based Chemically Amplified Resist Materials:** University of California/Berkeley has demonstrated sub-100 patterning with novel dendrimer-based resist materials.



SEM of negative tone lines patterned in a dendrimer based resist.

METROLOGY

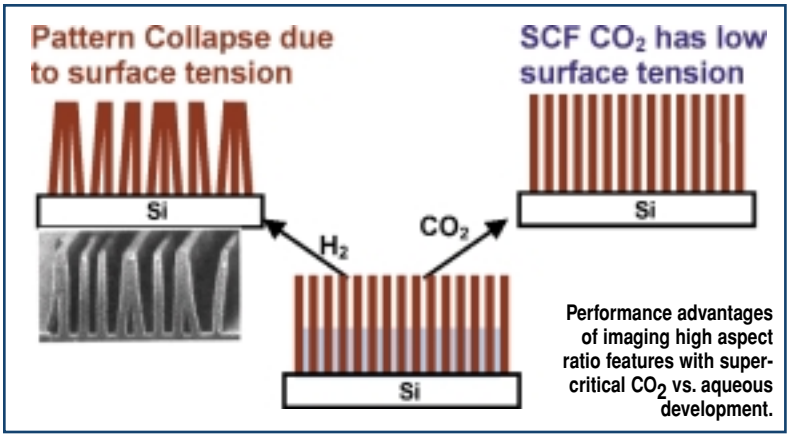
Advanced Techniques for E-beam Metrology:
University of Tennessee/Knoxville researchers are exploring fundamental challenges in ultra-low voltage e-beam imaging and dynamic charging; and are developing a point projection microscope for non-destructive nanoscale 3-D metrology. They recently reported the first reconstructed 3-D images of 100 nm features from the nanoscale point projection microscope.

HIGH PERFORMANCE, ENVIRONMENTALLY BENIGN PROCESSES

The agenda of the SRC/NSF Engineering Research Center (ERC) in Environmentally Benign Semiconductor Manufacturing is focused on future manufacturing facilities with minimal consumables (e.g. water, energy, acids, solvents, and gases) and minimum emission of waste materials. The ERC's program currently consists of:

- Back-End Processes, with emphasis on replacing perfluorocompound chemistries for dielectric wafer etch, PECVD chamber cleaning processes, slurry waste from CMP processes, and low-K dielectric technology for interconnect systems with environmentally benign process;
- Front-End Processes, with emphasis on benign surface preparation and novel high-K dielectric materials;
- Factory facilities, with emphasis on minimization of water and energy usage;

Research Contributions



Performance advantages of imaging high aspect ratio features with supercritical CO_2 vs. aqueous development.

- Patterning, with emphasis on non-solvent lithography and additive processing; and
- Education, with emphasis on creating an engineering curriculum that includes design for the environment.

Example results from 2000 research include:

- Reduction of chemical vapor deposition (CVD) effluents by pulsed plasma excitation (MIT);
- An electrophoretic cross-flow filtration technique for reducing total suspended solids (TSS) and copper ions from Chemical-Mechanical Polishing (CMP) waste streams (University of Arizona);
- Using electrodialysis to remove dissolved copper from the dispersion medium of CMP waste (University of Arizona);
- Demonstration of 150 nm features through e-beam patterning of CVD fluorocarbon films developed with supercritical CO_2 (Cornell University and MIT). Filed provisional patent for non-solvent, resistless patterning.

IMPROVING DESIGN PRODUCTIVITY & TIME-TO-MARKET IN DESIGNING, ANALYZING, AND TESTING IC PRODUCTS

Four major challenges in the design of electronic circuits and systems are:

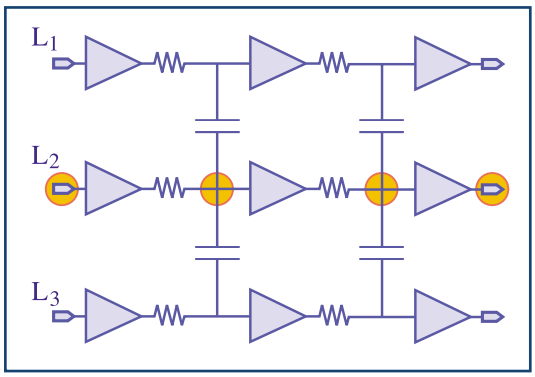
- Increasingly complex circuit design in the deep submicron range;
- Exponential growth in the number of circuits;
- Heterogeneous systems; and
- Market pressures to reduce design time.

Additional challenges include test cost and speed, digital/analog mixed-signal parts, verification, and design reuse.

TEST AND TESTABILITY

Unit test costs, driven up by increased numbers of pins, gigahertz speeds, and inaccessible cores, may soon exceed manufacturing costs. University of Texas/Austin is addressing reduced-cost test techniques for systems-on-chip, extension of self-test techniques to use the power of the processor to run tests for itself and peripheral cores at-speed, and on tools for test generation and testability insertion for bridging, crosstalk, and delay faults. University of Illinois/Urbana-Champaign has focused

on test data volume reduction, a new scan technique showing significant promise in reducing test application time and test data volume for system-on-chip designs. Testing and diagnosing failures in complex, heterogeneous systems are being investigated at Universities of Texas/Austin, Washington, and Illinois, with emphasis on self-test and design for testability. New failure modes such as crosstalk disturbances and analog-digital noise coupling are the focus at the University of Southern California and University of California/San Diego.



Buffers in Global interconnects are one technique used to eliminate crosstalk glitch effect (University of California at San Diego)

SYNTHESIS

Traditional synthesis separating technology-independent decomposition and, technology-dependent library binding, leads to sub-optimal realizations that cannot be improved incrementally. Work at the University of Michigan is focused on carefully interleaving of these stages. Researchers at the Universities of California/Berkeley and Colorado are addressing synthesis and improvements in quality of results and performance of the VIS and CUDD synthesis systems now in wide use among SRC members.

POWER ESTIMATION AND REDUCTION

Tools for the early estimation of power and for power reduction are critical in today's mobile applications, to avoid costly redesign, and to enable design exploration in a design-reuse environment. Researchers at the University of Southern California have developed techniques ranging from quasi-synchronous, derived clocking schemes and clock gating, to architectural- and operating system-level modeling to investigate how power is affected and can be reduced. At the University of Toronto, bottom-up and top-down power models have been used in the difficult task of estimating power early in the process, before the design has even reached the gate level.

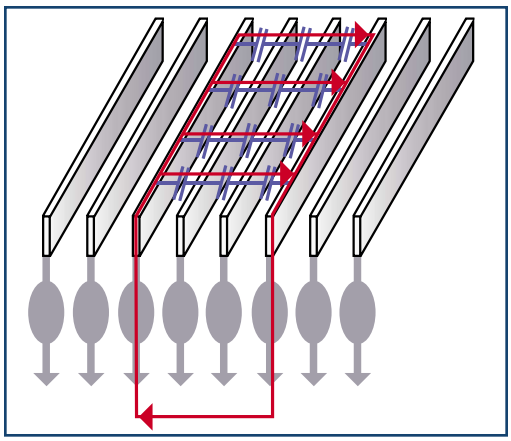
VERIFICATION

Researchers at the University of California/Berkeley, the University of Texas, and Carnegie Mellon University are on the forefront of formal verification work producing tools in use by SRC members. BDD and non-BDD techniques, coverage analysis, hybrid formal/simulation methods, model checking advances, and counterexample exposure techniques have been applied to multiprocessor memory protocols, data flow processor arrays, and other member company designs. These techniques are assisting in locating and correcting errors at the design stage and are assuring that correct silicon is shipped to customers.

Research Contributions

DEEP SUBMICRON EFFECTS

Present algorithms for extraction of parasitic capacitance and inductance are inadequate for gigascale and gigahertz designs. Carnegie Mellon University has demonstrated accurate, computationally efficient 3-D extraction algorithms to reduce design iterations.



Modeling inductance and capacitance concurrently is required to accurately assess potential problems with on-chip inductance (Carnegie Mellon University)

Noise coupling through the silicon substrate is a particular concern for mixed-signal circuits. Accurate simulation of noise coupling requires construction of an equivalent electrical network that can then be used in conjunction with circuit simulation tools. University of Illinois/Urbane Champaign is producing accurate and computationally-efficient, three-dimensional substrate analysis methods for use with circuit simulation tools to effectively attack this problem.

HETEROGENEOUS SYSTEMS AND CIRCUITS FOR TOMORROW'S APPLICATIONS

Today, there is increasing need to merge not only analog and digital functions on the same chip, but also to incorporate radio frequency (RF) elements, sensors, and micromechanical components. Simultaneously, technologies used to manufacture these systems are driving toward greater packing density and dramatically lower supply voltages. These trends pose enormous challenges for designers and technologists.

SYSTEM LEVEL DESIGN

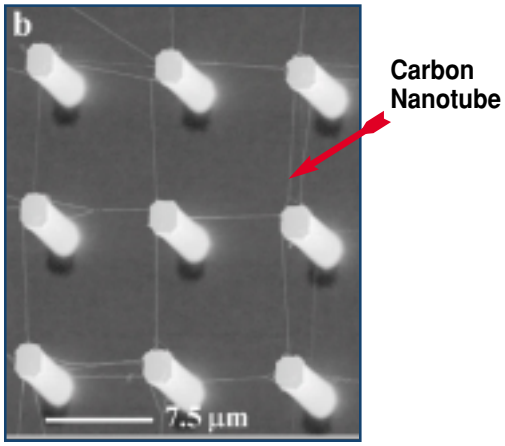
Heterogeneous designs require combinations of analog circuits, digital functions, mechanical elements, and embedded software in which power, speed, and packing density must be optimized. University of Wisconsin, Princeton University, Virginia Tech, and University of Illinois are investigating advanced processor architectures, power management, and communications circuits. New tools for evaluating and refining design options are being developed.

CIRCUIT DESIGN

Major research investments are being made in high-performance analog to digital conversion circuits. Advanced memory architectures that conserve power and dramatically improve performance are being developed. Novel digital logic circuits extending CMOS to clock rates of several GHz are being developed at the University of Washington. Advanced circuit designs that take advantage of Silicon-on-Insulator (SOI) technology are being developed at the University of Michigan.

FUTURE SEMICONDUCTOR DEVICES, MATERIALS AND PROCESSES

As feature sizes decrease toward the granularity of matter, phenomena, previously of secondary importance, play an increasingly important role in the performance of MOSFETs. These phenomena, with new materials, such as nanotubes, offer opportunities for novel information technologies that could displace or, perhaps, complement existing MOS technologies.



A network of carbon nanotubes connecting silicon pillar. (Provided by Professor H. Dai, Stanford University)

In 2000, SRC continued exploring new nanoelectronic technologies in areas such as molecular electronics, quantum computing, and spintronics that target long-term strategic goals, with a possibility for nearer-term impact. Examples include projects on quantum cellular automata (Notre Dame University) and on molecular electronics (University of California/Los Angeles).

These initiatives include:

- Integrated nanotubes for future electronics (Stanford University);
- Integrated molecular RAM and SRAM (Yale University);
- Background-charge insensitive single electron memories (SUNY/ Stony Brook);
- Nuclear spin based memory and logic (Harvard University);
- Integrated nanosystems with cooperative assembly of nano-quantum devices and vertical nano MOS (University of California/Los Angeles);
- Single-integrated hybrid-chip molecular quantum computer (University of California/Riverside.

SRC published a key document on Research Needs in Basic Science of Semiconductors (http://www.src.org/member/about/srcstaff_pubs.asp). This document seeks to identify and characterize research needs in the basic physical sciences that are required to sustain the exponential progress in nanoelectronics.

TECHCON 2000

Craig Barrett, President and CEO of Intel Corporation, delivered the keynote address for the Conference Banquet at TECHCON 2000.

By many accounts, TECHCON 2000 was the best technical conference hosted by SRC to date. The three-day event was packed with student presentations, awards ceremonies, and networking opportunities. Industry dignitaries at the conference included Robert Burger, Nobel Prize winner Jack Kilby, and keynote speakers Craig Barrett of Intel and Bijan Davari of IBM.

JobsFair — TECHCON's networking event — gathered 200 of the top students in microelectronic-related disciplines and representatives from 21 SRC member companies to provide a rich recruiting opportunity for interns and regular full-time hires. Several job offers were made on the spot as a direct result of JobsFair.

The 2000 Graduate Fellowship Program Annual Conference was held in conjunction with TECHCON 2000. The highlight of the GFP Banquet was the keynote address, which was delivered by Dr. William T. Siegle, AMD Senior Vice President and Chief Scientist.

TECHCON STATS AT A GLANCE

SRC-sponsored student presenters	153
Graduate Fellows and Masters Scholars presenters	44
Total SRC-sponsored student presenters	**197**
Technical paper sessions	25
Special sessions (Copper Contest & CSR Session)	2
Total Presentation Sessions	**27**
Faculty & Student attendees	268
Member Company attendees	359
SRC staff & Guest attendees	41
Total Conference Attendees	**668**
Member companies that participated in JobsFair	21
SRC Awards presented	82

Techcon 2000

Best In Session

199 students presented their research at TECHCON 2000 in five sets of five concurrent technical paper sessions with each set being followed by a TechFair poster session for papers presented in that set. Presentations were judged both on paper and poster presentation and the following "Best in Session" Winners were named for all twenty-five sessions.

SRC-SPONSORED STUDENT	PAPER TITLE
Stephen P. Nugent	An Ultra-Compact Empirical Model for Throughput Projection for Gigascale Integration
Gwang-Soo Kim	A Computationally Efficient Feature Scale Model for Copper Electrodeposition in the Presence of Additives
Noel Hoilien	Physical and Electrical Characterization of Zirconium Dioxide as a Gate Insulator
David Tully	Evaluation of Novel Hyperbranched Resist Materials for Next Generation Lithography
James G. Fiorenza	An RF Power LDMOSFET on SOI
Noppanunt Utamaphethai	Buffer-Oriented Microarchitecture Validation (BMV)
Azeez Bhavnagarwala	Fluctuation Limits on CMOS SRAM Scaling
Brian A. Floyd	CMOS Receiver Circuits for On-Chip Wireless Interconnection
Francisco Machuca	High Brightness III-Nitride Electron Emitters
Seongwon Kim	An Effective Defect-Oriented BIST Architecture for High-Speed Phase-Locked Loops
Rao Desineni	Test Analysis Using Fault Tuples
Hendrawan Soeleman	VT-Sub-CMOS: Robust Sub-Threshold Digital Logic
Zhijiong Luo	Temperature Dependence of Gate Current in Thin Ta(2)O(5) and TiO(2) Films
Matt Colburn	Recent Advancements in Step and Flash Imprint Lithography
Jir-Shyr Chen	Thermally Reworkable Underfill Materials: Controlled Tuning of Thermo-Mechanical Properties
Prakash Gopalakrishnan	Direct Transistor-Level Placement
Gaolong Jin	Uniform and Ordered Self-Assembled Ge Dots on Si-Based Substrates
Shyam Gannavaram	Ultra-Shallow, Super Abrupt Boron Doped Source/Drain Junctions with Above Equilibrium Dopant Activation for 50 nm and Beyond Using Low Temperature (500 C), In-Situ Boron Doped, Selective Si(x)Ge(1-x) Technology
Adam Pawloski	Photo-Acid Generation in Chemically Amplified Resist for Next Generation Lithography
Maura Jenkins	Interface Chemistry and Microstructure in Polymer/Epoxy Underfill Interface Systems
Steven A. Vitale	Characterization of High Density Plasma Etching of BCB Low-k Dielectric Films for Dual Damascene Integration
Atsushi Kawamoto	Atomic Scale Effects of Zirconium and Hafnium Incorporation at a Model Silicon/Silicate Interface by First Principles
Luca Daniel	Interconnect Electromagnetic Modeling Using Conduction Modes as Global Basis Functions
Paul Hyden	Improved Decision Processes Through Simultaneous Simulation and Time Dilation
Hsin-Chiao Luan	Germanium Photodetectors Integrated on Si for Si Optical Interconnects
Kevin Kidoo Lee	The Effect of Size and Roughness on Light Transmission in a Si/SiO(2) Waveguide: Experiments and Model
Charles M. Perkins (Fellows Award)	Electrical and Material Properties of ALD ZrO(2) Gate Dielectric

Techcon 2000 Awards

LANDMARK INNOVATION AWARD

Dr. Farhang Shadman, Director of the NSF/SRC-funded Engineering Research Center for Benign Semiconductor Manufacturing at the University of Arizona, received the first-ever SRC Landmark Innovation Award, along with a $10,000 cash prize. Dr. Shadman has provided four patents to SRC members enabling the creation of environmentally-friendly closed manufacturing systems which reuse gases and ultra-pure water during semiconductor fabrication.

ARISTOTLE AWARD

Professor Rafael Reif, of the Massachusetts Institute of Technology, was presented the Aristotle Award in recognition of his commitment to the educational experience of SRC students and the profound and continuing impact he has had on their professional careers. This award acknowledges outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project. Professor Reif has graduated some 40 Master's students and over 30 PhDs, including three SRC Fellows.

TECHNICAL EXCELLENCE AWARD

Lawrence T. Pileggi, professor of electrical and computer engineering at Carnegie Mellon University, received SRC's Technical Excellence Award in recognition for his work on "Simplified Inductance and Capacitance Extraction Algorithms," which has had a direct impact on the productivity and competitiveness of the semiconductor industry. It is estimated that his research findings may save several months in time-to-market.

The SRC Technical Excellence Award is given annually to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research, who are ground breakers and leaders in their fields, and who are regarded as model collaborators with their colleagues in the SRC member community.

MAHBOOB KHAN MENTOR AWARD

The Mahboob Khan Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from AMD, is presented to those individuals who have made significant contributions to the SRC community in their roles as an Industrial Liaison. Recipients represent "ideal mentors" whose commitment more than enhances the SRC research program.

Recipients of the 2000 Mahboob Khan Awards, which were presented at TECHCON, include:

Robert Allen, IBM Corporation (not shown)
Prashant Sawkar, Intel Corporation (not shown)

Mark Mason
Texas Instruments

David F. Reed
Advanced Micro Devices

INVENTOR RECOGNITION AWARDS

In addition to sponsoring the research efforts of many talented SRC university researchers, SRC makes a special effort to recognize and reward those researchers whose efforts lead to patentable inventions. At TECHCON 2000, SRC presented Inventor Recognition Awards to more than 46 university researchers and students.

Student Programs

The SRC community continues to see an outstanding return on its investment in SRC students. Through internships and permanent hires, students transfer research developed in the university community and build the network of highly qualified researchers both in industry and in academia.

In increasing numbers, students are forging the links between the individual member companies and the SRC community by serving as Industrial Liaisons and Technical Advisory Board Members. Student Programs managed by SRC include the Graduate Fellowship Program, the Master's Scholarship Program and three Undergraduate Engineering Programs.

GRADUATE FELLOWSHIP PROGRAM

The Graduate Fellowship Program is in its fifteenth year and continues to be successful in attracting many of the best U.S. citizen/permanent resident students to doctoral study in disciplines of interest to the semiconductor industry. The number of company-named Fellowships grew in 2000 to fifteen (12 in 1999) as the membership recognized the value of this program to the industry.

Of the 197 technical papers that were presented at TECHCON 2000, 40 were presented by students participating in the Graduate Fellowship Program. Of those 40, seven won "Best in Session" awards. For more about TECHCON 2000, see page 14.

MASTER'S SCHOLARSHIP PROGRAM

The Master's Scholarship Program was created in 1995 and targets underrepresented minorities and women with outstanding potential in disciplines of interest to the semiconductor industry. This program will be opened to company-named scholarships in 2001.

THE UNDERGRADUATE ENGINEERING PROGRAMS

In June of 2000, the SIA Board of Directors approved funding for the Undergraduate Engineering Programs to be managed by SRC through the SRC Education Alliance. Three programs were funded and two were initiated in 2000. The third program is scheduled to begin in early 2001.

- **The Undergraduate Research Assistants Program** targets qualified students early in their undergraduate careers and connects them with SRC-sponsored research programs. The program also provides mentoring by graduate students and industry personnel. Fifty-three Assistantships were awarded for the 2000-2001 academic year.
- **MOSIS** is an established program centered at the University of Southern California, which provides students with the ability to fabricate their VLSI designs, thereby producing designers with real experience. The MOSIS program serves about 5000 students in design courses each year. SIA/SRC funding will allow continuation of this program originally funded by DARPA and NSF.
- **The Industry Experience for Faculty Program** is scheduled for implementation early in 2001 and will target faculty at non-SRC-funded schools who do not have connections to the semiconductor industry.

STUDENT STATS AT A GLANCE

Total SRC-supported students 1091
(including Graduate Fellows and Masters Scholars)

Total SRC graduates in 2000 183

Graduate Fellowship Program Stats

Total fellowships in program 64

Company-named fellowships 15
(3 AMD, 2 IBM, 1 Intersil, 3 Motorola, 2 National Semiconductor,
1 NIST, 1 Novellus Systems, 2 Texas Instruments)

Research Fellowships (funded by Hewlett-Packard & AMD) 2

Students to complete program in 2000 13
(9 joined member companies and 2 joined university faculties)

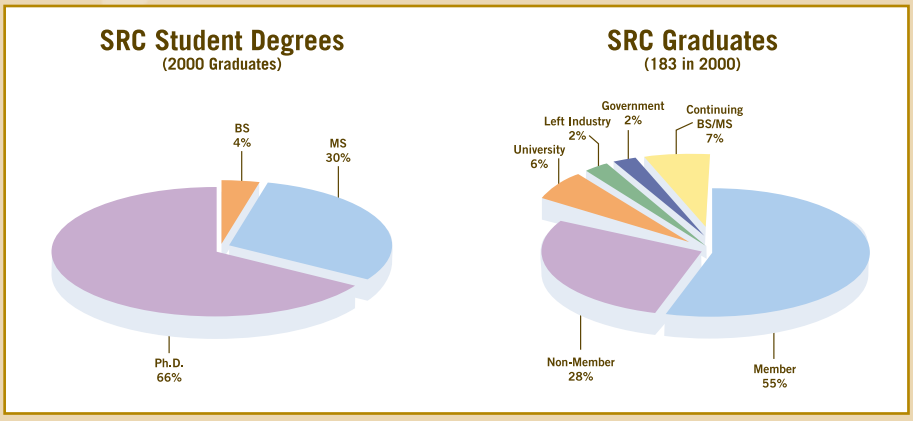
Graduate Fellows who presented papers at TECHCON 2000 40

Master's Scholarship Program Stats

Total scholarships in program 13

Students to complete program in last two years 9
(4 are pursuing Ph.Ds, and 3 have joined SRC member companies)

Master's Scholars who presented papers at TECHCON 2000 4



Industrial Liaison Program

The SRC Industrial Liaison Program is a powerful partnership that brings together the university community and experts from the semiconductor industry to promote an environment of cooperation. During 2000 nearly 500 industrial liaisons participated in the Industrial Liaison Program. This major industry commitment enabled the best technical people to guide, shape, and support SRC research efforts. The Industrial Liaison Program provides three vital functions:

DEVELOPING THE WORKFORCE

Industrial Liaisons serve as student mentors to provide guidance and inspiration to graduate students preparing to enter the semiconductor industry. They help the students achieve academic excellence through real-life exposure to industrial practices. Liaisons may arrange for internships or summer hires; they also frequently serve on students' thesis advisory committees or final examination committees.

ALIGNING RESEARCH

Industrial Liaisons encourage dialogue and technology exchange between the university and industrial communities. They assist by providing expertise, equipment, and feedback about industrial needs, as well as guidance and material help during all phases of the research. In the end, research results are realized faster, are more closely aligned with real industrial uses, and use the most relevant, state of the art technology that can be made available.

TRANSFERRING TECHNOLOGY

Liaisons work with researchers, member companies, and SRC to bring knowledge back to industrial sponsors in an expedient, cost-effective way. Their focus is on maximizing the return for their company. Liaisons work with the researchers during the entire life of a funded task to ensure that results will be made available in a form that is of use to industry. Liaisons are most effectively positioned to ensure that exciting new research is actually implemented in a timely manner.

INDUSTRY LIAISONS BY MEMBER COMPANY

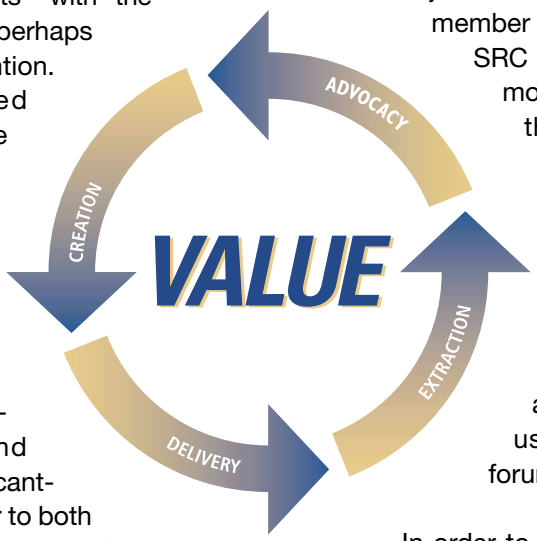
AMD	42
Conexant	10
Hewlett-Packard	9
IBM	84
Intel	111
LSI Logic	12
Motorola	88
National Institute of Standards Technology	5
National Semiconductor	8
Novellus	5
Texas Instruments	53
Other Companies	26
Total Liaisons that participated in 2000	**453**

2000 Value Delivery

In the fourth quarter of 1999, SRC formed a directorate, called the Value Chain to support, service, and satisfy its members. The Value Chain works to deliver value by:

- Identifying valid member needs;
- Developing and managing a research portfolio;
- Monitoring member satisfaction;
- Responding to identified shortcomings.

In 2000, all science areas worked with the members' technology advisory boards to develop and refine "technology needs statements" with the mixed signal domain perhaps getting the most attention. New, well-received approaches to the reviewing, ranking, rating and selecting of white papers and proposals were tested, including utilization of the Internet. Procedures for contract reviews and reporting were significantly streamlined in order to both simplify the procedures and to provide more timely technical information to the members via the SRC Web site, and a record number of publications were placed on the SRC Web site for member access.



In order to enhance the ability of the Technical Advisory Board (TAB) members to effectively deliver value to their members, all of their handbooks were updated and an Orientation Course for new TAB members was created and implemented.

The Industrial Liaison program, which is highly valued by the graduate students and also provides member companies with valuable, early research results, was revitalized under a new program manager and reached a record number of industrial liaisons.

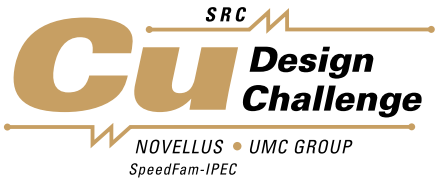
The students, perhaps the most valuable output of the SRC programs, were showcased at TECHCON 2000 where 197 papers were presented by them on their leading-edge research.

A major effort went into identifying member needs relative to the SRC Web site itself. After months of intense effort, the new Web site framework was unveiled at TECHCON 2000. The members liked what they saw, including the ease of navigation and the ability to collaborate using the Web site forums.

In order to improve the monitoring of our members needs, the annual member satisfaction survey was refined, plus telephone surveys of key members of both the Board of Directors and the Executive Technical Advisory Board were conducted in addition to their written surveys. The level of member satisfaction was measured to increase year over year, as well as associated measure of value (weighted relevance index) to the members.

SRC Copper IC Design Challenge Completed

In 2000, SRC completed its first design contest. The "Copper IC Design Challenge" was fully sponsored by members Novellus Systems and UMC with additional support from SpeedFam/IPEC. Two key objectives for this contest were to raise the level of interest and knowledge in the area of IC design within the universities and to increase interest in designing with copper interconnects, accelerating the adoption of this relatively new semiconductor copper technology within the future design community. The contest was an overwhelming success.



43 teams entered the Contest and over 140 students were involved. Judging criteria focused on creativity of design, impact of the design on future applications, design efficiency, test procedures, correlation of test results to the design performance predicted in Phase 1 and completeness of the materials submitted. Thirteen teams with over 50 students completed Phase 2 involving fabrication of their designs in copper. Five Phase 1 winners were recognized at ISSCC 2000 in February with $20K going to each of their universities. Three top teams were selected from among the 13 Phase 2 participants. These three teams presented their designs at TECHCON 2000, a student technology conference which was held Sept. 21-23 in Phoenix, Ariz. For more on TECHCON 2000, see pages 14-17.

The University of Minnesota captured first place and a $35,000 award with its "RF Front-end Design with Copper Passive Components" concept. The team, led by Professor Ramesh Harjani, included members Jonghae Kim, Mingta Hsieh and James P. Koeppe.

The topic of the second-place design, submitted by University of Florida, was "A Wireless Clock Distribution System: Clock Receiver and Transmitter Circuits." This team received a $25,000 award, was led by Professor Kenneth O and included Brian A. Floyd and Chih-Ming Hung.

The third-place award of $15,000 went to Carnegie Mellon University for its project, "CMOS Micromachined RF Components." The team, led by Professor Gary Fedder, included Hasnain Lakdawala, Hao Luo and Xu Zhu. The cash prizes will support integrated circuit (IC) design education programs at these universities. In addition, ten other finalist teams were awarded cash prizes of $15,000 each for successfully completing both phases of the contest.

This contest has provided an excellent opportunity for the students and faculty to demonstrate their creativity using a leading-edge copper technology. SRC is strongly considering future sponsored contests as a way to increase faculty and student interest at both the graduate and undergraduate levels in microelectronics and design, and a way to provide increased industry support to student activities in these areas.

SRC Web site

Since its 1996 inception, SRC's Web site has evolved at much the same pace as the Internet. In 2000 alone, site content grew by nearly 30% with a highwater mark of 22,000 pages of content by year-end. Site usage increased at the same pace with over 3800 active users registered by December, 2000. Based on these numbers, SRC has clearly established a prominent and successful value delivery mechanism via the Internet.

Significant new Web site capabilities were brought online in 2000, including:

- **Internationalization:**
  Early in the year, SRC established processes, addressed all necessary legal issues and brought online the appropriate technology to enable the Web site to effectively serve an International membership.
- **Students Online:**
  SRC-supported students were provided with online accounts so they could be integrated into our web community.
- **New Site Previewed:**
  A completely redesigned Web site was previewed at Techcon 2000 in Phoenix, Arizona and received positive feedback on its increased functionality.

The new SRC Web site was designed using one overriding premise: Embrace the latest in web-based technology to better serve the SRC community, but DO NO HARM to its success to date. Highlights of the new site include:

- A fully redesigned site look-and-feel to simplify navigation and target content;
- An integrated News function designed to highlight new content. This News feature will ultimately adapt to the identity and interests of each user;
- Redesigned Science Areas pages that are easier to navigate because of their consistency;
- Dynamically-served pages that are synchronized with SRC's corporate database. The goal: more flexible, up-to-date responses to Members research information needs;
- Discussion forums to facilitate online collaboration within the SRC community. The SRC Forums technology is designed for flexibility and can be easily adapted to meet Member company collaboration needs.

The underlying infrastructure of the new site provides a vast opportunity to rapidly deploy new capabilities and functionality in the coming year with a particularly strong focus on enhancing collaboration within the industry.

Industry Assignee Program

The Industry Assignee Program was designed to ensure that the needs of Member companies play an active role in shaping the day-to-day operation of SRC's global, leading-edge, collaborative research program. Through this program, Assignees maintain their current employment status at their respective Member companies, but work on-site with SRC staff and management. Assignees use their unique understanding of their company's and the industy's R&D interest to have a direct and meaningful impact on the daily activities at SRC. In exchange for that invaluable perspective and input, Member company employers receive a rebate on their SRC membership dues. Assignees may work full-time on-site at SRC or split their time between SRC and their regular employer. The 2000 Industry Assignees are:

Lawrence Arledge, Texas Instruments
Mr. Arledge served as the Physical Design Thrust Program Manager in Computer Aided Design & Test Sciences and the Circuits Design Thrust Program Manager in Integrated Circuits & Systems Sciences in 2000. He is also a Senior Member of the Technical Staff in the Mixed Signal Products Group at TI.

George Bournioff, Intel Corp.
Dr. Bournioff is the Advanced Devices Technologies Thrust Program Manager in Nanostructure & Integration Sciences. He is also a senior program manager in the Strategic Research Group of Intel where he serves as co-chairman of the Semiconductor Technology Committee. He holds BS, MS and P.hD degrees in physics from the University of Texas/ Austin.

Dale Edwards, Advanced Micro Devices
Mr. Edwards has been serving as the Circuit Design Thrust Program Manager in Integrated Circuits & Systems Sciences since January 1999.

Industry Assignee Program

Jyh-Shyang Jenq, United Microelectronics Corp.
Dr. Jenq is the Front-End Processes Thrust Program Manager in Materials & Process Scienc. He is also an EDRAM Process Integration Manager for UMC and holds a BS in Forestry and MS and Ph.D degrees in Materials Science from the University of Wisconsin/Madison.

William H. Joyner, Jr., IBM Corp.
Dr. Joyner is the Director of Computer-Aided Design and Test Sciences. Dr. Joyner is also the co-chair of the Design TWG of the International Tehnology Roadmap for Semiconductors [panel chair of the 2001 Design Automation Conference, and associate editor of ACM Transactions on Design Automation of Electronic Systems].

Frank Robertson, Intel Corp.
For part of 2000, Mr. Robertson served as the program manager for the Front-End Processes Thrust in Materials and Process Sciences. He later transitioned to become the Factory Systems Program Manager in Nanostructure & Integration Sciences.

Quat T. Vu, Intel Corp.
Dr. Vu is a senior staff member of Intel Santa Clara, CA. He is on assignment to SRC as the Packaging and Interconnect Thrust Program Manager in Nanostructure & Integration Sciences. He holds MS and Ph.D degrees in Electrical Engineering from California Institute of Technology.

Intellectual Property

The value of SRC membership is enhanced and protected by providing intellectual property assets spanning numerous SRC sponsored university research programs. Intellectual property (IP) assets exist to support SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs to SRC member companies. SRC's significant portfolio of intellectual assets serves to minimize the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship.

In return for sponsorship, SRC receives non-exclusive, worldwide, royalty free licenses to IP resulting from such research programs. Although IP rights are owned by the university, IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results is provided, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to provide a level playing field for members by ensuring that those who utilize SRC sponsored technologies do so only within the scope of a valid license.

During 2000, seven SRC-sponsored U.S. patents were issued, bringing the total U.S. portfolio of SRC patents to 168. This year's patents relate to materials and processes, novel device structures and devices, copper interconnect technology, optoelectronics, waveguide technology, resists and their processing, and advanced SOI (silicon-on-insulator) devices. In addition, several SRC sponsored foreign patents issued which were related to previously granted U.S. patents. SRC's significant patent portfolio supports both U.S. and global member company operations in numerous countries around the world. For the first time, issued patent information was added into SRC research catalog web pages so members can appreciate a patent in light of the research program from which it arose. Soon, SRC's new Web site will permit members to submit realtime queries into SRC's IP database to obtain status on pending and issued patents as well as SRC-sponsored software.

In addition, SRC provides over 200 software programs, software models, and technical databases to member companies. Software and database IP licenses from SRC sponsored research programs represents a growing and complementary IP portfolio. Members are directed to the online software directory at www.src.org for further details. SRC members also receive non-exclusive, worldwide, royalty free intellectual property licenses in applicable software programs and technical databases.

The Intellectual Property highlight of 2000 was the awarding of the inaugural Landmark Innovation Award to Dr. Farhang Shadman, of the University of Arizona, at TECHCON 2000. Jack Kilby, a recent recipient of the Nobel Prize, presented the award to Dr. Shadman for his notable and valuable inventions in environmentally friendly semiconductor fabrication technologies, which has provided long term and significant benefits to SRC members.

U.S. PATENTS ISSUED IN 2000

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Passivated copper conductive layers for microelectric applications	Ding Peijun W. Lanford Wei Wang	Feb. 10, 1998 May 2, 2000	6,057,223	SUNY/ Albany
Systems, methods and computer program products for detecting the position of a new alignment mark on a substrate based on fitting to sample alignment signals	Xun Chen Thomas Kailath Amir Ghazanfarian Mark McCord R. Fabian Pease	May 21, 1998 May 16, 2000	6,064,486	Stanford University
Photoresist compositions comprising norbornene derivative polymers with acid labile groups	David Medeiros U. Okoroanyanwu Grant Willson	Mar. 7, 1997 Aug. 15, 2000	6,103,445	Univ. of Texas/ Austin
Optoelectronic integrated circuits having polycrystalline silicon waveguides therein	A. Agarwal Marcie Black Jim Foresi Lionel Kimberling Debra Koker	Oct. 13, 1998 Aug. 22, 2000	6,108,464	M.I.T
Films for use in microelectronic devices and methods of producing same	Jeffry Kelber	Apr. 10, 1998 Sept. 5, 2000	6,114,032	Univ. of North Texas
Silicon-On-Insulator Transistors having improved current characteristics and reduces electrostatic discharge susceptibility	Mansun Chan Chenming Hu Ping Ko Hsing-Jen Wann	Sept. 10, 1999 Sept. 19, 2000	6,121,077	Univ. of California/ Berkeley
Methods for decreasing surface roughness in novolak-based resists	G. Reynolds James Taylor	Oct. 6, 1998 Dec. 19, 2000	6,162,592	Univ. of Wisconsin

Focus Center Research Program

SPONSORS:

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- Analog Devices
- Conexant
- Cypress
- IBM
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- Xilinx

Semiconductor Industry Supplier Association:

- Air Products
- Applied Materials
- Novellus
- SCP Global
- Speed-Fam
- Teradyne
- Veriflo

DUSD (S&T):

Deputy Undersecretary of Defense for Science & Technology

DESIGN AND TEST

Two years ago, the University of California at Berkeley became the lead university for the Design and Test Focus Center (Gigascale Silicon Research Center). **Professor Richard Newton** is the center's director. The Design and Test Center's research agenda addresses concepts such as component/communication-based design, constructive fabrics, fully programmable systems, calibration of achievable design, validation, power and energy.

UC/BERKELEY

CMU
MIT
Penn State
Princeton
Purdue
Stanford
UCLA
UC/San Diego
UC/Santa Barbara
UC/Santa Cruz
Univ. of Michigan
UT Austin
Univ. of Wisconsin

INTERCONNECT

The Interconnect Focus Center is based at the Georgia Institute of Technology. **Professor James Meindl** has been the director since the center was established, almost two years ago. The center's research teams examine six major tasks: system architecture and circuit innovation, physical design tools, novel communications mechanisms, integrated input/output interconnects, materials and processing, predictive modeling and metrology.

GEORGIA TECH

MIT
Stanford
RPI
UCLA
Univ. of Albany

MATERIALS, STRUCTURES AND DEVICES

Recently, the Massachusetts Institute of Technology was designated as the lead university for a new Materials, Structures and Devices Focus Center. **Professor Dimitri Antoniadis** is the director. This center will research sub-10-nanometer silicon-based FETS, silicon-based quantum-effect devices, molecular and organic semiconductor electronics, nanotube electronics and modeling and simulation.

MIT

Cornell
Princeton
Purdue
Stanford
UC/Berkeley
UCLA
Univ. of Albany
UT/Austin
UVA

CIRCUITS, SYSTEMS AND SOFTWARE

A new Circuits, Systems and Software Focus Center was also recently created, with Carnegie Mellon University as the lead university. **Professor Rob Rutenbar** is the director. The center's research will focus on analog/mixed signal circuit analysis and synthesis, system level technologies and software solutions to CMOS limitations.

CMU

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