SEMICONDUCTOR RESEARCH CORPORATION®

2002 ANNUAL REPORT

CELEBRATING 20 YEARS

Celebrating 20 years

By 1981, university research in silicon technology had almost vanished and industry research was declining rapidly. By creating Semiconductor Research Corporation (SRC) in 1982, industry defined mechanisms permitting cooperation in long-range research to meet common needs while preserving competition. The creation of SRC re-established the importance of silicon microelectronics research and, over the ensuing two decades, has provided both the knowledge and the appropriately educated scientists and engineers for continued advancement of the industry. We are pleased, proud, and congratulate the team composed of member company personnel, university researchers, and SRC staff for their significant accomplishments during the first 20 years.

MEMBERS

Advanced Micro Devices, Inc.
Agere Systems (formerly Lucent)
Chartered Semiconductor Manufacturing
Conexant Systems, Inc.
Eastman Kodak Company
IBM Corp.
Intel Corp.
LSI Logic Corp.
Motorola, Inc.
National Semiconductor Corp.
Texas Instruments, Inc.
UMC Group

SCIENCE AREA MEMBERS

Axcelis Technologies
Cadence Design Systems, Inc.
Mentor Graphics Corp.
Novellus Systems, Inc.
Shipley Company
Synopsys, Inc.
Ultratech Stepper, Inc.

ADJUNCT MEMBERS

Hewlett-Packard Company

ASSOCIATE MEMBER

The MITRE Corp.

AFFILIATE MEMBERS

Coventor, Inc.
Integrated Systems Engineering, Inc.
Mission Research Corp.
Numerical Technologies, Inc.
PDF Solutions, Inc.
SILVACO International
Tessera Technologies, Inc.
Torrex Equipment Corp.
Ziptronix, Inc.

US GOVERNMENT PARTICIPANTS

DARPA
National Institute of Standards and Technology
National Science Foundation

STRATEGIC SEMICONDUCTOR INDUSTRY PARTNERS

International SEMATECH
Semiconductor Industry Association

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Vision

Semiconductor Research Corporation® (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

Mission

SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the International Technology Roadmap for Semiconductors (ITRS), focusing on universities
- Relevantly educated university graduates with high rate of placement in member companies
- Global scope, encompassing membership, performer base, government leveraging and consortial relationships
- Capability to operate in multiple modes distinguished by time horizon, research scope, management style, membership and organizational structures
- Complementary structuring and coordination of research programs to maximize overall research coverage at minimum cost
- Timely transfer of research results
- Collaboration to enhance commercialization and leveraged research

Message from the President

Twenty years ago, the Semiconductor Industry Association (SIA) convened an extraordinary group of visionaries who clearly understood that innovation creates competitive advantage and propels every company in our industry forward.

These industry leaders also realized that research fosters innovation, yet silicon research at the nation's universities was virtually non-existent. No single company could afford to focus sufficient university attention on silicon technology to meet the industry's silicon research needs.

Semiconductor Research Corporation was their solution, conceived and established to address this research dilemma through collaborative fundamental research. In doing this through universities, SRC also would help fill the industry's need for more relevantly educated students, who could immediately bring their university research experience and familiarity with the industry's needs into the workplace and quickly become productive employees.

SRC was incorporated in February 1982. I was hired as the Executive Director a few months later and operations began on May 1, 1982. Research Triangle Park was chosen as the permanent site because of its setting among major research universities and its supportive state government. We were up-and-running in Research Triangle Park by September 1982 with 11 charter industry members. Our first two employees, Richard Alberts and Robert Burger were hired, and we held our first Technical Advisory Board meeting. SRC's first request for proposals was issued, and in November, Hewlett Packard became our first recruited member company. Centers of Excellence were established in Microsciences and Technology at Cornell, in Computer Aided Design at the University of California at Berkeley, and in Systems and Architecture at Carnegie Mellon; five additional awards were made from 166 proposals resulting from our first request for proposals by year's end.

In 1983, SRC's membership grew to 24 companies, its first patent was issued, and 50 additional research contracts were initiated, involving 30 universities, 100 faculty and 125 graduate students.

The basic foundation for SRC was firmly established by the end of 1983, and SRC was already making an impact. During the next several years, we established relationships with the National Science Foundation and the National Security Agency. Erich Bloch, our first board chair, Bob Burger and I recognized the need for a consortium-based development effort for the industry that eventually was formed and located in Austin, Texas. Bob Burger suggested the name for this new consortium: SEMATECH.

I "double-hatted" as Managing Director of SEMATECH during its first year. The focus at that time was to secure congressional support for the government's role in this new venture. Working closely with Clark McFadden, SRC's current corporate attorney, and company representatives, a strategy to secure the support of Congress was developed and carried out. Austin, Texas, was selected as the site for SEMATECH, and a budget was also created to support university Centers of Excellence at U.S. universities. These Centers would conduct research supportive of SEMATECH's new mission. SRC was selected to manage these Centers, which contributed valuable research efforts for about 10 years, after which they were phased out due to changes in SEMATECH's funding sources.

In the early years of SRC, our management team believed strongly that we needed to structure research roadmaps to guide our research activity. Accordingly, we put into place a series of roadmaps which eventually, with the support and guidance of technical experts from other members, evolved into the present-day International Roadmap for Semiconductors (ITRS) that is managed by the SIA today.

Our first TECHCON was held in Atlanta, Georgia, in 1988. Our seventh TECHCON will be held in Dallas, Texas in 2003. This conference features technical papers presented by students, poster sessions by students, and recruiting events and presentations by industry leaders. The keynote address for TECHCON 2000 was given by

Craig Barrett, CEO of Intel Corporation. The 2003 TECHCON keynote address will be given by Paul Horn, Senior VP of Research for IBM. TECHCON has been compared by our members to the best technical conferences. Additionally, it offers our members a good opportunity to connect with our graduate students as potential employees.

New levels and models of cooperation with the federal government have highlighted the past decade. The National Science Foundation and SRC announced its first joint Engineering Research Center at the University of Arizona. DARPA and SRC have co-funded the Lithography Network for over six years. The Focus Center Research Program was conceived by the SIA, with SRC being asked to manage it through a new subsidiary, called the Microelectronics Advanced Research Corporation (MARCO). Despite a dramatic economic downturn during the last few years, high satisfaction with the Focus Center program has led to its expansion and additional funding by US Department of Defense and DARPA.

As the integrated circuit industry neared the millennium, its structure began to change, becoming more segmented and global. SRC kept up with the trend toward globalization by welcoming new international members, like UMC in Taiwan, and initiating new membership recruiting efforts for suppliers and other related companies. We also responded to industry changes by offering more customized research programs, new participation and membership options, and new approaches to managing intellectual property. We have also increased our collaboration with other consortia, such as STARC of Japan and International SMT (formerly SEMATECH).

International research cooperation is critical to SRC's future. The industry relies on SRC to address the research needs outlined in the ITRS. The growing gap between the estimated cost of ITRS research needs and the research actually funded has reached more than US $400 million per year. Factoring the redundancy of research conducted around the world, combined with inaccessibility due to geographic or language barriers, the gap actually rises for any one region, such as the U.S., to between US $700 and $800 million dollars.

To help address this gap, SRC must grow. We must recruit more new members from the diverse segments of the industry. This requires us to continue to enhance our comprehensive and compelling Value Proposition. We must establish SRC's presence in new geographic locations and expand our relationships with international universities, governments and consortia. Globalization in all aspects of SRC's activities, from membership to university research labs, will help provide graduates in the regions where they are needed and will also help to reduce the research funding gap.

In looking to the future, SRC must strive to establish research programs that are aimed at critical challenges identified in the ITRS as well as to anticipate member needs that may be beyond or outside the ITRS and that are suitable for the university research environment. We must also seek to balance research efforts that address common as well as diverse needs of members. Our research scope must be expanded to address new and emerging needs that include areas such as integrated optoelectronics, ultra-low power systems, embedded software and innovative patterning techniques.

As we globalize, we must put into place global student programs to address broad technical talent needs in regions where members have a strong presence. In parallel, we need to strengthen our undergraduate and master's programs to create a pipeline for the technical talent pool.

SRC has, in effect, created a virtual and geographically diverse university-based research laboratory in the United States in the last 20 years. Our task now is to globalize that virtual research laboratory to enhance research capability and best serve member needs.

The integrated circuit industry is changing. Various industry segments will continue to adapt and change as the industry adjusts to changing markets and economic conditions. SRC must continually seek to adapt its business strategies, operational practices, and member participation structure to meet these changing needs and seek to leverage the new opportunities that are presented. In doing this, we always seek to maximize value to our members by strengthening core competencies, increasing financial leverage for our members, and optimizing our Value Proposition.

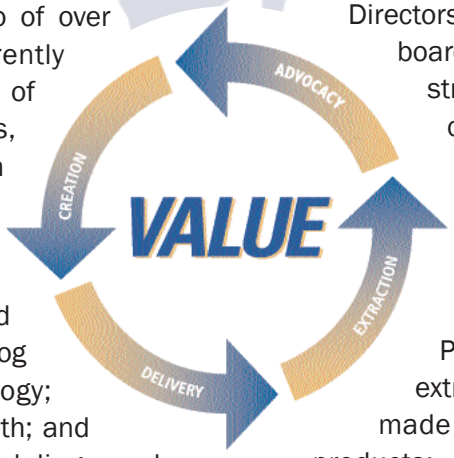
Overall, SRC is committed to being agile, vital and dynamic as it responds to the continuously changing needs of the industry. Our vision is to be the world's premier research management consortium.

Company Profile

Pioneers in collaborative research®

In 2002, Semiconductor Research Corporation celebrated its 20th anniversary. Over the past 20 years the industry has invested nearly US $600 million through SRC, and well over 3,000 scientists and engineers have received advanced degrees from SRC supported programs.

SRC's core directed-research program has a continuously evolving portfolio of over 350 projects that are currently targeted at the full spectrum of semiconductor technologies, including: circuit and system design; design tools; test and testability; materials and processes; packaging and interconnect; advanced patterning; mixed signal/analog technologies; metrology; environmental safety and health; and advanced device and modeling and simulation. We have described significant results from the research efforts in the year 2002 **(see pages 6-12).**



MARCO, an SRC subsidiary, currently has four Focus Center Research Centers conducting complementary research projects that are described in the MARCO annual report.

SRC continued to enhance student programs in its core program to ensure development of the highest quality talent for our member companies. In addition, the SRC Education Alliance, described on **page 14,** addresses the need for developing undergraduate talent relevant to the industry.

Because the semiconductor industry and its International Technology Roadmap (ITRS) for Semiconductors have become global, SRC now has members and university research programs in countries around the world. In order to enable an effective approach for delivering value to our member companies, research results and publication are posted on the secured web site for member access. In 2002, a record number of publications and deliverable results were placed on the site, along with patents and software to which the members have royalty-free access. Also in 2002, the site was used for real-time collaboration as well as threaded discussions.

Through the combined efforts of the Board of Directors, our various technical advisory boards and SRC staff, our research strategy and operational plans are continually refined to produce value, satisfying the members as evidenced by the annual member satisfaction survey. The survey addresses all four dimensions of the Value Proposition—creation, delivery, extraction, and advocacy—that are made available via SRC's primary products: Research Results, Relevantly Educated Talent, Integrated University Research Capability, and Networking.

We have continued to hone the processes and tools associated with the delivery of SRC value to our member companies. Also, we have continued to refine the mechanisms and support that are provided to facilitate the extraction of maximum value in the most cost-effective manner for our member companies, as evidenced by the increased use of electronic meetings utilizing both the SRC web site and "net-meeting" software. Finally, we work with the representatives of our member companies on the Board of Directors and the various advisory boards to continuously revitalize our products, programs, processes and systems to enhance value for our members.

Company Profile

Year 2002 was another difficult year for the industry and for SRC. The marketplace has undergone significant changes that have, in turn, changed the complexion of the industry, research needs, and the research budgets. As a result, preparation for 2003 presented even greater challenges to maintain critical research programs and to maintain SRC's reputation as a preferred sponsor of university research. Several examples of the dynamic nature of our business and the value that the community of our consortium has brought forth in the year 2002 are presented in this report. This abbreviated report can only describe some of the key accomplishments, major initiatives, and important events of 2002 that demonstrate the value, strength, and agility of the consortium, for example:

- Our Executive Technical Advisory Board (ETAB) continued to provide high-level technical/strategic directions to shape the research portfolio. The ETAB also developed the architecture for a modified Science Area structure, which will be implemented in 2004.
- The SRC Board of Directors approved several Strategic Initiatives that impact SRC's business model and practices that would help SRC to enhance its value to all segments of the industry.
- Professors Supriyo Datta and Mark Lundstrom of Purdue University were the recipients of the Technical Excellence Award for their work in the area "Device Physics and Simulation of Nanoscale MOSFETs."
- Well over 100 Fellows, Scholars, industry representatives, and SRC staff attended the 2002 Graduate Fellowship Program Annual Conference in September. The keynote address was delivered by Tom Engibous, Texas Instruments Chairman and CEO. Ninety-five percent of attendees rated the conference greater than four on a five-point scale.
- Ten SRC-sponsored U.S. and foreign patents were issued, bringing the total portfolio of SRC-licensed patents to 195, all of which can now be queried by members on the SRC web site.

There were many other noteworthy 2002 accomplishments in other areas not described in this abbreviated report, such as:

- Member companies assigned Industrial Liaisons to work with researchers on a record percentage of tasks, a strong indicator of the ongoing efforts to derive value from the technology and to mentor the students toward a rewarding career in the industry.
- SRC successfully launched an e-meeting initiative to better enable remote-attendance at meetings by utilizing state-of-the-art teleconferencing and web-based solutions. Not only has this strategy provided a means to reduce travel costs but also to significantly enhance participation and collaboration.
- SRC continued to expand the scope of its web site capabilities by providing integrated, simple-to-use web-based forms to better collect and update information. These included online submission of publications descriptions and full documents, software descriptions, student information and full resumes, web site user information updates and the first deployment of online event registration with e-commerce secured credit-card transactions.
- In 2002, SRC clearly saw the benefits of web-based efforts. The SRC web-site saw a 22% increase in logins and a 48% increase in page hits over 2001 usage data. The number of individuals within the SRC community that logged into the site in 2002 increased to over 3,100 in 2002 -- an increase of nearly 20% over 2001.

SRC RESEARCH: Enabling Silicon Nanoelectronics

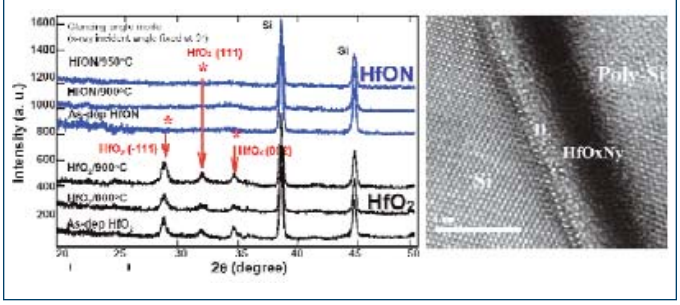
Formidable scientific and technology challenges must be overcome to design and produce integrated circuits and systems that sustain the traditional exponential improvements in performance as characteristic features scale from tens of nanometers to angstroms. Semiconductor Research Corporation operates a comprehensive research program at approximately 70 universities involving over 250 faculty and 1,000 graduate students that provides innovative solutions to industry technology challenges. Summarized below are some of the many contributions made by SRC research teams in 2002 to enable the continued advancement of semiconductor technology.

The Road to Ultimate CMOS Devices

Bulk CMOS Devices

Scaling of the MOSFET to its ultimate limit requires the introduction of materials that represent a significant departure from silicon and silicon oxides that have served so well to date. The SRC/ISMT Front End Processes Research Center has identified promising candidate high-K gate dielectric materials, explored their properties, and conducted process-related studies of the oxide interfacial layer that must be minimized to most aggressively scale the dielectric Equivalent Oxide Thickness (EOT). **Figure 1** shows an x-ray diffraction analysis of a chemical vapor deposited hafnium oxy-nitride gate dielectric film that can sustain up to 950°C annealing without crystallization and that exhibits thermal stability superior to hafnium-oxide film.

FIGURE 1: Analysis of CVD HfO_xN_y



Modeling and simulation studies of the transistor high-K gate stack have identified correlations between the d-state energies of the transition metal atoms and the electronic structure of transition metal oxide alloys. This has led to a fundamental understanding of the performance of transition metal alloys as (a) high-K gate dielectrics, and (b) dual metal gate electrodes in advanced CMOS devices. The research is also providing a systematic methodology for atomic scale materials engineering of transition metal oxides that supports the selection of potential successful candidate materials.

Research has shown that by applying stacked layers of Ni/Pt to form a Germanosilicide, contact resistance can be effectively reduced and good thermal stability can be achieved.

Advanced metal gate materials that have also been studied include (a) simple metals and metal alloys, (b) compound metals, (TaNx, TaSiNx, Ta-Ru alloy), and (c) metal silicides. Gate electric research has focused on a wide variety of issues including effective work functions, thermal and chemical stability at metal/dielectric interfaces, process compatibility, threshold voltage control, interface and bulk film characterization, and subsequent device performance and reliability. Recent results have shown that a Ta-Ru alloy is a very promising candidate for both N-MOS and P-MOS metal gates because its work function can be readily adjusted and because it supports process simplification.

Modeling and simulation of the role of dopants on the ON state current of a device and on OFF state device leakage has been instrumental in (a) elucidating the role of dopant/interstitial clusters, {311} crystal lattice orientation, and interaction loops as regulators of interstitial concentration and hence of diffusivity enhancement, and (b) in elucidating the interactions among these clusters and defects.

Advanced CMOS Devices

At least five microelectronics companies, including four SRC members, are fabricating and evaluating variations of the FinFET transistor for possible introduction at the 45-nm node. The University of California at Berkeley Team has demonstrated a novel FinFET optical spacer process that provides the narrowest fin (less than 10nm) with tight parameter control by fabrication of operational p- and n-channel FETs on the same wafer.

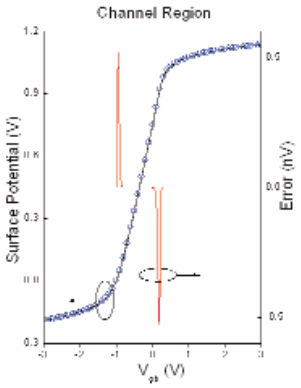
Another approach to enhancing MOSFET performance is to utilize strained silicon in the channel to obtain enhanced carrier mobility. An investigation of mechanisms for electron mobility enhancement at high vertical electric fields in

Enabling Silicon Nanoelectronics

strained Si n-MOSFETs has demonstrated that electron mobility at high fields ("surface roughness regime") is significantly enhanced by strain. This group also found that at high inversion charge densities, the Coulomb scattering related to the high doping density in the channel (necessary to be above 10^{18} /cm^3 for bulk devices at sub-45-nm nodes) is screened by the conduction electrons. The observed mobility enhancing result is very significant because it demonstrates that strain-induced performance enhancement can be obtained for devices with channel doping densities as high as 6 x 10^{18} /cm^3.

Parsimonious and accurate circuit-level models for devices are known as Compact Models, and the SRC research has a tradition of developing widely adopted MOSFET Compact Models. A "Surface Potential Approach" has been developed for Compact Models that is an important new contribution that both simplifies and accelerates the device simulations. A clever new analytical equation relating surface potential of the gate oxide/channel interface to the channel sheet charge is used to provide an accurate and time-efficient model for nano-scale MOSFETs used in circuit simulators. Figure 2 illustrates the high degree of accuracy of this new analytical solution for surface potential benchmarked against numerical solution. An in-depth evaluation of this model by a member company has verified the accuracy, parameter extraction efficiency, and simulation speed-up possible using this model.

FIGURE 2: Comparison between analytical surface potential model and numerical solutions



Enabling Wireless Technologies

SRC wireless research programs spans advanced devices, RF circuit design, system architectures, design tools, and test strategies. Because of the strategic importance of this high-growth segment to SRC member companies, SRC established in 2002 a cross-disciplinary approach to management of research in all mixed signal technologies, including RF and wireless. This program brings together many ongoing research efforts as a focused program and will result in coming years in many new projects. In one current program, a platform-based radio design approach is being developed, allowing the rapid design of multi-protocol wireless receivers for flexible, adaptable digital cell phones. Another program is developing advanced dynamic data shaping algorithms, aimed at multi-rate processing of video data over bandwidth-limited noisy channels, for use in advanced personal communication devices. SRC researchers are breaking new ground in wireless networking for a wide range of computing and personal devices with data rates up to 1 GHz by use of time-space diversity and sophisticated high-rate base-band signal processing. Design and validation of RF and wireless circuits poses enormous challenges; SRC funds several programs in advanced built-in test methodologies for RF circuits, as well as system-level design tools for studying fundamental algorithms for modulation, signal processing, error control, and data encoding.

Patterning at the Nanoscale

Current hardware research in patterning technology focuses on non-traditional patterning options for enabling reliable and low-cost advanced mask fabrication, ASIC design testing, and high volume sub-32 nm patterning applications. In 2002, this initiative explored the feasibility of multi axis e-beams and arrays of scanning probes, micro-mirrors, and micro inkjet write heads for niche application insertion at and beyond 2010. These efforts strongly couple with complementary initiatives in high rate data management and hardware-software trade-offs. Next Generation Lithography (NGL) related research explores the limits of Extreme Ultra-Violet (EUV) lithography and the potential for ameliorating Electron Projection Lithography (EPL) space charge effects. In 2002, exploratory projects in non-lithographic patterning, defect tolerant lithography, directed self-assembly, nanoengineered materials, and the deterministic positioning of dopant atoms were conducted. The scope of advanced mask research recently expanded to include exploring tools for repairing NGL masks and modeling step-and-flash and immersion mask technologies.

Enabling Silicon Nanoelectronics

SRC also maintained its research emphasis on developing novel modeling tools for optimizing advanced mask design.

Imaging materials research is exploring novel families of resists and optical materials and to develop a first principles understanding of correlations between the molecular structure and patterning performance. Recent results suggest that novel families of resist materials, such as photo labile dendrimers and block copolymers exhibit potential for 157 nm, NGL, and/or mask-less applications. Patterning related modeling research encompasses molecular models to aid resist and optics design, dynamic models of high aspect ratio pattern formation and self-assembled systems, and NGL and post-NGL pattern transfer simulations. Finally, metrology research addresses the need for novel non-destructive methods for measuring 3D nanostructures, interfaces, and material properties, including direct monitoring of acid diffusion during resist processing.

Increasing Factory Value-Add Through Resource Management

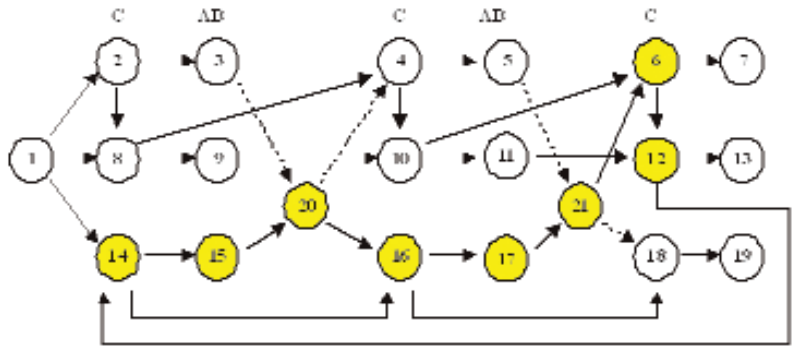
Factory Operations

A new methodology and software system for dynamic scheduling of preventive maintenance in highly automated, 300-mm factories was developed where it demonstrated in one member's fabrication facility and yielded a 5% improvement in tool availability. In addition, a new methodology for fabrication facility analysis and scheduling was developed that combines a new "Resource Driven" method of scheduling with the original "Job Driven" method. This combination provides a complete suite of methods and tools to facilitate timely, resource-efficient and accurate tools for scheduling and re-scheduling semiconductor fabrication facilities. Simulation tools resulting from this research will enable facilities to achieve balanced wafer throughput with decreased cycle time, provide a more flexible means for adjusting factory output and, thereby, reduce wafer and product cost. (See Figure 3.)

Environmentally Benign Manufacturing

The primary venue for Environmental Safety and Health (ESH) research in SRC is the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing at the University of Arizona in Tucson. Significant progress has been made this year in the four major areas of research: Back-End Processes, Front-End Processes, Factory Integration, and Patterning. Back-End Process work has included new chemistry for etching low-k dielectrics, novel, low-energy processes for depositing low-k dielectrics, and work on waste reduction in copper CMP. Front-End process development has included novel dry wafer cleaning processes, novel surface passivation and selective deposition, and work on etching high-k dielectrics. In Factory Integration, innovative water purification/recycling development and simulation continues, along with work on integrated ESH impact assessment processes and technology. Patterning continues to explore solvent-less lithography using direct patterning of dielectrics and supercritical CO2 based processes.

FIGURE 3: Wafer Fab Scheduling



Disjunctive graph showing a backward cycle caused by a solution to a specific flow that has been uncovered and can be resolved by the model

Enabling Silicon Nanoelectronics

Toward Interconnect and Assembly for the Terahertz Regime

A new Center for Advanced Interconnect Science and Technology was formed in 2002 to develop innovative approaches to ameliorate the increasing impact of interconnects on integrated circuit performance. In the new program, the copper metallization emphasis is on size and structure effects that will limit the usefulness of shrinking geometries of metal lines. The new program is emphasizing the critical need for ultra-thin barriers and ultra-low k dielectric that is emphatically evidenced by scaleback of these parameters in the ITRS Interconnect roadmap. Also included in the Center are new reach-out programs on radical solutions in optical interconnects and a new initiative in terahertz interconnects. As an example of the radical approaches being investigated, **Figure 4** shows a unique approach to manufacturing assembly techniques to provide mixed technology capability to insert optical emitters for on-chip optical interconnect systems.

FIGURE 4: Magnetic assembly of VCSEL Nanopills for Optical Emitters in Photonic Interconnects

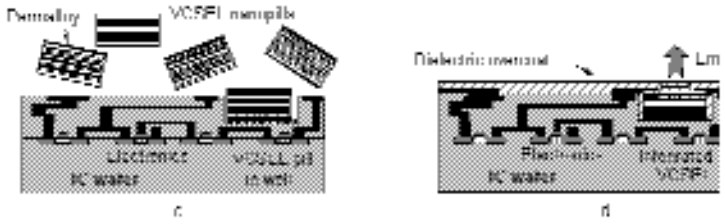
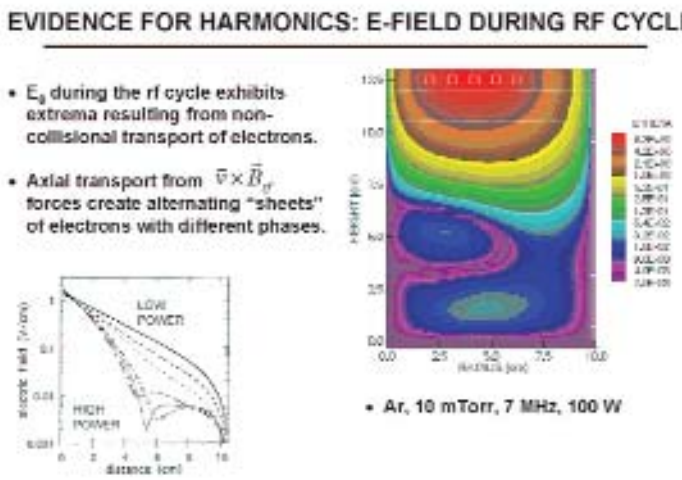


FIGURE 5: Plasma Process Models



In 2002, plasma processing programs have focused on the bridge between reactor scale modeling and feature scale modeling. Exciting results have included new methodologies to investigate and visualize harmonic content of electron energy distributions and excitation rates in plasmas commonly used in manufacturing operations. This capability offers the valuable possibility for real-time control of plasma systems based on optical emission. A snapshot in time of a dynamic visualization of plasma E fields during plasma RF excitation is shown in **Figure 5.** This dynamic visualization capability offers major opportunities to better comprehend the inner workings of plasma systems.

A constitutive model for eutectic and high-lead (C4) solders, based on a new percolation theory, has been developed to examine damage in high lead solders. This model includes the effect of damage developed during fatigue cycling and can be incorporated into an ANSYS finite-element-analytical model of solder joints. The model has been transferred to a member company via a student internship and to two other member companies. Algorithms for simulating I/O noise in multilayer packages for coupled transmission lines in the presence of bouncing voltage planes and decoupling capacitors are now available. This work has provided a key enabling capability for the design of future ASIC products. Better understanding of heat transfer processes has resulted in new predictive performance evaluation models for two phase heat spreaders, along with design parameters.

SRC's research program in Packaging and Interconnect addresses the difficult challenges of environmentally benign solders (i.e., Pb, Sb, and Bi free packaging materials), the impact of Cu/low-k materials on packaging, thermal dissipation, and improved underfills for flip-chip on organic substrates. In the longer term beyond 2007, SRC's program is addressing the difficult challenges of "High frequency die" and "Small, high pad count" through programs in accurate and efficient, full wave

electromagnetic field modeling and in novel approaches to global interconnect based on microwave free space and guided wave communications techniques.

Constraint-Driven Design Methodologies for Circuits and Systems

Design Space Exploration refers to the process of specifying a system architecture that meets a large set of functional requirements. The design space must be explored rapidly and accurately and evaluation of selected technology options must be supported. In 2002, research on a new abstraction algebra has resulted in a prototype system, which uses process algebra models and compiler optimization techniques to optimize system designs, culminating in direct synthesis of the design into the VHDL language. In another research program, nondeterministic finite automata models are used in transaction-level specification of systems, that can be synthesized into cycle-accurate register level representations for synthesis.

Power and energy considerations are of critical importance in all design activities, from specification through circuit design and physical implementation. In 2002, important results at the circuit design level include an 8 bit, 20 Ms/sec analog to digital converter which operates on a 1.8 volt supply and consumes only 50 milliwatts. A family of novel digital logic topologies has been developed which have been shown to reduce power (relative to conventional static CMOS structures) by 30% to 60% in certain applications; these families range from multi-threshold styles, to subthreshhold operation, to new domino logic architectures, and transistor-ordering schemes.

SRC sponsors extensive research into the effects of crosstalk and coupling, noise tolerance and avoidance, soft errors, logic upsets, and variability. In 2002, new software was released which estimates the substrate current spectrum for digital logic blocks; these estimates are used in library characterization to calculate bounds on noise and performance over fabrication and environmental parameters. Another recently completed program has produced high performance timing analysis algorithms which account for device variability, based on actual process statistics.

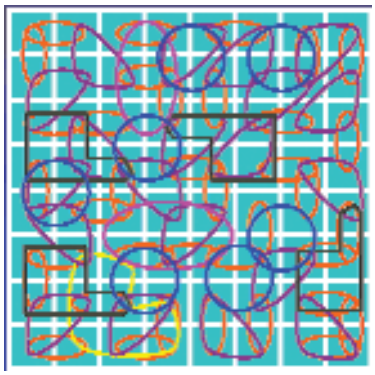
Recent results on interconnect issues in design include current mode signaling techniques, which exhibit significantly reduced susceptibility to signal cross-coupling and waveform degradation, compared to conventional voltage mode schemes with repeaters. In another project, differential signaling is used for chip-to-chip connections to reduce coupling and power consumption dramatically, requiring only one or two additional wires rather than doubling the number of wires per bit.

Research focused on the use of advanced devices in design currently addresses diverse issues such as application of silicon-germanium devices, silicon on insulator technologies, MEMS devices, and quantum dot devices in novel circuit applications. A revolutionary architecture for quantum cellular automata memory structures is under study, promising storage densities in the range of terabytes per square centimeter. Other programs study side effects of advanced technologies, such as the effect of gate tunneling current on digital logic structures. In one program, a wide variety of logic structures is being studied via simulation to determine the sensitivity of performance parameters and power consumption to gate leakage currents. Another critical side effect of advanced system on chip technologies is the electrostatic discharge susceptibility (ESD) of integrated radio frequency components. Novel ESD structures suitable for antenna terminals of 10 GHz RF receivers were developed this year, employing parts of the protection structure as passive components in the RF circuitry.

Design Tools for the Deep Submicron Regime

In place and route, SRC investigators have devised a method for generating synthetic examples with prescribed characteristics having optimal wire length; for the first time, place and route algorithms can be measured against how close they come to optimality, as well as against each other.

FIGURE 6: Placement Examples with Known Optimal wire length provide a standard for evaluating placement of algorithims.



Enabling Silicon Nanoelectronics

Partitioning algorithms two orders of magnitude faster than previous techniques can quickly partition large placed designs so that selected design metrics (area, power dissipation, number of cells, number of timing violations) are balanced across partitions. As the effects of scaling become more important for tools, researchers have developed an efficient integrated RCL interconnect extraction, simulation, and optimization flow which reduces complexity without losing accuracy and stability; this in turn facilitates aggressive optimizations based on realistic circuit models and accurate simulation methods. An efficient substrate resistance matrix extraction tool, integrated with a 3D layout extractor, can update a net list to capture the effects of substrate coupling. With the need for early estimation of design characteristics becoming more essential, SRC investigators have developed a framework to estimate the best achievable speed for a given design and its corresponding area cost at an early stage, obtaining good estimates of achievable performance without performing detailed design. And to address mixed-signal designs, a scalable substrate noise coupling macro-model has been incorporated into a commercial framework to perform substrate noise coupling analysis during schematic design and after post-layout extraction, assisting with overall floor planning and placement, and shielding of noise sensitive blocks.

Estimates persist that more than half the resources spent in getting designs to market are invested in verification. SRC members rely on SRC-sponsored work on formal verification tools for detecting errors and verifying industrial designs. A hybrid constraint solving framework produced by SRC researchers handles various levels of circuit abstraction automatically, targets functional test generation as well as formal verification, and incorporates word-level techniques and linear integer arithmetic techniques into an efficient solver. Addressing the state explosion problem which is exacerbated by both larger and more complex designs, a new refinement quickly discards uninteresting parts of the state space and significantly outperforms previous techniques. Processor-specific verification advances include tools which are expressive enough to model and verify diverse systems such as out-of-order processor cores, pipelined processors, complex load-store units from industrial microprocessors, and a cache coherence protocol. A technique for automatically abstracting large scale sequential hardware designs has been used to effectively generate counterexamples to correctness assertions, a key to detecting and correcting errors. All of these techniques are in use by SRC member companies.

Test and design for testability also continue to be challenges exacerbated by the move to larger, more heterogeneous designs where crosstalk and signal integrity effects play an increasing role in producing defects. Researchers have developed an efficient approach to testing on-chip ADCs and DACs which reuses existing digital processing units to generate input stimuli. A comprehensive analysis framework for analyzing and generating tests for switch failures in dynamic logic due to multiple sources of noise including coupling, charge-sharing and leakage has also been developed. And several efforts are addressing test generation and fault simulation for defect aggravated crosstalk. SRC members have used test time reduction techniques to significantly reduce tester time on a number of parts, resulting in lower test costs. Members have also used university-developed ATPG patterns on industrial parts, finding them to have superior defect detection capabilities when compared to standard commercial ATPG patterns. With an increase in research in analog test, investigators have provided promising jitter measurements for PLLs and VCOs. All of this work provides capabilities to member companies that are not available commercially.

Exploring Future Technologies

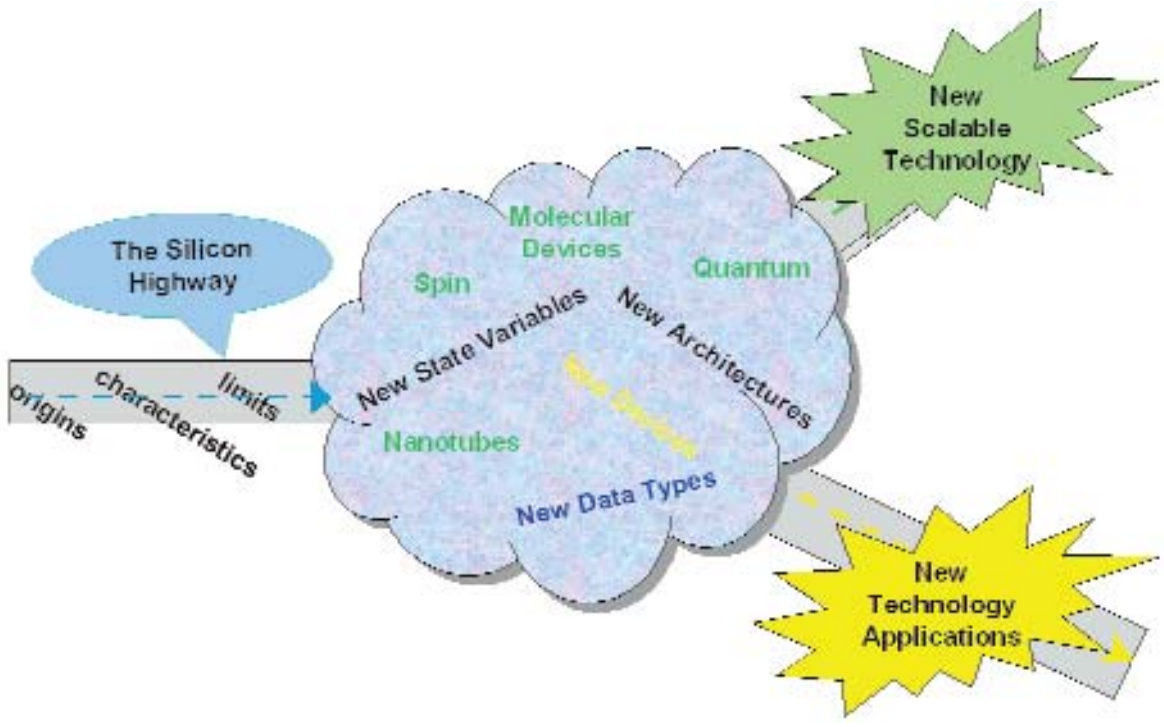
As CMOS approaches several fundamental scaling limits and the electronics create a power dissipation nightmare, SRC research is creating options to enable a gradual paradigm shift based on new approaches to information processing. Research approaches range from new FET-like structures that will preserve design methodologies and systems architectures to completely new approaches to representing the logic state and information processing. For example, novel FET concepts, such as MOTT Transistors, are being explored to sustain FET device architecture for high density, high performance and low power scaling. Conversely, a new phase-based logic technology amenable for implementation by cellular nonlinear networks is under investigation. This approach may permit low-energy, capacitive coupling between cells and thereby ultra-low-power logic. Another approach explores highly dense memory structures (floating back-gate and multi-bit storage quantum-dot memory) as elements integrable with CMOS to perform memory-based

Enabling Silicon Nanoelectronics

logic. To make use of these emerging devices and logic architectures, new systems architectural approaches are being explored as alternatives to von Neumann computing. Examples include cellular nonlinear networks, Bio-Inspired Computing and Quantum Computing. An integrated approach is being pursued to novel information processing schemes leading to building a portfolio of basic concepts including implementations of self-assembly, molecular electronics, magnetic semiconductors and solid-state qubits for quantum computing.

SRC has also begun to explore applications-driven emerging technologies. Research is underway to provide understanding of the materials and device characteristics of organic transistors on threads for computational fabric, silicon nano particle devices and novel models for E-textile management. These technologies could have an impact on applications requiring large area and flex electronics. For high performance computing and emerging technologies, we are also exploring smart embedded software concepts such as context-aware computing. The objective of this research effort is to apply knowledge and models from the cognitive and social sciences to create context-aware architectures that when coupled with sensors, MEMs and embedded computational devices/software (e.g., speech and image recognition) will provide enhanced information-human interface. **Figure 7** captures the sense of impending changes in the silicon highway.

FIGURE 7: Changing Vectors of the Semiconductor Industry



Award Recipients

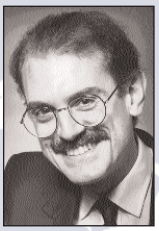
Technical Excellence Award

DATTA

LUNDSTROM

Professors Supriyo Datta and **Mark Lundstrom** of Purdue University are the recipients of the Technical Excellence Award for their work in the area "Device Physics and Simulation of Nanoscale MOSFETs." Funding for Dr. Lundstrom's work titled "Physics & Modeling of Heterostructure Semiconductor Devices" began in 1983, Dr. Datta joined the research team three years later in 1986. During this 20th anniversary year, we are honored to recognize these professors who have made multiple contributions to the semiconductor industry during the past 20 years.

Aristotle Award



SANGIOVANNI-VINCENTELLI

The 2002 Aristotle Award was presented to **Professor Alberto Sangiovanni-Vincentelli**, University of California/Berkeley. The Aristotle Award recognizes SRC-supported faculty whose deep commitment to the educational experience of SRC students has had a profound and continuing impact for SRC members over a long period of time.

This award is given to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research, who are ground-breakers and leaders in their fields, and who are regarded as model collaborators with their colleagues in the SRC member community.

Mahboob Khan Award

The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as Industrial Liaisons. Recipients represent “ideal mentors” whose commitment more than enhances the SRC research program. The 2002 award recipients were:

Doug Garrity of Motorola has worked with Dr. David Allstot's research team at the University of Washington in the area of Analog to Digital Converters. According to Dr. Allstot, "Doug's experience enables him to identify marginal ideas in favor of more promising approaches, thus his mentoring allowed SRC Fellow Douglas Beck to focus on an important research contribution rather than wasting valuable time and resources on incremental ideas."

Ram Kumar Krishnamurthy of Intel, an expert in "High Performance Digital Design," has worked with Dr. Vojin Oklobzija at the University of California/Davis. He has been "instrumental in guiding research toward the needs of the industry, by providing opportunities for graduate students and professors to spend time at Intel."

James Libous of IBM has been an advocate within the SRC community for work in Advanced Packaging being done by Dr. Madhavan Swaminathan's team at Georgia Tech. Dr. Libous was instrumental in arranging summer industrial experiences for several students, exposing them to the industrial environment then remaining in contact with the students upon return to the academic community.

Jeffrey Parkhurst of Intel, an industry expert in the field of Circuit Design, has been a long-time advocate of the Industrial Liaison Program within the industry, taking a proactive role in recruiting new liaisons within Intel. His work with the Universities of California at Berkeley and Davis has provided a beneficial link between professors and students at both of these universities and Intel. Jeff has provided leadership in the identification of top Ph.D. research projects that address the needs of the industrial community.

Terry Sparks of Motorola has worked on the Alternative Chemistries for Dielectric Etch project at MIT for the last five years. Three SRC students have completed five summer internships at Motorola where they interacted with Terry on a daily basis. An example of his impact on one student can be found in SRC Fellow Simon Karecki's thesis preface, in which Dr. Karecki thanked Terry, "who taught me all I know about plasma etch."

Charles Szmanda of the Shipley Company has worked with Dr. Paul Nealey's research group in the development of Photoresist Materials and Processes at the University of Wisconsin for the past five years. His understanding of the role of components of chemically amplified resist systems in resist dissolution and pattern development resulted in SRC Fellow Adam Pawloski's thesis research.

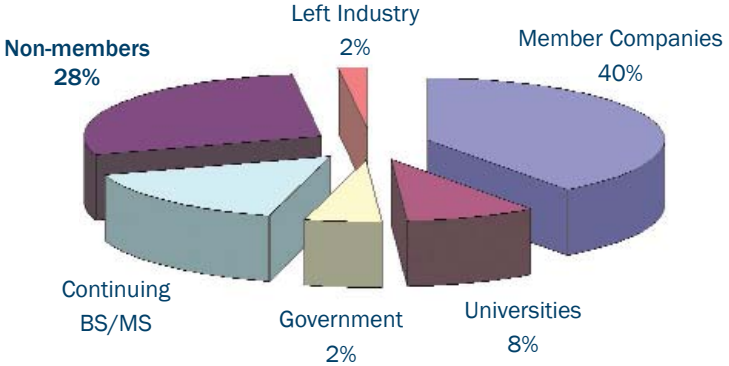
Student Programs

Winners of Outstanding Research Presentation Awards at the 2002 Graduate Fellowship Program Annual Conference were (left to right) AMD/SRC Fellow Ritwick Chatterjee, Massachusettes Institute of Technology; International Fellow Luca Daniel, University of California at Berkeley; and IBM/SRC Fellow Eric Pop, Stanford University. Research presentations were judged in three categories: Design, Material and Process Sciences, and Nanostructure and Integration Sciences.

Over 1,100 students participated in SRC-funded research in 2002. Of the graduates, about 70% went to work for SRC member organizations or are undergraduate or master's students continuing to higher degrees, further strengthening the links within the SRC community. Other 2002 accomplishments included:

- Two new core Fellowships, four new Company-Named Fellowships and one new International Fellowship were awarded through the Graduate Fellowship Program to bring the number of fellowships at the beginning of the 2002 fall term to 51.
- Eight new Master's Scholarships were awarded, including three new Company-Named for a total of 15 at the beginning of the 2002 Fall term. Two of the new scholarships were awarded to graduates of the Undergraduate Research Assistants Program.
- Well over 100 Fellows, Scholars, industry representatives, and SRC staff attended the 2002 Graduate Fellowship Program Annual Conference in September. The keynote address was delivered by Tom Engibous, Texas Instruments Chairman and CEO. Ninty-five percent of attendees rated the conference greater than four on a five-point scale.
- Over 500 resumes were published on the SRC Web site. A new process was developed by SRC to allow students to update their database information and submit their resumes via the SRC Web site, thereby significantly reducing barriers for students.
- The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars. A copy may be obtained by contacting SRC Student Relations at the SRC corporate address.
- The first Simon Karecki Award was made from the Simon Karecki Endowment to Casey Finstad at the University of Arizona. This award recognizes outstanding student performance through the SRC/NSF Center for Environmentally Benign Semiconductor Manufacturing, centered at the University of Arizona.

2002 SRC STUDENT HIRING STATISTICS



Nearly 70% of students completing degrees under SRC-funded research in 2002 joined the SRC community or are continuing to higher degrees.

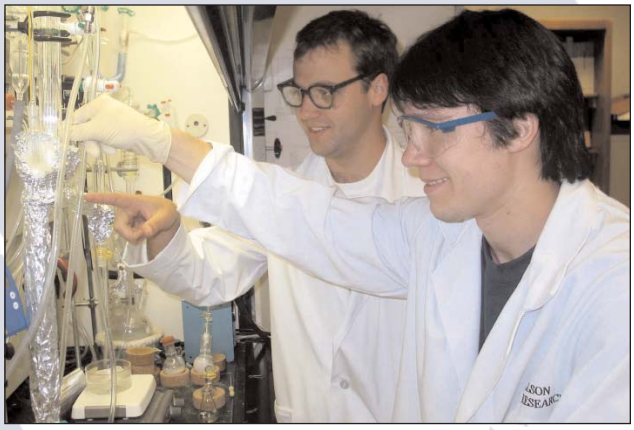
SRC Education Alliance

The SRC Education Alliance (SRCEA) is a wholly-owned subsidiary of the Semiconductor Research Corporation. The SRCEA is a non-profit (501(c)3) charitable foundation with strong ties to the SRC research and student programs. The Undergraduate Engineering Programs and the Simon Karecki Endowment are managed under the SRCEA.

The Undergraduate Engineering Programs (UEP) were successfully launched in July 2000 with the second year completing in June 2002. The UEP includes the Undergraduate Research Assistants (URA) and MOSIS. The SIA Board member companies committed to funding for the UEP for three years through June 2003.

Undergraduate Engineering Programs Year Two: Assessment and Recommendations was published in October 2002 and is on the SRCEA Web site at srcea.src.org/programs/default.asp.

Eighty-two students participated in the URA Program in Year Two. Retention in the program remained high with 89% either continuing from the academic year to the summer term or graduating. The program has graduated a total of 34 students; 56% have either joined sponsoring companies or continued to graduate study. The diversity of the student population remained high, with about one-third being female and about 10% in under-represented minority categories. GPA also remained relatively high at 3.63 for a representative sample.



URA student Jose Rangle (foreground) and SRC Fellow Matt Pinnow work together in Professor Grant Willson's research lab at the University of Texas/Austin.

The number of students participating in MOSIS in Year Two was well over 5,000, surpassing the 1998 level (1998 was the last year of government funding for MOSIS and the benchmark for current metrics). MOSIS also showed a continued rise in the number of classes and class projects. Responding to a request from the UEP Advisory Board, MOSIS has provided information about class projects and university contacts via the SRCEA Web site. MOSIS continues its efforts to include smaller schools in the MOSIS educational service, to build more extensive libraries for use by students and to explore options to make fabrication by MOSIS more attractive for SRC-funded graduate students.

With SIA funding for the Undergraduate Engineering Programs ending in June 2003, SRC and SRCEA have proposed that oversight of the programs should stay in the SRCEA with funding from other sources. To that end, SRC and SRCEA continue to explore other funding options for these programs.

Undergraduate Engineering Program Sponsoring Companies

Advanced Micro Devices, Inc.	IBM Corp.	Motorola, Inc.,
Agere Systems	Intel Corp.	National Semiconductor Corp.
Analog Devices, Inc.	Intersil Corp.	Texas Instruments, Inc.
Conexant Systems, Inc.	LSI Logic Corp.	Xilinx, Inc.
Cypress Semiconductor Corp.	MICRON Technology, Inc.	

Focus Center Research Program

MARCO

Semiconductor Industry Association (SIA):

- Advanced Micro Devices, Inc.
- Agere Systems
- Agilent Technologies
- Analog Devices, Inc.
- Conexant Systems, Inc
- Cypress Semiconductor
- IBM Corporation
- Intel Corporation
- LSI Logic Corporation
- MICRON Technology, Inc.
- Motorola, Incorporated
- National Semiconductor
- Texas Instruments
- Xilinx, Inc.

SIA Semiconductor Industry Association

Semiconductor Industry Suppliers:

- Air Products & Chemicals, Inc.
- Applied Materials, Inc.
- KLA-Tencor Corporation
- Novellus Systems, Inc.
- SCP Global Technologies
- SpeedFam-IPEC
- Teradyne, Inc.

Department of Defense:

- Deputy Undersecretary of Defense for Laboratories and Basic Sciences (DUSD/LABS)
- Defense Advanced Research Projects Agency (DARPA)

DARPA

DESIGN AND TEST

The University of California at Berkeley is the lead university for the Design and Test Focus Center (Gigascale Silicon Research Center--GSRC). **Professor Jan Rabaey** is the center's director. The Design and Test Center's research agenda addresses concepts such as component/communication-based design, constructive fabrics, fully programmable systems, calibration of achievable design, validation, power and energy. With increased complexity of integrated circuits and relentless competitive pressures of time-to-market, the GSRC agenda is focused on the discovery of software design tools, circuit families, libraries and the approaches used to integrate a design process.

UC/BERKELEY

- Carnegie Mellon University
- Mass. Institute of Technology
- Pennsylvania State
- Princeton University
- Purdue University
- Stanford University
- UCLA
- UC/San Diego
- UC/Santa Barbara
- UC/Santa Cruz
- University of Michigan
- Univ. of Texas / Austin
- University of Wisconsin

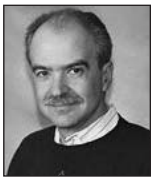
INTERCONNECT

The leadership for the Interconnect Focus Center (IFC) is based at the Georgia Institute of Technology. Professor James Meindl is the focus center director. The Center's research teams examine six major tasks: System architecture, physical design tools, novel communications mechanisms, chip to module interconnects, materials/processing/predictive modeling and metrology. With aggressive scaling, interconnect becomes the dominant source of delay and energy consumption. The IFC looks to discover and invent new interconnect solutions that will meet or exceed ITRS projections.

GEORGIA TECH

- Mass. Institute of Technology
- Rennselaer Polytechnic Institute
- Stanford University
- Univ. of Albany
- UCLA

MATERIALS, STRUCTURES & DEVICES



The Massachusetts Institute of Technology was designated as the lead university for the Materials, Structures and Devices Focus Center (MSD). **Professor Dimitri Antoniadis** is the Focus Center director. This Center will research sub-10-nanometer silicon-based FETS, silicon-based quantum-effect devices, molecular and organic semiconductor electronics, nanotube electronics and modeling & simulation. Maintaining the historical CMOS performance trend requires new materials and structures by 2008-2010, or earlier, if current bulk-Si data do not improve significantly. The MSD center explores the most promising path for device evolution in the next two to three decades.

MIT

- Cornell University
- Princeton University
- Purdue University
- Stanford University
- University of Albany
- UCLA
- UC / Berkeley
- Univ. of Texas / Austin
- University of Virginia

CIRCUITS, SYSTEMS & SOFTWARE

The Focus Center team for Circuits, Systems and Software (C2S2) is led by the Carnegie Mellon University. **Professor Rob Rutenbar** is the director. The center's research will focus on the analysis and synthesis of analog and analog/mixed signal circuits, explore novel system level technologies and search for software solutions and work-arounds for the deep submicron CMOS process limitations. The scaling of tomorrow's semiconductors toward ulitmate physical limits conflicts with the need for rapid transistors to fruition against the challenges of reduced design time.

CMU

- Columbia University
- Cornell University
- Mass. Institute of Technology
- Princeton University
- Stanford University
- UC /Berkeley
- University of Illinois at Urbana-Champaign
- University of Michigan
- University of Washington

Intellectual Property

Intellectual property (IP) assets covering SRC sponsored university research programs are provided by SRC to its members to protect and enhance the value of SRC membership. IP assets serve to support the SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs to SRC member companies. The SRC's significant portfolio of intellectual assets minimizes the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship. IP assets are interwoven with the SRC research catalog and complement the value chain as an important benefit of SRC membership.

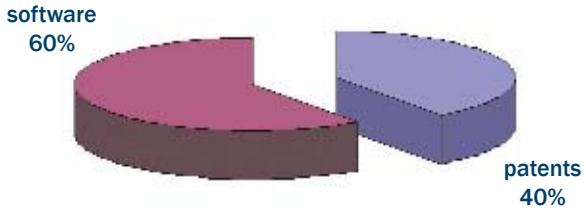
In return for sponsorship, SRC receives non-exclusive, worldwide, royalty-free licenses in IP from university research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results may be provided, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to provide a level playing field for members by ensuring that those who utilize SRC-sponsored technologies do so only within the scope of a valid license.

SRC is investigating ways in which IP assets can provide new and additional sources of value to the SRC member community. SRC and North Carolina State University have announced an innovative joint licensing and commercialization partnership focused on commercializing selected inventions arising from SRC-sponsored university research programs at NCSU. The new partnership presents an optional alternative licensing relationship between SRC and NCSU for mutually selected inventions developed under SRC sponsorship. Under the partnership, select SRC and university intellectual property rights are combined and licensed to SRC. The formerly separate IP rights have greater value once combined in an escrow managed by SRC.

The formerly separate IP rights have greater value once combined and allow exclusivity in licensing. As a result, SRC can provide enhanced commercialization prospects and greater licensing value as compared with the traditional SRC-university licensing model. The university, SRC, and SRC member companies agree on terms to sublicense one or more companies able to commercialize the invention and share the royalties collected. SRC, its member companies and NCSU are working together to implement this new experimental licensing model.

SRC has also implemented an IP Advisory Board (IPAB), comprising several SRC member company representatives, to work with SRC on the traditional and new experimental IP licensing matters. The IPAB will be an integral part of the decision-making process pertaining to these exciting opportunities. For further

IP PORTFOLIO COMPOSITION



details regarding the IPAB, please contact Frank Pita, Director of Corporate Legal Affairs and IP Counsel.

During 2002, ten SRC-sponsored U.S. and foreign patents issued, bringing the total portfolio of SRC licensed patents to 195. SRC's significant patent portfolio supports both U.S. and international member company operations in numerous countries around the world. SRC's web site permits members to submit real-time queries into SRC's IP database to obtain status on pending and issued patents as well as information on SRC-sponsored software.

The SRC IP portfolio also provides over 288 software programs, software models, and technical databases to member companies. Software and database licenses from SRC-sponsored research programs represent a growing and complementary part of the SRC IP portfolio. Members are directed to the online software directory at http://www.src.org for further details. SRC members receive non-exclusive, worldwide, royalty-free intellectual property licenses in applicable software programs and technical databases.

SRC U.S. and Foreign Patents ISSUED IN 2002

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Step and Flash Imprint Lithography	Grant Willson Matthew Colburn	Mar. 11, 1999 Jan. 1, 2002	6,334,960 (U.S.)	Univ. of Texas at Austin
Methods of Forming Features of Integrated Circuits Using Modified Buried Layers and Integrated Circuits Having Features so Formed	Andrew Ritenour	May 24, 2000 Feb. 12, 2002	6,346,446 (U.S.)	Massachusetts Institute of Technology
Oxidation of Silicon on Germanium	Lionel Kimerling Hsin-Chiao Luan	June 25, 1999 March 5, 2002	6,352,942 (U.S.)	Massachusetts Institute of Technology
A Capacitorless Dram Device on Silicon-On-Insulator Substrate	Chenming Hu Hsing-Jen Wann	Dec. 1, 1994 Mar. 21, 2002	69429106T2 (Germany)	Univ. of California at Berkeley
Methods and Compositions for Imaging Acids in Chemically Amplified Photoresists Using pH-Dependent Fluorophores	Scott Bukofsky Paul Dentinger Robert Grober James W. Taylor	May 26, 1999 April 23, 2002	6,376,149 (U.S.)	Yale University and Univ. of Wisconsin
Using Block Copolymers as Supercritical CO2 Developable Photoresists	Christopher Ober	Oct. 26, 1999 April 30, 2002	6,379,874 (U.S.)	Cornell University
Water-Processable Photoresist Compositions	Grant Willson Shintaro Yamada	Aug. 14, 2000 June 4, 2002	6,399,273 (U.S.)	Univ. of Texas at Austin
Wire Width Planning and Performance Optimization for VLSI Interconnects	Jason Cong David Z. Pan	Feb. 22, 2000 June 18, 2002	6,408,427 (U.S.)	Univ. of California at Los Angeles
Oxidation of Silicon on Germanium	Lionel Kimerling Hsin-Chiao Luan	Jun. 26, 2000 Aug. 15, 2002	154359 (Taiwan)	Massachusetts Institute of Technology
Multiple-Thickness Gate Oxide Formed by Oxygen Implantation	Chenming Hu Tsu-Jae King	Dec. 1, 1999 Aug. 16, 2002	154458 (Taiwan)	Univ. of California at Berkeley

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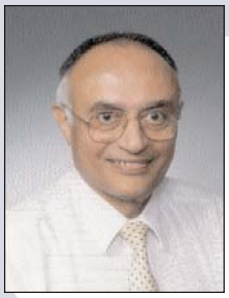

Dinesh Mehta
Vice President,
Business Operations
& Strategic Initiatives

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Yoshio Nishi	Texas Instruments	(through June 26, 2002)
Hans Stork	Texas Instruments	(as of June 26, 2002)
Richard Schinella	LSI Logic	
Walter Class	Axcelis	
Fu-Tai Liou	UMC	(through March 14, 2002)
Frank Wen	UMC	(as of March 14, 2002)
Craig Sander,	AMD	
Wilbert van den Hoek	Novellus	
John Warlaumont	IBM	
Sunlin Chou	Intel	
Don Harbert	Compaq	(through August 1, 2002)
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Mohan Yegnashankaran	National Semiconductor	
Dave Nichols	Eastman Kodak	
Larry Sumney	SRC	

Clark McFadden, Dewey Ballentine, Secretary and Counsel

* Executive Director, MARCO

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