SEMICONDUCTOR RESEARCH CORPORATION®

2003 ANNUAL REPORT

Message *from the* President

In 2003, with the guidance from its Board of Directors, SRC made significant moves in order to maintain the founders' vision of providing a strong university research infrastructure with high value output of technology and students to form the base for the future of the semiconductor industry.

In order to be able to provide greater benefits to our members, SRC laid the groundwork to become a taxable entity starting January 1, 2004. A new program management mode has been piloted to exploit the core SRC expertise that can help individual companies manage their university research programs more cost effectively. The new tax status will also permit SRC to revitalize the concept of Topical Consortia in response to the focused needs of specific sets of members in the rapidly changing environment. SRC is also piloting an exclusive IP license model which would provide greater competitive advantage to SRC members.

In 2003, the research programs again made impressive contributions to the technology base for the members to use in their critical decisions for the future. Because cost of design may be one of the greatest threats to the continuation of the ITRS roadmap, the related Science Areas have significantly increased effort in SRC programs, from high performance mixed signal design and test to radical computing architectures. Meanwhile, the device design, processing, lithography and packaging areas continue to advance the technologies necessary for scaling the dimension requirements of the ITRS. Demand forecasting software from the Factory Operations Research Center programs is already being implemented by an SRC member company. In keeping with the longer-term strategic thinking, SRC staff continues to work with the Board and the ETAB at summer strategy meetings to develop the broad themes for going forward during the next few years. The strength of the process and device research will be maintained utilizing leverage from various government research funds while increasing the work in IC and system design-related research.

Of course the impressive technological breakthroughs would be of little value if they were not quickly provided to the members. In 2003 an Internet-based system for delivering results of key research, Technology Transfer e-Workshops, was piloted and ramped-up as a result of overwhelming member requests. Neither the researcher nor the member engineers had the inconvenience or the expense of significant travel, and the lectures, with the audio, have been archived on the SRC Web site.

TECHCON 2003, held in Dallas, Texas, was marked by excitement and energy as 130 SRC students presented a broad spectrum of SRC-funded research in papers and posters. The Focus Center Research Program was also represented in an invited student session, as was the SiGe Design Challenge. Highlights were an address by Nobel Laureate Richard Smalley, Rice University, and the keynote address by Paul Horn, IBM.

The SRC Web sites continue to play an important role in SRC's value management and delivery model. Web site usage from member companies continues to increase significantly, leveraging the growing volume of research and programmatic content of the sites. Equally important has been the dramatic increase in usage by the SRC research community as SRC extended its Web functionality to better enable universities to submit timely research results online and students to update their resumes for member recruiting opportunities. 2003 also saw the release of a new MARCO/FCRP Web site fully integrated within the SRC family of sites to better enable MARCO members to gain rapid access to Focus Center research results.

In 2003 SRC continued its tradition of providing timely, stellar research results to assist its members' strategic plans, while also strategically positioning SRC to be of ever-increasing strategic value to our members as we move forward in the 21st century.

Larry Sumney
President and CEO

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Vision

The SRC operates globally to provide competitive advantage to its members as the world's premier university research management consortium delivering relevantly educated technical talent and early research results.

Mission

The SRC's mission is to manage a range of worldwide, consortial, academic-based research and education programs, each matching the needs of their sponsoring entities.

The SRC's core research program provides:

- Innovative, strategic, pre-competitive research guided by the ITRS, focusing on universities
- University graduates with high rate of placement in member companies
- A global forum for pre-competitive collaboration among all segments of the semiconductor industry, universities and governments
- Advocacy to various government and other funding agencies for support of University semiconductor research
- A comprehensive Value Proposition that focuses on maximizing member value

Company Profile

Pioneers in collaborative research

Over the past 21 years, the industry has invested more than $600 million through SRC, and well over 3,000 scientists and engineers have received advanced degrees from SRC supported programs.

SRC's core directed-research program has a continuously evolving portfolio of more than 350 projects that are currently targeted at the full spectrum of semiconductor technologies, including: circuit and system design; design tools; test and testability; materials and processes; packaging and interconnect; advanced patterning; mixed signal/analog technologies; metrology; environmental safety and health; and advanced device and modeling and simulation. We have described significant results from the research efforts in the year 2003.

MARCO, an SRC subsidiary, currently has five Focus Centers conducting complementary research projects that are described in the MARCO annual report.

SRC continued to enhance student programs in its core program to ensure development of the highest quality talent for our member companies. In addition, the SRC Education Alliance addresses the need for developing undergraduate talent relevant to the industry.

Because the semiconductor industry and its International Technology Roadmap for Semiconductors (ITRS) have become global, SRC now has members and university research programs in countries around the world. In order to enable an effective approach for delivering value to our member companies, research results and publication are posted on the secured web site for member access. In 2003, a record number of publications and deliverable results were placed on the site, along with information about patents and software to which the members have royalty-free access. Also in 2003, the site was used for real-time collaboration as well as threaded discussions.

Through the combined efforts of the Board of Directors, our various technical advisory boards and SRC staff, research strategy and operational plans are continually refined to produce value, satisfying the members as evidenced by the annual member satisfaction survey. The survey addresses all four dimensions of the Value Proposition—Creation, Delivery, Extraction, and Advocacy/Enhancement—that are made available via SRC's primary products: Research Results, Relevantly Educated Talent, Integrated University Research Capability, and Networking.

We have continued to hone the processes and tools associated with the delivery of SRC value to our member companies. Also, we have continued to refine the mechanisms and support that are provided to facilitate the extraction of maximum value in the most cost-effective manner for our member companies, as evidenced by the increased use of electronic meetings utilizing both the SRC web site and "net-meeting" software. Finally, we work with the representatives of our member companies on the Board of Directors and the various advisory boards to continuously revitalize our products, programs, processes and systems to enhance value for our members.

Year 2003 was another difficult year for the industry and for SRC. The marketplace has undergone significant changes that have, in turn, changed the complexion of the industry, research needs, and the research budgets. As a result, preparation for 2004 presented even greater challenges to maintain critical research programs and to maintain SRC's reputation as a preferred sponsor of university research. Several examples of the dynamic nature of our business and the value that the community of our consortium has brought forth in the year 2003

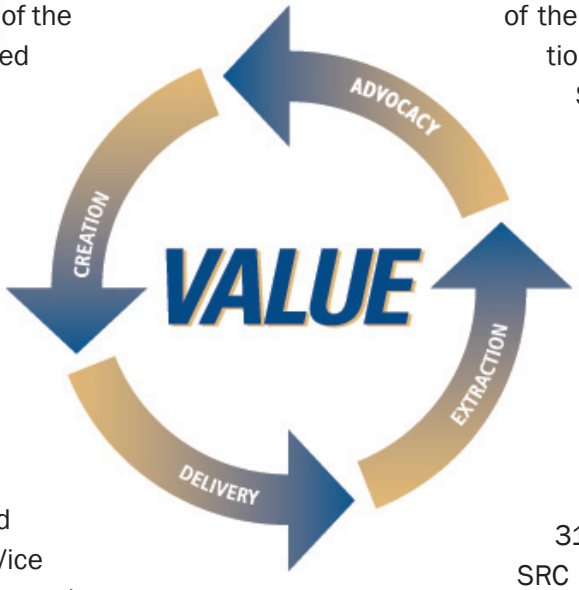
Company Profile

are presented in this report. This abbreviated report can only describe some of the key accomplishments, major initiatives, and important events of 2003 that demonstrate the value, strength, and agility of the consortium, for example:

• Our Executive Technical Advisory Board (ETAB) continued to provide high-level technical/strategic directions to shape the research portfolio. The ETAB also developed the architecture for a modified Science Area structure, which will be implemented in 2004.

• The SRC Board of Directors approved several Strategic Initiatives that impact SRC's business model and practices that would help SRC enhance its value to all segments of the industry.

•Professor Sachin Sapatnekar of the University of Minnesota received the Technical Excellence Awards for his work in "Analysis and Optimization of Signal and Supply Networks."



• SRC's sixth major technical conference, TECHCON, was held in Dallas with more than 130 students presenting papers. The keynote address was delivered by Paul Horn, IBM Senior Vice President and Director of Research. 60 SRC Fellows and Scholars participated, presenting 32 papers and 46 posters, and winning seven Best in Session Awards. The Graduate Fellows Program banquet keynote was delivered by Dr. Claudine Simson, Motorola Corporate Vice President.

• Fourteen SRC-sponsored U.S. and foreign patents were issued, bringing the total portfolio of SRC-licensed patents to 209, all of which can now be queried by members on the SRC Web site.

There were many other noteworthy 2003 accomplishments in other areas not described in this abbreviated report, such as:

• Member companies assigned Industrial Liaisons to work with researchers on a record percentage of tasks, a strong indicator of the ongoing efforts to derive value from the technology and to mentor the students toward a rewarding career in the industry.

• SRC continues with its e-meeting initiative to better enable remote-attendance at meetings by utilizing state-of-the-art teleconferencing and web-based solutions. Not only has this strategy provided a means to reduce travel costs but also to significantly enhance participation and collaboration.

• The year 2003 saw continued expansion of the SRC suite of Web sites. In addition to a significant redesign of the SRC Core Web site that encompassed the new science areas, SRC also greatly expanded the scope and content of the MARCO/FCRP Web site, incorporating database driven research content with full submission capability granted to each of the participating Focus Centers. Web site usage for 2003 demonstrate that over 3100 personnel logged into the SRC Core Web site nearly 30,000 times.

• At the 2003 Design Automation Conference, 43 of 55 technical sessions included SRC involvement and two of the four Best Paper awards were awarded to SRC-sponsored research. At the 2003 International Conference on Computer-Aided Design, 43 of 46 technical sessions included SRC involvement and one of two Best Paper awards went to an SRC industrial liaison. In addition, at the 2003 IEDM, 22 papers out of 229 acknowledged SRC or MARCO support.

SRC RESEARCH:
Mission Critical Research

For more than thirty years the semiconductor industry has provided its customers exponential gains in performance per unit cost. The industry has codified the strategy of sustaining exponential progress through the 2003 International Technology Roadmap for Semiconductors (ITRS) that gives detailed estimates of technical requirements over a fifteen-year horizon. Successful realization of the technologies that meet ITRS requirements will provide the basis for continued expansion of the benefits provided by integrated circuits to society.

A vibrant and productive research and development pipeline is essential if the challenges given by the ITRS are to be met. SRC supported university research is designed by its members to intersect the industry development cycle in a timely manner to sustain the ITRS technology cadence. In the following, selected SRC research results that are providing significant benefits to members are described. SRC gratefully acknowledges its productive research partnerships with NSF, DARPA, NIST, International SEMATECH, and the state of New York in 2003, and especially its university participants and its member companies.

The research areas in the following section are organized by the new science areas planned for 2004.

Device Sciences

Gate Stack Materials and Processes

CMOS technology evolution will most likely include new gate stack materials and processes. To address these needs, SRC research is focused in three key areas: 1) new high-k dielectrics and metal electrodes for the gate stack to reduce gate leakage, 2) fully depleted Silicon-On-Insulator (FD) (SOI) and multiple gate structures to mitigate short channel effects and 3) use of new source/drain contact materials and super saturation doping to lower source/drain contact resistance.

SRC research seeks alternative high-k gate dielectrics to achieve an equivalent-oxide-thickness (EOT) of 0.5 nm, new metal gate electrodes and new metrology techniques for the gate stack. One high-k gate dielectric material, HfSiON, has been shown to exhibit excellent thermal stability for high annealing temperatures while remaining amorphous for a relatively high N concentration with no formation of deleterious polycrystalline phases (figure 1). A new approach for achieving an EOT of 0.5 nm has been developed that includes high dielectric permittivity, and relatively high conduction and valence band offset energies to reduce leakage current between the gate and dielectric. This approach combines a transition metal with a rare earth metal in a ternary oxide to form new dielectric materials.

Thermal stability and work function values are key parameters for selection of metal electrode materials to ameliorate asymmetric threshold voltage shifts in n-channel and p-channel MOSFETs with metal gate electrodes. Since the work function values of metal gates may be impacted by the properties of underlying dielectric, new work function extraction methodologies that take into account electric charges in the high-k dielectric bulk and interfaces are required. The RuTa alloy is considered to have significant potential because changing its alloy composition can monotonically vary its work function to control the threshold voltage of MOSFETs. Research also has revealed the influence of B and As dopants on the work function of fully silicided NiSi gate electrodes.

A new method for measuring a variety of phonons, including soft optical phonons, in MOS structures was

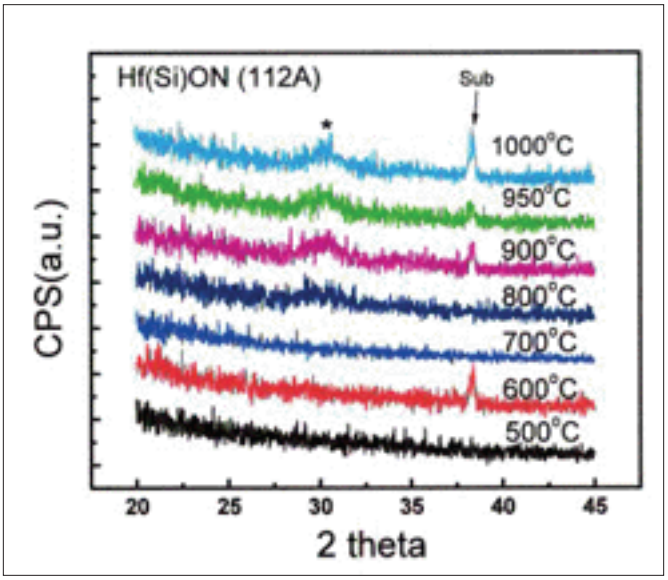


Figure 1: X-ray diffraction spectra of 11.2 nm HfSiON film.

reported in 2003. This technique may provide a new means for extracting more accurate values for channel mobility in high-k/metal gate MOSFET structures. New results have also demonstrated a better understanding of phase stability and segregation as a function of composition and temperature, accurate measurements of interface layer composition and film composition, and a better understanding of mobility issues.

New Device Technologies

Electron and hole mobilities and, as a consequence, MOSFET 'on' current can be substantially increased in strained silicon and silicon/germanium alloy layers used in MOSFET channels. In one study the strained epitaxial layer structure was designed to provide enhanced and nearly symmetric mobilities for n- and p-channel MOSFETs. The strain-enhanced mobility (mobility enhancement factor) in an n-channel MOSFET is quite substantial and relatively independent of the silicon channel thickness. For p-channel MOSFETs, the p-mobility enhancement factor can be adjusted to provide a better match of its on current with that of the n-channel MOSFET. The heterostructure stack enables large mobility enhancements for both n- and p-channel MOSFETs with ultra-thin channels over a broad range of vertical fields (figure 2). Investigators are also exploring the use of a strained layer, which is flip-chip bonded and transferred from its parent wafer to the oxide layer on a second wafer, without disturbing the strain.

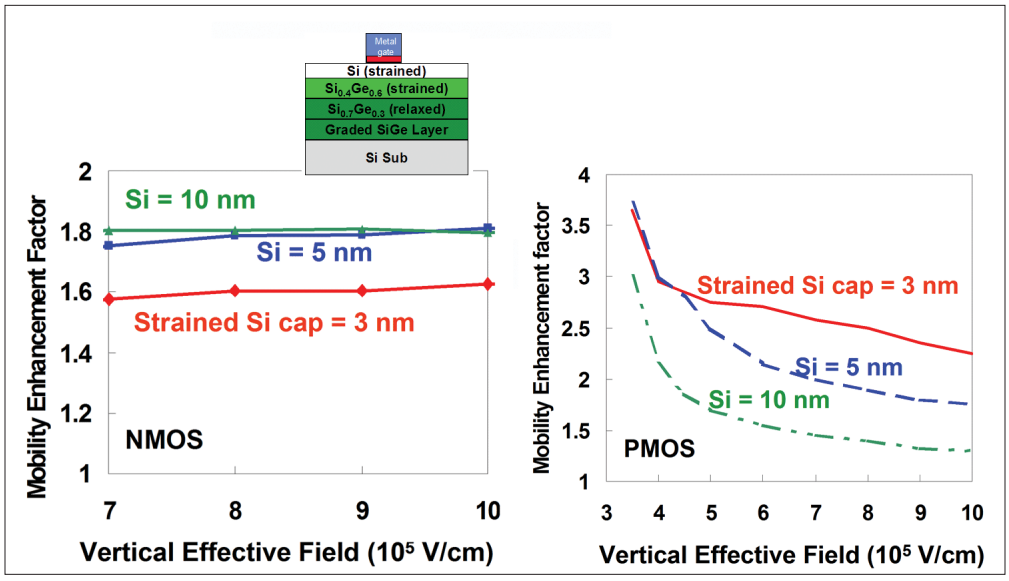


Figure 2: The heterostructure stack

Nanomanufacturing Sciences

Patterning

The SRC has five major research thrusts in patterning: 1) Systems and components, including Next Generation Lithography (NGL) limits, high volume, sub-32 node applications; 2) Masks, including repair, step-and-flash and immersion mask technologies; 3) Imaging Materials, including resolution, processing limits, processing limits for chemically amplified resists, high information content materials, e.g., dendrimers and other self-organizing polymers, understanding of correlations between molecular structure and patterning performance; 4) Modeling, including molecular models to aid resist and optics design, dynamic models for high-aspect ratio pattern formation, NGL and post-NGL pattern transfer simulations; 5) Metrology, including non-destructive measurement of 3D nanostructures, interfaces, material properties, and direct monitoring of acid diffusion during resist processing.

The SRC patterning research had considerable mission critical impact in 2003. The SRC/DARPA Advanced Lithography Research Network research in Maskless Patterning has provided a knowledge base for the issuance of a DARPA Broad Area Announcement, directed to sub-50 nm maskless lithography, with awards to be made in early 2004. The objective of the SRC/DARPA 2003 Low Volume Patterning Workshop that preceded this announcement was to assess the feasibility of a demonstration project using the optical mirror-array approach to maskless, or programmable-mask lithography. The target of such a demonstration is 1-6 W/Hr (300 mm wafers) with performance extendable to the 45 nm node and beyond. Mirror-array lithography is an optical approach for direct data transfer to the wafer and is expected to impact low volume manufacturing, rapid design prototyping, mask fabrication, government needs and potentially, advanced process

Mission Critical Research

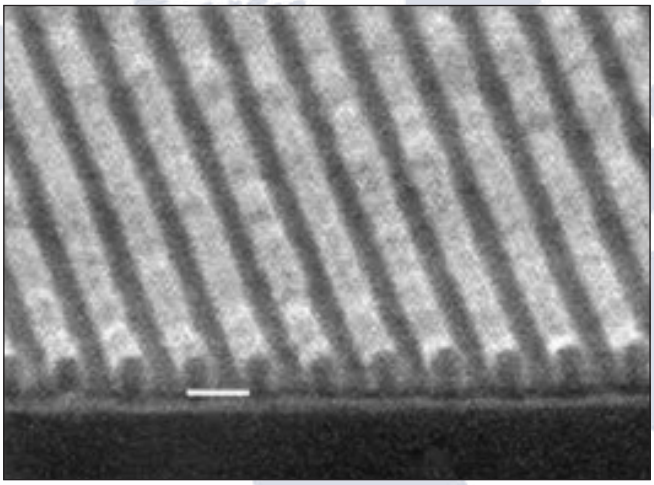


Figure 3: 193 nm Immersion Lithography images of 38 nm dense lines and apaces

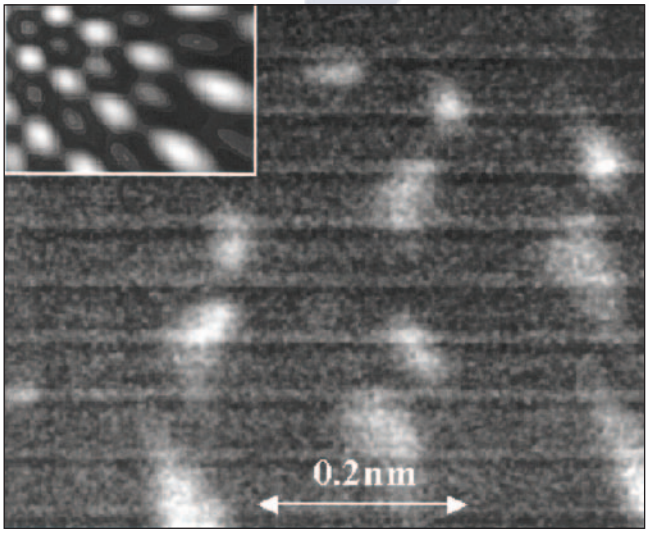


Figure 4: Holographic images of single atoms, simulated (top left) and observed (bottom right)

development.

SRC and DARPA continue to support research that explores the feasibility of an array of approaches to maskless lithography, including multi-axis e-beams and arrays of scanning probes, micro-mirrors, and micro inkjet write heads for niche application insertion at and beyond 2010. These efforts strongly couple with complementary initiatives in high rate data management and hardware-software trade-offs.

SRC Immersion Lithography research contributed to the recent demonstration of a 193 nm immersion lithography system's ability to image 38 nm dense lines and spaces (figure 3). Additionally, research continues to provide important insights into the fluid fill process for immersion lithography and was cited as a 2003 ETAB Compelling Reason for SRC membership.

Recently, the SRC research investment in Step and Flash Lithography has shown promise as an alternate future patterning option. Based on these results and those from other groups, Imprint Lithography was added as a potential solution to the 2003 ITRS Lithography Roadmap. Also, Molecular Imprints announced the release of its first commercial tool, the Imprio 100, based on this SRC and DARPA sponsored research, with three tools having been sold thus far.

Using vapor phase silylation, the first sub-micron positive-tone lithographic pattern developed in pure super critical CO_2 was demonstrated. Additionally, a chemically amplified, intrinsically positive-tone photoresist system has also been developed using super critical CO_2.

Spectroscopic Imaging of Acids in Chemically Amplified Photoresists has yielded a new family of nanoscale material metrology tools. It was demonstrated that it is possible to probe acid-base chemistry in chemically amplified photoresist at the level of a single acid interacting with a single base. These experiments involve using individual, pH sensitive, fluorescent, organic molecules as nanoscale probes of photoresist components and processes. Simultaneous images of protonated and unprotonated materials are demonstrated (figure 5). Data analysis reveals both kinetics and thermodynamics not accessible to ensemble-averaged measurements. Results surprisingly suggest that single molecule kinetics are much slower, on the order of 10s-100s of milliseconds, than previously expected. The thermally activated behavior of the kinetics suggests post exposure bake may be as much about solvation dynamics as it is about acid diffusion. Other promising areas of patterning research include directed organization of block copolymers, molecular glasses, and defect tolerant and holographic imaging of individual atoms (figure 4).

Factory Sciences

The Factory Operations Research Center (FORCe)

conducted research in: Wafer Fabrication (Fab) Scheduling, Intelligent PM Scheduling, Demand Data Mining and Capacity Planning, Demand Forecasting and New Approaches to Simulation. The three-year initial phase, jointly funded by SRC and International SEMATECH, and focused on wafer fabrication, is constituted as a pipeline from concept to research to development to customer. Full process fab scheduling and dispatch approaches were demonstrated in a test bed that incorporated a member company's wafer fab model. These scheduling/dispatch approaches resulted in improved performance against benchmarks and other proposed approaches and provided multiple sub-process solutions for specialized fab modules. Significant improvement was demonstrated in availability of equipment by using preventive maintenance algorithms. A member company is integrating this software into its operations and a supplier is negotiating to incorporate the approach into its products. Another member company is integrating SRC demand forecasting software into its planning systems, and a supplier is exploring development work to also make the capability into a commercial product. An SRC resource-driven approach to scheduling is being used by one company to build its fab model for major run-time reduction. In parallel with the ongoing research, a development project funded by International SEMATECH will take the research results from one of the FORCe projects into the implementation stage via a commercial supplier partnership. This infusion of development support will make the program software available in off-the-shelf products.

Environment, Safety, and Health

Environment, Safety, and Health (ESH) research continues to be an important element of the overall Nanomanufacturing Science mission. The SRC ESH research portfolio is focused at the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing. In 2003 this center is in its eighth year of a 10 year agreement between NSF and SRC. The center has recent emphasis on fundamental studies of CMP tribology, fluid effects, and pad properities in the Back-End Processes Thrust. In the Front-End Processes area the focus is on novel cleaning and surface conditioning as well as the cleaning of new materials such as gate-stack materials. Seed projects in the Factory Integration Thrust focus on the important areas of environmental impact assessment and life cycle analysis. In the patterning thrust, research continues on solventless deposition of resists and super-critical CO_2 developable resists.

As the center approaches the end of its NSF funding cycle, SRC members will plan for the future of ESH research and explore multiple models for continuing research in this area.

Interconnect and Packaging Sciences

The SRC has been in the forefront of research and development of the new Cu-low k dielectric metallization system that has been recently adopted by the semiconductor industry. BEP researchers were among the first to work on this metallization system, starting in the early 1990's, and SRC sponsored research has provided both forefront research and background understanding of the deposition, patterning, and reliability of Cu-low k. In 2003 research sponsored by the Back End Processing (BEP) thrust has made significant progress in identifying and quantifying fundamental limitations in the scalability of Cu metallization. In 1998 it was speculated that increases in resistance of narrow lines due to surface scattering would cause major limitations to extrapolation of metal dielectric systems to future technology generations. In 2002 and 2003, researchers funded by the BEP thrust have shown by careful measurements that the limitations associated with grain boundary scattering and impurity scattering are as significant as that projected for surface scattering. These researchers have begun studies directed at reducing the problems of grain boundaries by using novel techniques to increase grain size in deposited interconnects, as well as researching the basics of electrodeposition with the goal of eliminating the impurities that are deposited in the Cu electroplating step.

A further limitation in the Cu-low k system that has become apparent in the past few years has been the need for very thin barrier materials to prevent penetration of Cu metallization into the low-k dielectrics. The SRC Center for Advanced Interconnect

Mission Critical Research

Science and Technology (CAIST) program has responded to this need with novel research on self-assembled polymeric barriers <5 nm thick that in 2003 have been demonstrated to have excellent barrier properties. Further unique approaches to barriers using atomic layer passivation techniques have been developed, and fundamental understanding of the interactions of possible barrier materials with both low-k materials and Cu has been obtained.

It has been found that dielectrics will require porosity in addition to low-k bulk material to provide the ultra low dielectric constants needed for future interconnect systems. Recent SRC research has shown that it is possible to produce some of these porous materials by use of supercritical CO_2. In this application the bulk materials are saturated with supercritical CO_2, and then the temperature is raised, allowing the supercritical CO_2 to vaporize, forming gas bubbles in the dielectric. The gaseous CO_2 then diffuses through the dielectric leaving the pores to produce a low effective dielectric material. This process has been developed to a transferable state by recent SRC programs.

The use of Cu-low k metal dielectric systems has resulted in many new degradation modes and failure mechanisms. During the past few years SRC programs in both BEP and Packaging thrusts have addressed the identification of such mechanisms and processing necessary to eliminate them. During 2003 SRC researchers developed new reliability evaluation test structures and new reliability measurement methodologies employing both cycled thermal and electrical stress. These new measurement techniques have not only provided a significantly shorter time reliability testing method, but have also allowed the identification of a new failure mode for the Cu-low k system. This capability offers a significant cost savings to member company reliability testing.

Research has proceeded on various aspects of optical interconnects in the 2003 SRC program. SRC researchers have demonstrated optical gain in silicon nanoparticle structures, a significant step towards producing an on-chip optical source for future generations of optical interconnects. Other SRC researchers have demonstrated a radically new method of magnetic assembly of nanopill III-V optical emitters on silicon integrated circuits for on-chip optical interconnects. This method, called Magnetically Assisted Statistical Assembly (MASA), uses a novel combination of magnetic material deposited in cavities on ICs and on one side of nanopill VCEL optical emitters. When the emitter pills are placed in large quantity in a liquid medium, and then washed over the IC, the VCEL pills are attracted to, and retrained in, the cavities on the IC. This unique process concept has been demonstrated in 2003, and will be evaluated further for needed refinements for mass production compatibility in 2004. These two programs, one on on-chip optical emitters and one on hybrid optical emitter fabrication, represent significant contributions to the possibility of optical interconnect for on-chip use. Several programs are investigating novel methods for propagating high speed signals to chips in System-in-Package implementations, using capacitive coupling (figure 5), microwave transmission, and network-like architectures to replace traditional interconnect methods.

Chip cooling has become recognized as one of the major factors enabling continued scaling of ICs. In response to this need, in 2003 the Packaging Thrust identified Thermal Management and Control as a key sub-thrust, and started several new programs in this area.

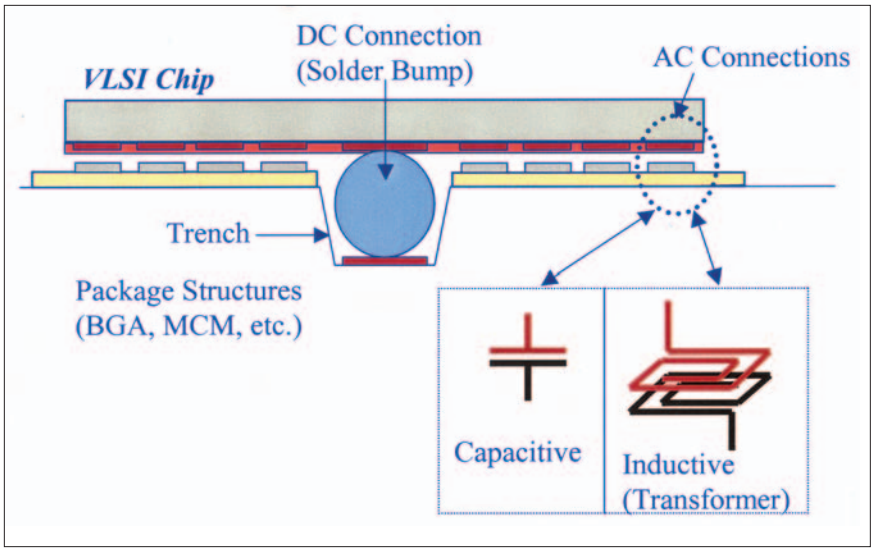


Figure 5: Method for capacitive or inductive on-chip or chip-chip interconnects

Mission Critical Research

Initial work in these programs addressing fundamental studies of the impact of filler distribution on Thermal Interface Materials (TIM) performance, including changes in volume fraction and coordination number, have illustrated a reduced thermal conductivity near TIM boundaries. These studies have led to identification of improved thermal conductivity of particle-polymer composite TIMs filled with carbon nanotubes that eliminate some of the boundary effect, and enhance TIM performance by over 200%.

Design and Tools

Over the past two decades, SRC research in design and design automation has created technologies that today have become mission-critical for member companies. Fundamental research on formal methods in design has evolved into robust tools for verification and synthesis. Many of these techniques have been directly adopted by member companies and incorporated into their advanced design flows, while others have seeded new companies in the design automation industry, which provide tools used by other member companies. Methods and tools for automatic test pattern generation were pioneered by SRC researchers, and are in widespread use today to assure high quality products and rapid yield learning. Compact device models such as the BSIM family have been developed by SRC researchers, and are used worldwide for circuit design in member companies, as well as in commercial tools. Physical design of VLSI circuits has been transformed from a manual activity to a largely automated operation by the development of optimization-based techniques for cell placement, routing, interconnect parasitic analysis, and successive refinement of layouts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap, according to the 2003 ITRS. The future of design in SRC member companies will continue to be enabled by breakthroughs in research that is in progress today. When billion-device circuits designed in sub-22 nm technologies become commonplace, the advanced techniques that form the subject matter of today's research will be the foundations of the necessary design methodologies and tools. Current research programs are addressing these challenges from a number of perspectives.

Integrated Circuit and Systems Design

In this science area, focusing on both circuit design and integrated system design, researchers are developing methods that allow composition of pre-designed system level blocks, guaranteeing compatibility and functionality. In other efforts, a compiler-based design space exploration tool allows rapid evaluation of alternative computer architectures at several different levels of detail, from overall system performance through the timing level. Other research seeks to provide accurate estimation of power dissipation for alternative gate-level architectures, which may be propagated to the system level, where designers can evaluate the impact of design alternatives.

In the near future, reconfigurable systems will become commonplace, due to the extremely high cost of fabrication for ASICs, and the increasing probability that all elements on a chip will not function correctly at all times. Several SRC research programs are aimed at studying various facets of reconfigurability, in anticipation of the mission-critical nature of these techniques. In one effort, a "colloidal computing" paradigm is being developed, in which massive arrays of computing elements can self-assemble into working systems despite the presence of nonfunctional units, as well as self-heal when in-service failures occur.

In another project, onboard monitoring hardware keeps track of program execution, and dynamically reconfigures intense software loops to be executed in hardware for greatly enhanced performance. New architectures are enabling the development of embedded communication applications via pre-designed system-level circuit blocks (figure 6) and reconfigurable interconnection networks. In a particularly futuristic program, researchers are studying probabilistic design techniques that utilize fault-tolerant design modules appearing at the system level to be fault-free; this technique is aimed at implementing complex systems from future nanoscale technologies in which device-level perfection cannot be assumed.

High performance data converters are a vital link in all communications systems and mixed signal applications. In one SRC program, techniques are being studied which will allow 14-16 bit precision

Mission Critical Research

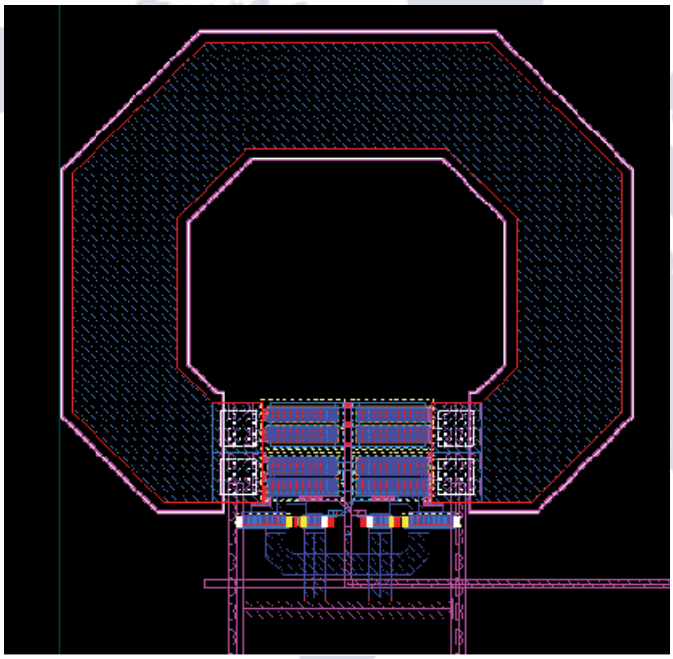


Figure 6: Layout of a 48 GHz VCO in 90 nm CMOS

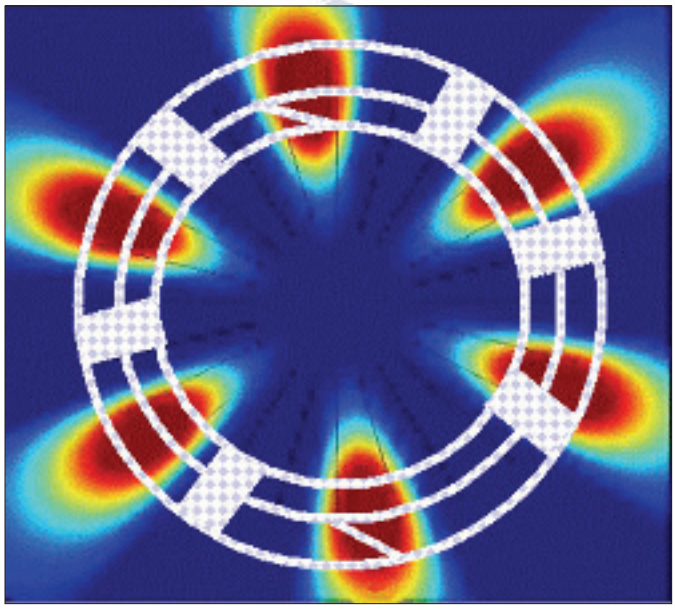


Figure 7: QCA memory with buried clock wires

data converters to be tested and calibrated without the need for expensive, high-precision test systems. In another, 12-bit accuracy at 600 megasamples per second is achieved through the use of massively parallel bandpass converters in a gigabit per second wireless LAN application. In still another, a novel track-and-hold circuit has been developed, which permits 15 bit accuracy in digital radio applications up to 100 megasamples per second.

Radical alternative architectures for future systems are also being explored, in anticipation of the day when scaled CMOS and traditional interconnect architectures will no longer be adequate. An SRC research effort is developing advanced architectures in which computation is embedded and distributed throughout terabyte-level memory systems, using quantum cellular automata (QCA) rather than gate-level logic (figure 7). In another program, novel signal representations inspired by biological neural processing are being investigated as an alternative in the age of sub- 1 volt processes which do not support precision analog circuitry.

Automated tools, long an integral part of digital design, are making their way into analog and mixed signal design through SRC research. A program in verification is extending formal methods to analog design through hybrid system model checking, allowing critical behaviors in important classes of mixed-signal designs to be verified formally. Several programs in test address the incorporation of analog and digital circuits on a single chip: accurate testing using repeatable low-accuracy input signal generators; built-in self test for analog circuits; use of digital test infrastructure on System on Chip designs. All of these efforts are important in reducing the burgeoning test cost of advanced designs.

Challenges in design for future technologies require tools that reach in two directions: up to manipulations at higher levels of design, and down to interfaces with manufacturing. As technology dimensions decrease, techniques such as optical proximity correction become necessary but expensive. At the design level, SRC research enables Optical Proximity Correction (OPC) to be applied selectively, reducing turn-around time and increasing yield while reducing manufacturing cost (figure 8). In the critical area of power reduction, with leakage current becoming a critical factor, researchers experimenting with voltage scaling and multiple voltage levels have discovered methods that will be coupled with tools at all levels to address the power challenge. And with leakage current a growing factor, SRC research is aimed at fast estimation of total leakage current for large circuits and leakage current minimization; and statistical timing analysis techniques that take into account variability in process characteristics and supply voltage.

Mission Critical Research

At the other end of the spectrum, the ability to make decisions for System-on-Chip and System-in-Package Designs without detailed implementation requires fast, accurate estimators and higher-level manipulation techniques. Research programs at SRC will enable early performance prediction and correction, and high-level planning of circuits and interconnects in mixed signal design (figure 9).

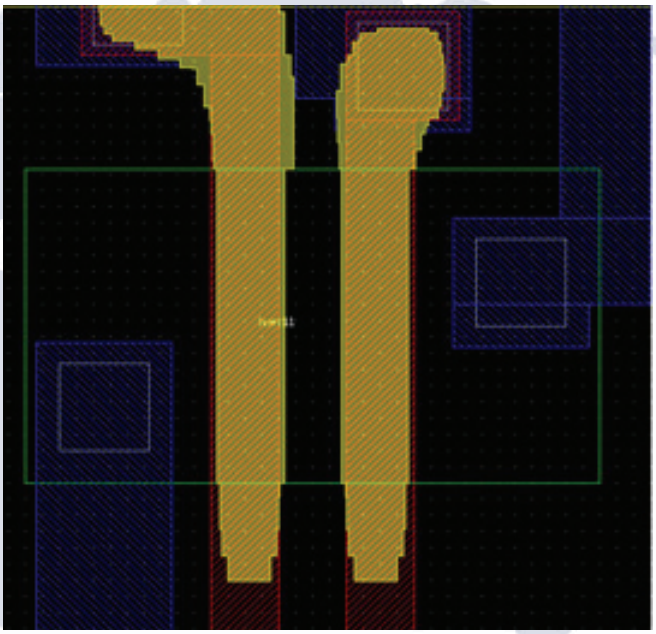


Figure 8: Selective OPC for better patterning

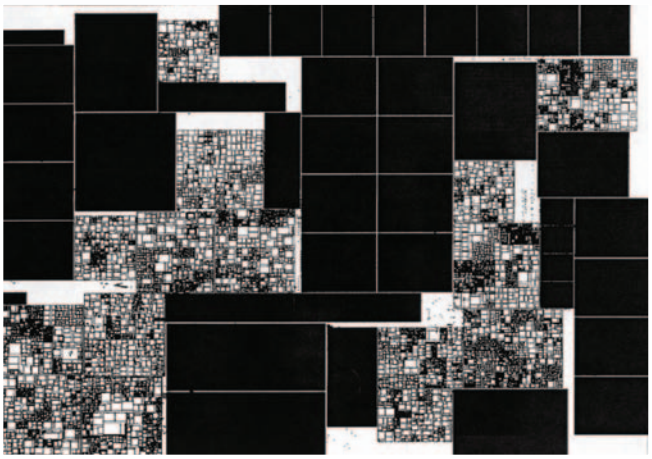


Figure 9: Mixed-Mode chip planning: blocks and cells

Exploring Future Technologies

Paradigm Shift in Computing Technologies

SRC research on new devices ranges from new FET-like structures that will preserve current design methodologies and systems architectures to completely new approaches to representing the logic state and information processing. For example, novel FET concepts, such as "MOTT Transistors'' and "Electrically Controlled Optical Switch" are being explored to sustain FET device architecture for high density, high performance and low power scaling. Conversely, a new phase-based technology amenable for implementation by cellular nonlinear networks and that may permit ultra-low-power logic is under investigation. To make use of these emerging devices, new systems architectural approaches are being explored as alternatives to von Neumann Computing. For example, the "Delay-based Architecture" concept that makes use of time delays as a state variable rather than charge of voltage in more conventional systems is being studied.

Novel ideas are needed to address the anticipated increases in power dissipation of high performance integrated circuits as scaling continues and to manage increasing variability on-chip of device parameters. SRC is addressing the former challenge via exploratory projects in probabilistic design and fault tolerance and the latter challenge with research in adiabatic computing and novel heat removal concepts. Exploratory projects in self-assembly, magnetic semiconductors, spintronics, and interconnects methodologies are also underway.

Enabling Technologies for Emerging Applications

To address the emerging new markets for the semiconductor industry, SRC has begun to invite proposals on concepts for enabling technologies for emerging applications, such as, devices for energy scavenging from the environment, security/encryption for mobile applications, speech recognition, ambient intelligence, machines that can conceptualize from data, holographic meetings, etc. The present portfolio emphasizes Bio-Electronic Interfaces and Organic Electronics/E-Textiles. For Bio-Electronic Interfaces, research is underway on integrated neuroelectronic systems and active bio-CMOS chips. The former project conducts basic research on ionic/electronic interfaces and low voltage signal processing and the latter is focused on organic/inorganic interfaces and may lead towards new applications, such as "Gene Chips."

Focus Center Research Program

Semiconductor Industry Association (SIA):
- Advanced Micro Devices, Inc.
- Agere Systems
- Analog Devices, Inc.
- Conexant Systems, Inc
- Cypress Semiconductor
- IBM Corporation
- Intel Corporation
- LSI Logic Corporation
- MICRON Technology, Inc.
- Motorola, Incorporated
- National Semiconductor
- Texas Instruments
- Xilinx, Inc.

Semiconductor Industry Suppliers:
- Air Products & Chemicals, Inc.
- Applied Materials, Inc.
- Cadence
- KLA-Tencor Corporation
- Novellus Systems, Inc.
- Synopsys
- Teradyne, Inc.

Department of Defense:
- Deputy Undersecretary of Defense for Laboratories and Basic Sciences (DUSD/LABS)
- Defense Advanced Research Projects Agency (DARPA)

SYSTEM DESIGN AND TEST

The University of California at Berkeley is the lead university for this focus center, the Gigascale Systems Research Center (GSRC) with **Professor Jan Rabaey** as the center's director. The center's research agenda focuses on pertinent problems the semiconductor industry faces in the next decade in the areas of system design, integration, test and verification. To sustain current growth, the industry requires orders of magnitude of improvement in energy efficiency, cost, reliability and time-to-market.

To address the multiple challenges within this focus, the center is structured along eight interlocking research themes, each of which is led by a theme leader. The horizontal themes, Heterogeneous System Design & Integration and Soft Systems, represent two visions on how integrated systems are to be realized. These horizontal themes are combined with four vertical ones, each of which addresses one particular aspect of embedded integrated system design. The Power-Aware Systems, Reliable Systems, System Verification and Embedded Self-Test themes, respectively, address the power and energy, reliability, verification and test roadblocks that are looming on the horizon. Finally, the System-Level Living Roadmap provides an environment to explore how the different cost metrics of design will evolve in the next decade, taking a system-level view. This high-level perspective is unique and complements and builds on top of the existing roadmapping efforts. This effort, which encompasses and integrates all the research activities of the center, is essential in identifying emerging challenges and in steering the research evolution of the center.

UNIVERSITY OF CALIFORNIA, BERKELEY
- Carnegie Mellon University
- Massachusetts Institute of Technology
- Pennsylvania State
- Princeton University
- Purdue University
- Stanford University
- UCLA
- UC/San Diego
- UC/Santa Barbara
- UC/Santa Cruz
- University of Michigan
- Univ. of Texas / Austin
- University of Wisconsin

CIRCUIT DESIGN AND TEST

The Focus Center for Center for Circuits and Systems Solutions (C2S2) is led by Carnegie Mellon University, and **Professor Rob Rutenbar** is the director. The center aims to develop new circuit design techniques needed to convert novel devices into robust performance across the most diverse range of applications.

Relentless scaling of semiconductor devices toward fundamental physical limits threatens to make obsolete today's most basic circuit design assumptions. Today's landscape of familiar trade-offs — area, speed, power, frequency, noise, reliability, linearity, yield, cost — is shifting radically. To build tomorrow's complex, integrated, heterogeneous systems, the industry requires a foundation of circuit designs it can trust.

Circuits play a unique role in the "food chain" from materials to gigahertz: they hide the physics from designers; they form the most basic system-building blocks; and they provide the essential traction for handling billions of competing system implementation details.

C2S2 research invents the new design techniques necessary to convert near-limit scaled devices and post-silicon devices into useful system-building blocks. It targets these design innovations across diverse design domains: digital, analog, RF, photonic, and MEMS designs.

Research in the Circuit Design Center provides the needed link between devices and system design.

CARNEGIE MELLON UNIVERSITY
- Columbia University
- Cornell University
- Massachusetts Institute of Technology
- Princeton University
- Stanford University
- UC /Berkeley
- University of Illinois at Urbana-Champaign
- University of Michigan
- University of Washington

Focus Center Research Program

INTERCONNECT

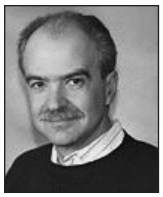
The Interconnect Focus Center (IFC), led by Georgia Institute of Technology with **Professor James Meindl** as the director, conducts research to discover and invent new electrical, optical and thermal interconnect solutions that will meet or exceed ITRS projections and enable hyper-integration of heterogeneous components for future terascale systems.

The center focuses on research of all aspects of the wiring that connects the millions of transistors on a microchip, from process to system-level architecture. Today and in the future, the microelectronics and nanotechnology industries will lead the evolution of technology in industries from automotive to medical, and from computing to aviation. The IFC strives to stay atop all advances in these fields and play a major role in driving this technology into the future. To that end, the center's research themes have evolved to accommodate this goal.

The research focus in IFC is to discover and invent electrical, optical and thermal interconnect solutions that enable hyper-integration of heterogeneous components.

GEORGIA INSTITUTE OF TECHNOLOGY
- Stanford University
- Massachusetts Institute of Technology
- SUNY Albany
- Rensselaer Polytechnic Institute
- Cornell University
- University of California, Santa Barbara
- University of Central Florida
- University of Texas at Austin
- Carnegie Mellon University
- North Carolina State University
- University of California, Berkeley

MATERIALS AND DEVICES



Materials and Devices research is conducted by the Center for Materials, Structures and Devices (MSD), at the Massachusetts Institute of Technology. **Professor Dimitri Antoniadis** is the center director. This center's focus is to explore and determine the most promising path for microelectronics in the next two to three decades by pursuing two overlapping approaches: scaling of CMOS to its ultimate limit and interdisciplinary exploration of new-frontier devices.

Since its inception in 2000, the MSD Center has successfully launched entirely new materials combinations for high performance CMOS applications, while pushing new frontier devices, such as carbon nanotubes to new heights of performance through the combination of novel chemical synthesis of nanostructures with advanced front-end processes borrowed from silicon technology. In addition, the MSD Center is well along its way to establishing realistic benchmarking of highly disparate devices on equal footing, via close collaboration of experimentalists from different disciplines with advanced modeling and simulation researchers.

Research in this center is organized into five research themes. Four of the themes concentrate on experimental research in device technology while the fifth collaborates with the other four in addressing key process and device issues by advanced modeling and simulations.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
- California Institute of Technology
- Cornell University
- North Carolina State University
- Pennsylvania State University
- Princeton University
- Purdue University
- Stanford University
- SUNY Albany
- University of Texas, Austin
- University of Virginia
- University of California, Berkeley
- University of California, Los Angeles
- University of California, Santa Barbara
- University of Florida

NANO MATERIALS

Research in Nano Materials is conducted by the Focus Center on Functional Engineered Nano Architectonics (FENA), the newest focus center. **Professor Kang Wang** of UCLA is the center director. The center's research is directed at resolving the cross-cutting materials and device challenges related to beyond-CMOS in order to create new information processing paradigms with greater capabilities.

In order to tackle major challenges common to all nanometer scale devices, new nanoscale materials and processes are needed to address the core problems of nanoscale technology. Opportunities exist for creating a new generation of nanoscale materials, structures and devices, which will extend semiconductor technology to CMOS limits and beyond, and provide heterogeneous interfaces of new nanosystems, enabling a combination of biological and molecular functions that lead to new paradigms of information processing and sensing. Through this new generation of nanostructured materials, the semiconductor industry will continue to expand and create new applications of monolithically integrated (CMOS, molecular and biomolecular) nanosystems. FENA focuses on the materials challenges at the nanoscale for fulfilling these opportunities.

UNIVERSITY OF CALIFORNIA, LOS ANGELES
- University of California, Berkeley
- Stanford University
- University of California, Santa Barbara
- University of California, Riverside
- University of Southern California
- California Institute of Technology
- North Carolina State University
- Massachusetts Institute of Technology
- University of Minnesota
- SUNY Stony Brook
- Arizona State University

TECHCON 2003

TECHCON 2003, SRC's sixth major technical conference was held in Dallas, TX in August 2003. The event's success is attributed to the 130 students who presented papers and to the presentations: keynote address by Paul Horn, IBM senior vice president and director of research; a luncheon address by Art George, TI High Performance Linear Business Unit vice president; and presentations by many outstanding faculty and Nobel Laureate Richard Smalley. Special sessions included the SiGe Design Challenge winners and invited papers from the Focus Center Research Program.

Sixty SRC Fellows and Scholars participated in TECHCON 2003, presenting 32 papers and 46 posters, and winning seven Best in Session Awards. The Fellows Award went to Douglas Cannon, Novellus/SRC Fellow from MIT.

The Graduate Fellows Program banquet keynote was delivered by Dr. Claudine Simson, Motorola Corporate Vice President.

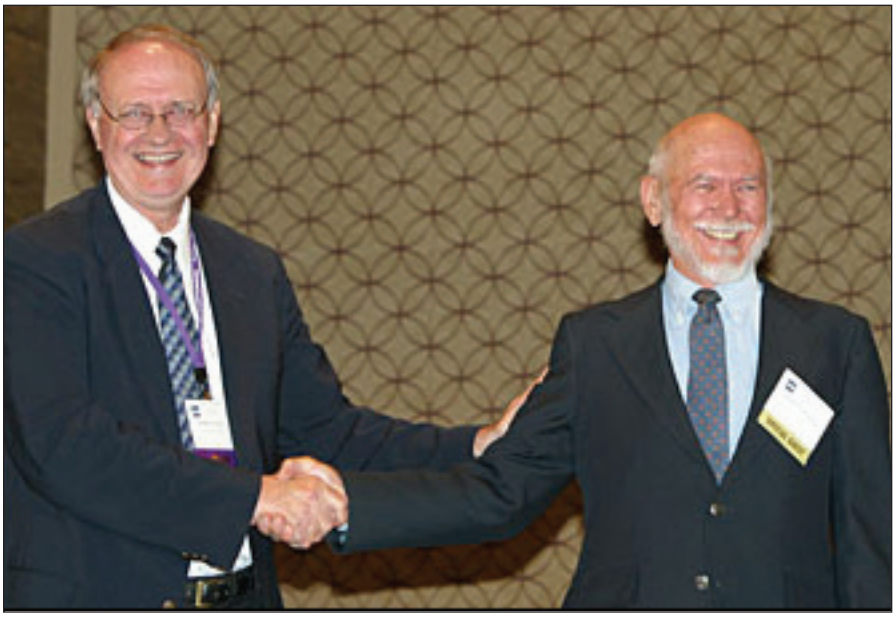
Networking opportunities abounded at TECHCON 2003, particularly in TechFair and at CareerConnections where eight SRC member companies took advantage of recruiting opportunities with some of the top students in microelectronics-related disciplines.

TECHCON Stats at a Glance

• Student presenters (SRC, FCRP, and SiGe Design Contest)	141
• Graduate Fellows and Master's Scholars presenters	46
• Technical paper sessions	16
• Special sessions (Copper Contest, e-Collaboration, Bio-Inspired Computing, and 21st Century Energy Initiatives)	4
• Total presentation sessions	20
• Faculty and Student Attendees	218
• Member Company attendees	155
• SRC staff & Guest attendees	34
• Total Conference Attendees	409
• Member companies participating in Career Connections	8
• SRC Awards presented (other than Best in Session)	125

Aristotle Award

The 2003 Aristotle Award was made to Professor Jimmie Wortman, North Carolina State University (retired). The Aristotle Award recognizes SRC-supported faculty whose deep commitment to the educational experience of SRC students has had a profound and continuing impact for SRC members over a long period of time. The award acknowledges outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project. Ralph Cavin, SRC VP for Research Operations, presented the 2003 Aristotle Award to Professor Wortman at TECHCON 2003.



Award Recipients

TECHCON Best in Session

130 students presented their research at TECHCON 2003 in four sets of four concurrent technical paper sessions with each set being followed by a TechFair poster session for papers presented in that set. Presentations were judged both on paper and poster presentation.

Session 1: CADTS: Test & Testability
Le Jin - Iowa State University
Linearity Testing of Precision Analog-to-Digital Converters Using Nonlinear Inputs

Session 2: ICSS: System Design
Claire Fang - Carnegie Mellon University
Efficient Static Analysis of Fixed-Point Error in DSP Applications via Affine Arithmetic Modeling

Session 3: DEVICES: Novel Devices & Modeling
Eric Pop, IBM/SRC Fellow - Stanford University
Monte Carlo Simulation of Heat Generation in Silicon Nano-Devices

Session 4: INT & PKG: Global Interconnect
Anthony Mule - Georgia Institute of Technology
Sea-of-Leads Wafer-Level Package with Optical Waveguides, Volume Grating Couplers

Session 5: CADTS: Design Verification
Smriti Gupta - Carnegie Mellon University
Towards Formal Verification of Analog and Mixed-Signal Designs

Martha Montague, AMD/SRC Fellow, University of Wisconsin, receives a Best in Session Award from Mr. Richard Schinella (r), SRC Board Chair from LSI Logic, and Dr. Dinesh Mehta (l), SRC.

Session 6: ICSS: Circuit Design
Cassondra Neau, SRC Fellow - Purdue University
Leakage Reduction Techniques for Nanometer Scale CMOS Circuits

Session 7: NANOMANUFACTURING: ESH
Subramanian Tamilmani - University of Arizona
Electrochemical Treatment of Copper CMP Waste Water Using Boron Doped Diamond Thin Film Electrodes

Session 8: INT & PKG: Interface & Reliability
Brian McAdams - Lehigh University
Initiation and Propagation of Delamination at the Underfill/Passivation Interface in Flip-Chip Assemblies

Session 9: CADTS: Logic & Physical Design
David Chinnery - University of California at Berkeley
Power Minimization with Multiple Supply Voltages and Multiple Threshold Voltages

Session 10: NANOMANUFACTURING: Patterning
Frank Gennari - University of California at Berkeley
Linking TCAD and EDA Through Pattern Matching

Session 11: DEVICES Nonclassical CMOS & Modeling
Douglas Cannon, Novellus/SRC Fellow - Massachusetts Institute of Technology
Near-infrared Ge Photodetectors Fabricated on Si Substrates with CMOS Technology

Session 12: INT & PKG: Thermal Management & Unit Process
Ward Engbrecht, Novellus/SRC Fellow - University of Texas at Austin
Boron Carbon-Nitride Films Deposited by Low Temperature Chemical Vapor Deposition

Session 13: Mixed Signal Technologies
Yong Wang - University of Washington
Integral Equation-Based Coupled Electromagnetic-Circuit Simulation in the Frequency Domain

Session 14: NANOMANUFACTURING: Patterning Materials
Martha Montague, AMD Mahboob Khan / SRC Fellow - University of Wisconsin
Imaging Layers Based on Surface-Initiated Polymers

Session 15: DEVICES: Front End Processes and Materials
Milan Diebel - University of Washington
Investigation and Modeling of Fluorine Co-Implantation Effects on Dopant Redistribution

Session 16: NANOMANUFACTURING: Factory
Xiaodong Yao- University of Maryland
Optimal Preventive Maintenance Policies for Unreliable Queueing/Production Systems with Applications to Semiconductor Manufacturing

Award Recipients

Mahboob Khan Award

The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as Industrial Liaisons. Recipients represent "ideal mentors" whose commitment more than enhances the SRC research program. The 2003 award recipients were:

Will Conley of Motorola has worked with Professor Grant Willson's group at UT-Austin for the past 3 years. He has chosen to interact directly with 11 students on a regular basis during the contract time period. He has arranged for multiple on and off campus experiences that provided a direct connection and alignment to the needs of the semiconductor industry. Thus preparing these students to excel in the "real world."

Larry Gochberg of Novellus Systems has served as an Industrial Liaison to the Optical Discharge Modeling Group at the University of Illinois/Urbana-Champaign under the direction of Professor Mark Kushner of UIUC for over 4 years. Larry served as a role model to two UIUC students, Ron Kinder and Junqing Lu, who later joined the Novellus Systems staff.

Hosam Haggag a Senior Test Engineer at National Semiconductor has had a significant impact on a number of SRC researchers and students. He has arranged multiple student internships to develop design and test skills and to promote joint research interaction. His responsiveness to issues within our community is motivated by the desire for outstanding and useful results.

Mani Janakiram of Intel is synonymous with the success of SRC's Factory Operations Research Center program. Also know as FORCe, the program includes University of Maryland's Michael Fu and Steven Marcus, University of Cincinnati's Emmanuel Fernandez, and UC-Berkeley's Lee Schuben. Mani has held a key and leading role in establishing an open forum within the SRC community to discuss, identify and prioritize industry needs in the broad area of factory operations.

Turker Kuyel of Texas Instruments has worked with Professors Randy Geiger and Degang Chen at Iowa State University researching "A New Strategy for Built-In Self-Test of Mixed Signal Integrated Circuits". Turker supervised Iowa State student Kumar Parthasarathy during a summer internship that later resulted in Kumar accepting a permanent position at TI after graduation.

Pawitter Mangat of Motorola has worked with the Center for NanoTechnology at the University of Wisconsin for the past 6 years. His continued support to Professors Franco Cerrina, Roxann Engelstad, and Paul Nealey has been a key component for the success of the Advanced Lithography and Metrology research project.

Luu Nguyen of National Semiconductor has teamed up with both Professor King-Ning Tu of UCLA and Professor Ganesh Subbarayan of Purdue University to provide an exceptionally high quality of scientific research that not only challenges the best out of himself and others, but also provides every possible help in achieving excellence in those around him.

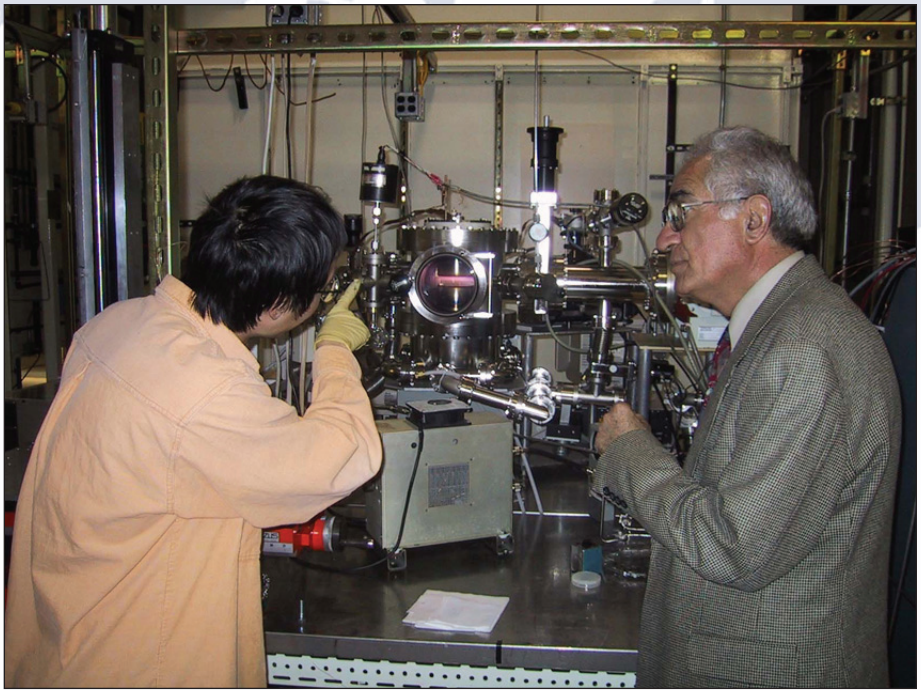
Technical Excellence Award

This award is given to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research, who are ground-breakers and leaders in their fields, and who are regarded as model collaborators with their colleagues in the SRC member community.

Work in the area of Analysis and Optimization of Signal and Supply Networks by Professor Sachin Sapatnekar of the University of Minnesota was selected for the 2003 Technical Excellence Award. According to Industrial Liaison, Sani Nassif of IBM, what is "most impressive about Dr. Sapatnekar's work is his willingness to take risks in looking at very hard problems and putting the appropriate amount of energy on a problem and understanding when it is appropriate to stop an avenue of exploration. True excellence is in doing a number of things very well."

Dr. Sapatnekar received his doctorate under direction of Dr. Steve Kang in an SRC program at the University of Illinois Urbana/Champaign in 1993 and became an SRC Principal Investigator in 1998.

Student Programs



Hong Biz Zhu (left), SRC student, and Professor Farhang Shadman (right) work with a plasma chamber at the University of Arizona.

More than 1,100 students participated in SRC-funded research in 2003, another 350 under MARCO/FCRP research. Of SRC students graduating in 2003, about 70% went to work for SRC member organizations or are undergraduate or master's students continuing to higher degrees, further strengthening the links within the SRC community. Other 2003 accomplishments included:

• Eight new core Fellowships, six new Company-Named Fellowships and one new International Fellowship were awarded through the Graduate Fellowship Program to bring the number of fellowships at the beginning of the 2003 fall term to 52. Sixteen Fellows graduated in 2003.

• The first Peter Verhofstadt Fellowship was awarded, and the Robert M. Burger Fellowship was awarded for the sixth time.

• Thirteen new Master's Scholarships were awarded, including 9 new Company-Named for a total of 18 at the beginning of the 2003 Fall term. Three of the new scholarships were awarded to graduates of the Undergraduate Research Assistants Program. Thirteen Master's Scholars graduated in 2003.

• 130 SRC students presented papers and/or posters at TECHCON 2003.

• 753 resumes were published on the SRC Web site.

• The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars. A copy may be obtained by contacting SRC Student Relations at the SRC corporate address.

• The second Simon Karecki Award was made from the Simon Karecki Endowment to Nikhil Krishnan, University of California/Berkeley. This award recognizes outstanding student performance through the SRC/NSF Center for Environmentally Benign Semiconductor Manufacturing, centered at the University of Arizona.

• The first MARCO/FCRP student/industry networking events were held in conjunction with the annual research reviews.

• TechConnects were held at the University of California/San Diego, University of Washington, and Rensselaer Polytechnic Institute.

SRC Education Alliance

The SRC Education Alliance (SRCEA), a wholly-owned subsidiary of the SRC, is a non-profit (501-c-3) charitable foundation. The Undergraduate Engineering Programs, including MOSIS and the Undergraduate Research Assistants Program are managed through the SRCEA; funding for these programs was provided by the SIA and SIA Board companies and ended in June 2003. Further information on these programs can be obtained from SRC Student Relations.

Impact of SRC-Guided Research

An indicator of both the quality and the impact of SRC research is the number of citations that SRC research papers have received. The table below lists twelve papers, all written by SRC researchers, that have each been cited more than 100 times. Papers cited as often as these are rare in the scientific literature, and a few approach the number of citations given to papers of Nobel Laureates.

1. "Point Defects and Dopant Diffusion in Silicon" by Plummer et al. (1989) Stanford
   503 citations 188 citations by industry (37%)

2. "Asymptotic Waveform Evaluation for Timing Analysis" by Pillage and Rohrer (1990) U Texas/Austin
   251 citations 88 citations by industry (35%)

3. "Ferroelectric Materials for 64 Mb and 256 Mb DRAM" by Parker and Tasch (1990) U Texas/Austin
   150 citations 40 citations by industry (27%)

4. "Alternative Dielectrics to Silicon Dioxide For Memory and Logic Devices" by Kingon et al. (2000) NCSU
   154 citations 37 citations by industry (24%)

5. "Hole Injection SiO2 Breakdown Model For Very Low Voltage Lifetime Extrapolation," by Schuegraff and Hu (1994) Berkeley
   135 citations 60 citations by industry (44%)

6. "Large-Scale CVD Synthesis of Single-Walled Carbon Nanotubes," Dai et al. (1999) Stanford
   133 citations 17 citations by industry (13%)

7. "Switching Devices Based on Interlocked Molecules" by JR Heath et al. (2001) UCLA
   125 citations 6 citations by industry (5%)

8. "BSIM - Berkeley Short-Channel IGFET Model for MOS-Transistors" by Sheu et al. (1987) Berkeley
   120 citations 41 citations by industry (34%)

9. "Plasma-Enhanced Chemical Vapor-Deposition – Differences Between Direct and Remote Plasma Excitations" by Lucovsky and Tsu (1987) NCSU
   113 citations 12 citations by industry (11%)

10. "Importance of Space-Charge Effects in Resonant Tunneling Devices" Lundstrom et al. (1987)
    102 citations 16 citations by industry (16%)

11. "Threshold Voltage Model For Deep-Submicrometer MOSFETs" by Hu et al. (1993) Berkeley
    101 citations 37 citations by industry (37%)

Intellectual Property

Intellectual property (IP) assets covering SRC-sponsored university research programs are provided by SRC to its members to protect and enhance the value of SRC membership. IP assets serve to support SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs to SRC member companies. SRC's significant portfolio of intellectual assets minimizes the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship. IP assets are interwoven with the SRC research catalog and complement the value chain as an important benefit of SRC membership.

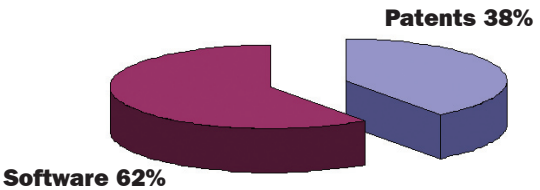
In return for sponsorship, SRC receives non-exclusive, worldwide, royalty free licenses to IP from university research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results may be provided, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to provide a level playing field for members by ensuring that those who utilize SRC-sponsored technologies do so only within the scope of a valid license.

SRC is investigating ways in which IP assets can provide new and additional sources of value to the SRC member community. In 2002, SRC and North Carolina State University pioneered an innovative joint licensing and commercialization partnership focused on commercializing selected inventions. This new program significantly benefits SRC members by increasing their potential competitive advantages while also providing for a possible new source of royalties. This year we presented the Exclusive Licensing Model to several universities and member companies, where it has received strong support. Under this new licensing model, select SRC and university intellectual property rights are combined and licensed to SRC. The formerly separate IP rights have greater value once combined in an escrow managed by SRC. As a result, enhanced commercialization prospects and greater licensing value can be provided as compared with the traditional SRC-university licensing model. The university, SRC, and SRC member companies agree on terms to sublicense one or more companies able to commercialize the invention and share the royalties collected. SRC, SRC member companies, and several universities are working together to implement this new experimental licensing model.

SRC's IP Advisory Board (IPAB), comprised of several SRC member company representatives, has worked closely with SRC on IP matters. This year SRC and the IPAB created a detailed IP Value Model to quantify the relative value of IP to SRC and its members.

During 2003, fourteen SRC-sponsored U.S. and foreign patents issued, bringing the total portfolio of SRC licensed patents to 209. SRC's significant patent portfolio supports both U.S. and international member company operations in numerous countries around the world. SRC's website permits members to submit realtime queries into SRC's IP database to obtain status on pending and issued patents as well as information on SRC-sponsored software.

IP PORTFOLIO COMPOSITION



SRC IP portfolio also provides over 348 software programs, software models, and technical databases to member companies. Software and database licenses from SRC-sponsored research programs represent a growing and complementary part of SRC's IP portfolio. Members are directed to the online software directory at URL http://www.src.org for further details. SRC members receive non-exclusive, worldwide, royalty-free intellectual property licenses in applicable software programs and technical databases.

SRC U.S. and Foreign Patents ISSUED IN 2003

Title Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Solventless, Resistless, Direct Dielectric Patterning Karen Gleason, Christopher Ober, Daniel Herr *Taiwan patent #NI-171285 issued on 2-Jun-03	12-Jan-00 21-Jan-03	6509138 (U.S.)	MIT Cornell Univ.
Binary Non-Crystalline Oxide Analogs of Silicon Silicon Dioxide for Use in Gate Dielctrics and Methods of Making the Same Gerald Lucovsky *Taiwan patent #NI-180834 issued on 11-Nov-03	5-Nov-99 22-Apr-03	6552403 (U.S.)	North Carolina State University
Supermolecular Structures and Devices Made from Same Daniel Herr, Victor Zhirnov	23-Feb-00 16-Dec-03	6664559 (U.S.)	n/a
Method of High Performance CMOS Design Su Kio, Gin Yee, Larry McMurchie, Carl Sechen, Tyler Thorp	14-Sep-00 15-Apr-03	6549038 (U.S.)	Univ. of Washington
Method and Apparatus for Double-sampling a Signal David Allstot, Douglas Beck	11-Mar-02 13-May-03	6563348 (U.S.)	Univ. of Washington
Formal Verification of a Logic Design Through Implicit Enumeration of Strongly Connected Components Peter Beerel, Aiguo Xie	28-Jun-01 25-Feb-03	6526551 (U.S.)	Univ. of Southern California
Lanthanum Oxide-Based Gate Dielectrics for Integrated Circuit Field Effect Transistors and Methods of Fabricating Same Angus Kingon, Jon Paul Maria	17-Jan-01 11-Mar-03	6531354 (U.S.)	North Carolina State University
High Mobility Heterojunction Transistor and Method Sanjay Banerjee, Qiqing Ouyang, Al Tasch	24-May-01 6-Nov-03	NI-179065 (Taiwan)	Univ. of Texas at Austin
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