Semiconductor Research Corporation®

Pioneers in Collaborative Research®

2004 ANNUAL REPORT

SRC Mission, Vision, and History

Mission

The SRC's mission is to manage a range of worldwide, consortial, academic-based research and education programs, each matching the needs of their sponsoring entities.

The SRC's core research program provides:

- Innovative, strategic, pre-competitive research guided by the ITRS, focusing on universities
- University graduates with high rate of placement in member companies
- A global forum for pre-competitive collaboration among all segments of the semiconductor industry, universities and governments
- Advocacy to various government and other funding agencies for support of University semiconductor research
- A comprehensive Value Proposition that focuses on maximizing member value

Vision: The SRC operates globally to provide competitive advantage to its members as the world's premier university research management consortium delivering relevantly educated technical talent and early research results.

SRC Historical Highlights

1981 – Robert N. Noyce, SIA Chair, announced the creation of SRC in December

1982 – SRC officially formed; Eric Bloch, IBM, first BOD chair; Larry Sumney named Executive Director

1983 – Industrial Liaison (mentor) program launched

1984 – First Executive Technical Advisory Board (ETAB) Summer Study held

1986 - SRC has 35 member companies; government participation initiated

1987 – SEMATECH and National Advisory Committee on Semiconductors established as a result of SRC initiatives

1988 – SRC Competitiveness Foundation created as a subsidiary of SRC; became the SRC Education Alliance (SRCEA) in 1993

1992 – National Technology Roadmap for Semiconductors created in a major industry cooperative effort led by SIA to define specific five-year technology goals; internationalized in 1998 and updated biennially

1997 – MARCO created as a subsidiary of SRC and the first Focus Centers established in 1998

2000 – First-ever SRC Landmark Innovation Award presented to Dr. Farhang Shadman by Nobel Laureate Jack Kilby at TECHCON 2000; UMC Group becomes first international member

2001 – SRC research program internationalized with National Taiwan University

2004 – Industry surpasses $629 million invested through SRC since inception to develop technology and talent, with nearly 3300 students receiving advanced degrees from SRC–supported programs; a record 20 SRC-sponsored patents were issued, bringing the total to 233

Message from the President

Since inception, SRC's research agenda has been aligned with a "roadmap." This roadmap began as the identification of the major research needs to advance industry's capability to achieve major goals that had SRC member consensus. As an example, a major goal in the early 1980's was to conduct the research that would enable the fabrication of a 256 MB DRAM in 1994. Over the next several years, this concept of research roadmaps evolved resulting in the creation of a National Advisory Committee on Semiconductors in 1988. Its purpose was to devise and promulgate a national semiconductor strategy to enable restoration of U.S. leadership in the semiconductor industry. Dr. Ian Ross who, at that time, was President of Bell Labs chaired the NACS. Seven major reports were issued between 1989 and 1992. The NACS initiative with the most lasting impact was the Micro Tech 2000 Workshop (with over 100 industry and government attendees) that developed an industry roadmap, to enable the creation of the technology to manufacture a 1 GB SRAM to benefit U.S. competitiveness. Recognizing that it was not in a position to implement this roadmap, the NACS requested that the SIA assume the responsibility. SIA, in turn, created a Technology Strategy Committee (TSC) that decided that the SRAM might not be the appropriate vehicle for all of its members and decided to refocus the roadmap. Efforts to do that involved over 200 people. This process resulted in a more complete plan that provided the basic approach that is used today, e.g. technology node cadence defined by feature size progression. The intent was to enable the research community to provide the knowledge needed in a timely manner to meet the goals. This was implemented in the 1992 National Technology Roadmap for Semiconductors (NTRS). It was revised and updated in 1994 and again in 1997, and in 1998, it became the International Technology Roadmap for Semiconductors (ITRS). Today, the ITRS is a highly refined and detailed document resulting from contributions by technology experts from all over the world.

The current ITRS lays out the research needs for the industry to take the CMOS transistor to its fundamental scaling limits. This is envisioned today to occur in the 2018 time frame. To do that, "innovate, we must" because many new technologies will be necessary to enable CMOS to be scaled, manufactured, and to operate at its scaling limits.

Both the SRC's Core Research Program and MARCO's Focus Center Research Program are primarily directed toward research to enable CMOS technology to continue to scale to its fundamental limits. Thus, Moore's Law for CMOS should continue for the next thirteen or so years. But, in order to continue to reduce cost per function beyond that time, what path should industry take, i.e., what will be the next "switch" and what supporting technologies and manufacturing paradigms will be required to make it commercially viable?

A recent SRC study estimates that the length of time from the first publication of a key research result to its commercialization is about 12 years on average. Therefore, the identification of the next switch in the next several years and supporting manufacturing technology is needed and, we believe, the industry agrees.

SRC has been asked by the SIA to establish a new subsidiary, the Nanoelectronics Research Corporation (NERC), to help carry out the SIA's Nanoelectronics Research Initiative (NRI). NERC's first activity will be to survey what nanoelectronics research is already being funded by the federal government.

The intent beyond that is to identify the most promising approaches, both from federal research efforts as well as research in other countries. We expect a "beyond CMOS" roadmap will be necessary and will be developed to guide the beyond CMOS research efforts. And, as with extending CMOS to its theoretical limits, "innovate, we must," as research in the beyond-CMOS area is carried out to identify the most promising directions for future development by industry.

As this activity proceeds, SRC will utilize the appropriate segments of its infrastructure to support NERC as it assists industry in this new activity.

SRC over the years has emphasized its commitment to maintain and develop world-class university research expertise. The foundation of SRC's (SRC Core research, MARCO, NERC) research sponsorship is a merit-based competitive process.

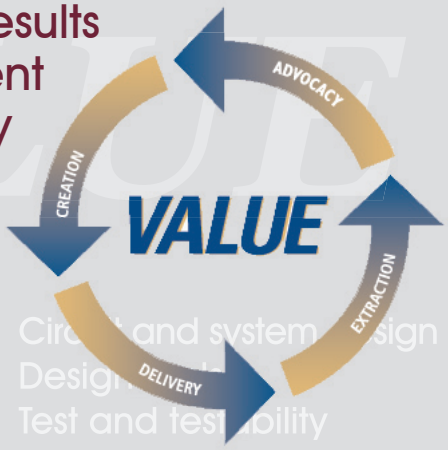
What has been the impact? First, our members consistently tell us the research is relevant and well-executed. Beyond that, we can examine the impact of a research publication as measured by the extent to which the paper is cited in professional journals. Additionally, the number of citations in industry publications can be a measure of their importance to the industry. An additional measure of research impact is the citation lifetime – number of citations vs. time.

In each of these areas, SRC-sponsored research appears to have an impressive impact. Using the database "Science Citation Index Expanded™," we are pleased to see many papers receiving over 100 citations. The largest number received so far for SRC papers is over 750! The lifetime of several of the papers is phenomenal. For instance, for one paper published in 1991, the citations have increased from two in 1991 to 33 in 2004 (total 283). For another, published in 1987, the number has grown from one to seventy-one in 2004 (total 754). Further, the citations of SRC research in industry publications ranges from 3% to 44% for 15 of the most influential publications. Examples of such papers are listed on page 7.

In summary, the impact of SRC's broad research program has been quite high, based not only upon member feedback, but also on the citation metrics approach described above. The SRC's research management methodology, deeply rooted in seeking the highest quality research, relevant to industry's needs, has worked well.

2004 in Perspective

Research Results
Relevantly Educated Talent
Integrated University Research Capability
Networking



In 2004 SRC continued to build on its 22-year legacy of laying a foundation for semiconductor advances manifested in Moore's Law. The industry has invested more than $629 million through SRC, and nearly 3,300 scientists and engineers have received advanced degrees from SRC-supported programs.

The marketplace and the complexion of the industry continue their rapid changes, presenting ever-greater global challenges to maintain critical research and to maintain SRC's reputation as a preferred sponsor of university research. Through the combined efforts of the Board of Directors, our various technical advisory boards, and SRC staff, the research strategy and operational plans are continually refined to maximize value to our members. To this end, SRC has continued aggressive efforts in executing and advancing its comprehensive Value Proposition. SRC's Value Proposition emphasizes all four dimensions of value: Creation, Delivery, Extraction, and Advocacy/Enhancement. This short report can only highlight some of the key accomplishments, major initiatives, and major events that took place in 2004.

Creation

Member company representatives constitute 15 SRC Science Area Technical Advisory Boards (TTAB) which develop needs statements and then evaluate and select programs proposed by the researchers in response to the industry needs statements. There were 143 new research projects started in the core portfolio that includes more than 350 projects spanning the full spectrum of semiconductor technologies, including circuit and system design; design tools; test and testability; advanced device technology; materials and processes; packaging and interconnect; advanced patterning; mixed signal/analog technologies; metrology; environmental safety and health; and modeling and simulation. SRC provides opportunities for member companies to participate directly in the management of the research consortium processes through the Industry Assignee Program; currently five industry assignees are participating in the program.

In addition to 17 research reviews and 17 advisory board meetings, the Graduate Fellowship Program Conference was held in San Francisco in September. It not only provided opportunities for networking, but also served to deliver the latest research results from top students. Dr. Sunlin Chou, Intel Senior Vice President and General Manager, Technology and Manufacturing Group, delivered the GFP banquet keynote address. Dr. James Comfort, IBM Vice President, Systems and Technology Group, and an alumnus of the Graduate Fellowship Program, spoke at the Awards Luncheon. The conference presented sixteen invited papers from SRC Fellows, 49 posters, and three Outstanding Research Presentation Awards.

In order to deliver relevantly-educated talent, SRC continued to enhance student programs, including a doubling of the TechConnect opportunities for recruiting and networking in its core program and in the MARCO subsidiary. In addition, the SRC Education Alliance, another SRC subsidiary, expanded its program, addressing the industry need to develop undergraduate talent. The SRC community continued to hire more than 70% of the

graduating students with their intimate knowledge of the latest technology. Read more about SRC's student programs on page 25.

The number of universities conducting research supported by SRC reached ninety-four, including a record twenty-three universities outside the United States. Three professors were awarded the SRC Technical Excellence Award by our member companies in recognition of outstanding contributions to the field of semiconductor electronics. Read about SRC award winners on pages 26 and 27.

The Faculty Recognition Award for Student Recruiting was created in 2004 to recognize and reward principal investigators who are most successful in recruiting native-born or naturalized students. The program also serves to highlight this challenge. Professors Mark Law and Kevin Jones from the University of Florida received the award in August, and Professor William Oldham from the University of California at Berkeley received it in November.

SRC added twenty patents to its intellectual property portfolio (which currently includes 233 SRC-issued patents) in 2004 (see page 28); SRC members have royalty-free licenses to these patents.

At the 2004 Design Automation Conference, 45 of 55 technical sessions included SRC involvement via contracts and/or grants to the research professors and students.

In addition, MARCO, an SRC subsidiary, has five Focus Centers (see page 20) conducting complementary research projects.

Delivery

In order to facilitate delivery of research results to member company engineers, SRC extended the Technology Transfer e-Workshops series to provide real-time lectures and interaction with professors on topics selected by the members. After a successful pilot in 2003, SRC held 13 e-Workshops in 2004 with a 97% satisfaction rating, including a set of five e-Workshops that were customized for an international member. The Internet-based meetings and the audio are archived for convenient referral.

Table of Contents

In addition, SRC sponsored several workshops and special meetings during 2004, including:

- A series of international mini-workshops on "An Assessment of Options for Post-CMOS Information Industry."
- SRC Forum on Non-Volatile Memories (co-sponsored with Stanford University)
- SRC/NASA Ames Workshop on Novel Materials and Assembly Methods for Extending Charge-based Technologies and Beyond (co-sponsored with NASA Ames Research Center)
- Silicon Nanoelectronics and Beyond II Workshop (co-sponsored with the National Science Foundation)

The year saw an increased use of the acclaimed SRC Web site. The expanded and enhanced suite of SRC sites houses a library of more than 14,000 publications, including approximately 2,000 added in 2004, along with information about patents and software to which the members have royalty-free access. SRC event registration is now online, and the white paper submission and review processes are also Web-enabled.

Five industrial assignees were also at SRC in 2004, to support management of the SRC research portfolio and to provide real-time access to the latest developments for their respective companies.

Extraction

In order to assist all of the members with maximizing the value from SRC, SRC continually collects and shares benchmark practices via the Benchmark Practice Handbook on the SRC Web site. Participation metrics are also provided quarterly in order to help member company representatives monitor participation in key meetings.

The members assigned 560 Industrial Liaisons to interface with the researchers in order to help provide insight to industry issues, to transfer technology back to their member companies, to offer industry support, and to provide mentoring to prepare students for rewarding careers in the industry.

Approximately 400 member representatives participated in various advisory board meetings to set research budgets and research agendas, to both select and review research programs, and to meet with professors and students.

Advocacy/Enhancement

The Executive Technical Advisory Board representatives annually review the research output, and in 2004, they individually identified more than 100 "nuggets" of compelling research. A few quotes from member companies are listed below:

CADTS
Clock Network Synthesis for High Performance, Low Power and Reliable IC Designs

"A new clock network synthesis technology is being developed as required for high chip complexity in hierarchical/SoC designs. Experimental results on benchmark circuits showed that about a 50% clock net wirelength reduction can be obtained through a simple, yet effective method using intentional skew routing and clock buffer blockage avoidance."

CADTS: Test
Reduction of Test Application Time and Test Data Volume

"... used the Scan Architecture concepts to significantly reduce tester time on a number of parts. The partially parallel and partially serial architecture allows for much improved data volume throughput, which translates to improved tester throughput, which translates to lower test costs."

CADTS: Physical Design
Synthesis for Analog Intellectual Property: Generalized Analog Circuit Synthesis.

"ACS, the ... cell-level analog synthesis framework that can size and bias a given circuit topology subject to a set of performance objectives and a manufacturing process, is a direct result of SRC funding. Analog cell design is currently a simulation-intensive manual process even for expert designers. ACS will help automate this part of the design and significantly boost designer productivity."

DS: Compact Modeling
Measurement and Modeling of Low Frequency Noise Sources in Advanced Bipolar Technologies

"Provides insight into the complex relationships between experimental noise characteristics of advanced BiCMOS transistors and the physics and technology of respective devices. Based on the improved understanding resulted from this research, existing processes can be further fine-tuned or redesigned towards superior noise performance."

DS: Digital CMOS
Strained Silicon MOSFETs with Silicon-Germanium Source/Drain Junctions--An Alternative Path to Strain Engineering in Nano-Scale MOSFETs

"This research continues the study of the recessed strained silicon germanium source/drain junctions (developed in the FEP Research Center) and the resulting strain in the channel. Implications of this research will be significant through at least the 32 nm node."

ICSS
System-On-Chip for Power-Aware Wireless Communications

"[This research] is particularly returning new methods in fault tolerant process-compensating architectures for scaled architectures, software power management algorithms, and a variety of other projects. The stature of this work was recently validated by the fact that several hundred designers from our member companies participated in and responded positively to an on-line workshop."

IPS
Fast and Accurate Electromagnetic Modeling Methodologies and Algorithms for SoC and SiP Design

"The fast, robust finite element solver for packages and interconnect structure electrical model generation was completed and through contract meetings held at the university, it's effectiveness demonstrated and the software source was transferred to [our company]. Testing of the program for predicting package resonance effects has been demonstrated here and presented in a program review. Further work is planned to incorporate the program into an internal tool set for package full wave electrical analysis. This is an excellent example of an efficient

SRC supported development effort resulting in timely technology transfer to industry."

IPS: BEP
Plasma Etching of High-κ Dielectric Materials

"This research is focused on methods to etch high-κ gate dielectrics and subsequently clean the silicon substrate to prevent boron contamination. Selectivity studies showed that the best selectivity of high-κ-to-silicon is for a pure BCl_3 plasma. This leads to residual boron, which can be removed with an Ar/H_2 plasma treatment. The cleaning effectiveness is highly dependent on chamber conditions and thus a chamber clean process was developed to maximize boron removal. This work should be of benefit as high-κ dielectrics are integrated into our advanced devices. The real-world solutions in this research will definitely find use in industry."

IPS: Packaging
Electrical Modeling and Simulation

"Over a long period of time, this program has developed numerous and effective software codes for the modeling and simulation of packages and interconnects. We have incorporated many of these software programs into our internal software tool set for modeling package layouts and delivering accurate SPICE simulation files to our internal and external customers."

NMS: ESH
Environmentally Benign Semiconductor Manufacturing

"New work in addressing potential ESH issues with nanotechnology is critical to understanding the potential impacts as nanotechnology research evolves."

NMS: Patterning
A Mesoscale Simulation Of The Lithographic Process

" The task continues to address comprehensive understanding of the role of resist components on pattern quality, with an emphasis on resist line edge roughness (LER). One highlight of this year's collaboration was the demonstration that adding base improves LER by increasing the gradient in photoacid concentration at the pattern edge. Mesoscale simulation models and software have made significant progress this year."

In summary, although 2004 was a very challenging year, our value proposition continued to satisfy the members, as evidenced in the above quotes and in the positive responses to the annual member satisfaction survey that addresses all four dimensions of SRC's comprehensive Value Proposition.

Impact of SRC-guided Research

The eleven papers below, all written by SRC researchers, have each been cited more than 100 times. Papers cited as often as these are rare in scientific literature, and a few approach or exceed the number of citations given to papers of Nobel Laureates.

1. "Point Defects and Dopant Diffusion in Silicon" by Plummer et al. (1989) Stanford
542 citations, 200 citations by industry (37%)

2. "Asymptotic Waveform Evaluation for Timing Analysis" by Pillage and Rohrer (1990) UT/Austin
283 citations, 101 citations by industry (36%)

3. "Ferroelectric Materials for 64 Mb and 256 Mb DRAM" by Parker and Tasch (1990) UT/Austin
164 citations, 44 citations by industry (27%)

4. "Alternative Dielectrics to Silicon Dioxide For Memory and Logic Devices" by Kingon et al. (2000) NCSU
222 citations, 50 citations by industry (23%)

5. "Hole Injection SiO2 Breakdown Model For Very Low Voltage Lifetime Extrapolation," by Schuegraff and Hu (1994) Berkeley
147 citations, 64 citations by industry (44%)

6. "Large-Scale CVD Synthesis of Single-Walled Carbon Nanotubes," Dai et al. (1999) Stanford
179 citations, 19 citations by industry (11%)

7. "Switching Devices Based on Interlocked Molecules" by JR Heath et al. (2001) UCLA
175 citations, 6 citations by industry (3%)

8. "BSIM - Berkeley Short-Channel IGFET Model for MOS-Transistors" by Sheu et al. (1987) Berkeley
124 citations, 41 citations by industry (33%)

9. "Plasma-Enhanced Chemical Vapor-Deposition – Differences Between Direct and Remote Plasma Excitations" by Lucovsky and Tsu (1987) NCSU
122 citations, 13 citations by industry (11%)

10. "Importance of Space-Charge Effects in Resonant Tunneling Devices" Lundstrom et al. (1987)
103 citations, 17 citations by industry (17%)

11. "Threshold Voltage Model for Deep-Submicrometer MOSFETs" by Hu et al. (1993) Berkeley
105 citations, 38 citations by industry (36%)

Innovate We Must

The overarching mission of the SRC Core Research Program is to conduct timely technology and design research that will better enable its semiconductor member companies to develop innovative, competitive new technologies and products. Research sustaining exponential progress towards ultimate CMOS will be the key enabler in this mission.

Ultimate CMOS is an aggressive mandate since it is believed that gate lengths for ultimate CMOS will probably be less than ten nanometers (nm) and that the changes in the CMOS technologies required to achieve this goal are likely to be unprecedented. We are already working to introduce new structures, materials, and processes to ensure that the severely scaled CMOS transistors can provide acceptable performance benefits. In addition, the copper/low-dielectric-constant interconnect systems for integrated circuits are becoming consumers of a substantial fraction of chip power while at the same time suffering from deleterious performance effects under scaling. Challenges abound also in the processing area; probably the most challenging of which is related to the absence of lithographic tools to support volume manufacturing in the far-sub-nanometer regime. Formidable challenges also extend to design technology due to the complexity of rapidly designing an integrated circuit whose transistors are far from ideal and whose parameters are not sensibly constant across the chip. Moreover, designers must increasingly focus on the minimization of chip power consumption to manage heat transport from the chip while at the same time attaining high performance. Finally, the design of integrated circuits whose operation requires the utilization of several different types of signals is increasingly important and challenging due to isolation and integration issues as well as the lack of design tools that can support integrated design and test in different signal domains.

We briefly describe selected 2004 accomplishments in view of these challenges in the following sections. Some of these challenges may not be amenable to solution via extrapolative thinking and thus we are encouraging SRC researchers to think out-of-box in their search for solutions. As a general rule, SRC research today is focused at and beyond the 22 nm ITRS 2004 node since we are confident that leading-edge industry research and development is forging pathways to this node.

In 2004, SRC continued its tradition of partnering with SEMATECH and various government institutions in support of its research. Specifically we have worked with NSF in support of environmentally benign semiconductor manufacturing, in the mixed-signal area, and in launching a new research program in factory operations. One of the exciting new venues with NSF is the *Silicon Nanoelectronics and Beyond* program that has been included as a theme in the NSF Nanoscience and Engineering (NSE) solicitation. SRC is committed to a substantial role in the proposal review process via the provision of industry reviewer nominees and will seek to include those programs funded by NSF as an integral part of the SRC research process, including participation in reviews and utilization of SRC technology transfer processes. We are pleased to acknowledge a partnership with the State of New York in the implementation of a new program in interconnect science and technology and in its continuing support with SRC for research in microelectronics design.

Device Sciences

The goal of Device Sciences was to advance the science and technology base required to sustain the exponential progress towards achieving the ultimate CMOS technology. Needed changes in the CMOS technologies will require highly advanced device structures incorporating many new materials integrated, for example, in the gate and channel regions of the MOS transistors. Device Sciences research supports the industry in its efforts to introduce these new structures, materials and processes to ensure that the severely scaled CMOS transistors can provide acceptable performance gains.

The required technology changes are impacting design methodologies and design tools to the extent of managing power dissipation through reduction of gate leakage current and short channel effects and through engineering the channel electrostatics. New high speed, accurate compact models incorporating predictive capabilities for design in advanced technology nodes are being developed. Compact models are also being developed for double-gate and multiple-gate MOSFETs to support such options for member companies who expect to introduce these new structures in the 32 or 22 nm nodes.

Device Sciences made important contributions in 2004 to compact models, materials technologies, and modeling and simulation tools required to extend CMOS to and beyond the 22 nm node. Compact modeling research has three component directions. The first is extending the industry standard compact model, BSIM, to support accurate simulation in high frequency applications. The second direction is to substantially improve and update the computational engine of compact models to improve accuracy and simulation speed for the advanced technology nodes. The final direction is to provide accurate, fast new models to simulate double- and multiple-gate MOSFET structures. Two updated and two new compact models were released. One of the updated models is the conventional threshold voltage-based model, BSIM 4.4, which was improved to address trap-assisted tunneling and recombination current that occurs at a reverse biased P-N junction when the doping on both sides of the junction is relatively high due to the halo-doping technology. The second updated model is BSIM-SOI 3.2 that adds a framework for partially- and fully-depleted SOI devices and features to more accurately model RF devices. A new model released is BSIM 5.0.0, featuring a new computational engine, "surface potential plus" (SPP). This model addresses the needs of nano-CMOS technology and RF high-speed CMOS circuit simulation with smooth and continuous I-V and C-V equations, and is an improvement over the conventional threshold voltage-based simulator. The new formulation allows extension of the model to non-classical devices like ultra-thin-body, and multi-gate MOSFETs. The second new compact model released was the alpha version of BSIMDG 1.0, which is a new member in the BSIM family developed for the double-gate MOSFET.

Additional device-related contributions include transfer of FinFET technology to SEMATECH and to an SRC member company, growth of SiGe selectively into raised source-drain regions to further lower parasitic resistance, and the subsequent transfer of this technology to several member companies. Also, the 3-D Monte Carlo device simulator, MoCa, developed over the last several years has been licensed and transferred to a former member company and is currently being commercialized.

Device Sciences also had important achievements in 2004 related to a new gate stack technology aimed at greatly decreasing gate leakage current at and beyond the 45 nm ITRS 2004 technology node. First and foremost, the high-κ gate dielectric emerging as the industry choice for reaching an effective oxide thickness (EOT) of 0.7 nm for the 45 nm node is HfO_2, HfSiON or a related derivative. These materials were first identified as attractive candidates several years ago in the SRC/SEMATECH Front End Processing Research Center, which is now in the last year of its eight-year effort and now referred to as the SRC/SEMATECH Front End Processing Transition Center (FEP-TC). A layered gate stack structure consisting of HfO_2 on Si capped with a top layer of HfSiON was shown to improve the thermal stability of the gate stack together with sustaining high channel mobility in the underlying silicon.

The FEP-TC completed a shift to the longer-term goal of identifying and developing higher permittivity dielectrics for EOT < 0.5 nm. Dielectrics such as lanthanum oxides, lanthanum aluminates, $HfxTi(1-x)O_2$ and $HfSrO_3$ are being studied. Collaboration with two member companies has led to < 0.02 nm interfacial oxide with thick molecular beam deposited $LaAlO_3$ in which no substrate reaction was found, but recrystallization was observed above 900°C (Figure 1).

The FEP-TC also discovered that charge trapping is a more severe reliability problem in high-κ gate dielectrics than time dependent dielectric breakdown

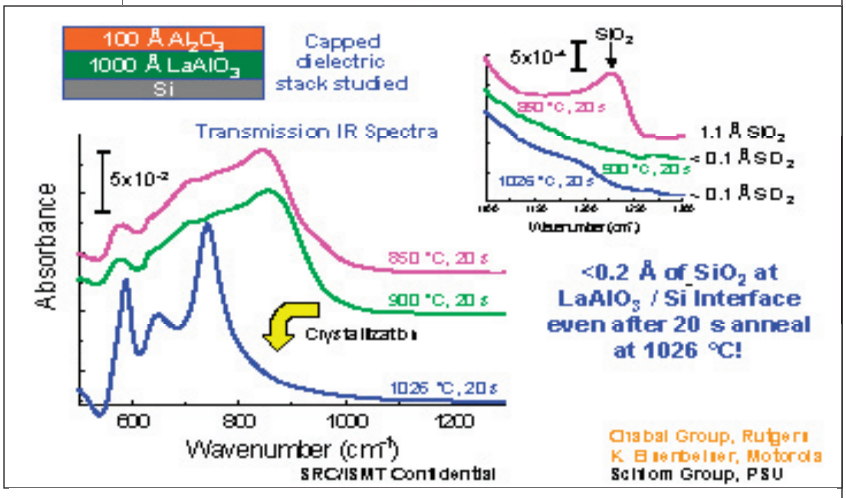


Figure 1. Thermal stability of amorphous LaAlO3 on Si

(TDDB) and developed a new charge pumping method to separate interface traps from bulk traps in a high-κ dielectric deposited on silicon. Finally, the Center furthered scientific understanding of low φ_m (metallic work function) and high φ_m metal gate electrodes deposited on high-κ gate dielectrics.

Nanomanufacturing Sciences

Nanomanufacturing Sciences (NMS) launched and leveraged several innovative and high potential impact programs that address and anticipate emerging strategic member research needs. Key programmatic highlights include:

• Launched a new joint SRC/DARPA Advanced Lithography Research Network and aligned this effort with DARPA's multi-year BAA-042 for maskless lithography;

• Launched the three year, joint SRC/NSF/SEMATECH FORCe II program;

• Established a focused multi-project endeavor on directed self-assembly to address specific patterning challenges, such as line edge roughness and dimensional control;

• Initiated strategic alignment between NMS and the Silicon Nanoelectronics and Beyond (SNB) working group on Novel Materials and Assembly Methods for Extending Charge Based Technology to its Ultimate Limits and engaged one 2004 SNB center, the NSF Nanoscale Science and Engineering Center at the Univ. of Wisconsin in Templated Synthesis and Assembly at the Nanoscale;

• Joined the following relevant and highly leveraged initiatives:

- Univ. of Wisconsin-Madison NSF Materials Research Science and Engineering Center (MRSEC) in Nanostructured Materials and Interfaces; the NSF Nanoscale Science and Engineering Center (NSEC) in Templated Synthesis and Assembly at the Nanoscale, the Center for NanoTechnology (CNTech); and the NSF Synchrotron Radiation Center (SRC). This cooperative agreement will expose our members to ~26 new faculty research programs and leverage a multi-year National Nanotechnology Initiative (NNI) award;

- Silicon Wafer Engineering & Defect Science Center (SiWEDs), a defect and contamination related initiative.

Patterning

The NMS Patterning thrust supports innovative research that addresses six strategic nanomanufacturing centric challenges: 1) Directed assembly research which targets specific imaging materials issues, such as line-edge roughness (LER), dimensional control, linearity, and resolution, and the direct patterning of electronically useful materials; 2) Robust sub-10 nm metrology tools; 3) Radical approaches to affordable and low variability post-NGL (Next Generation Lithography) patterning; 4) Low-volume patterning options; 5) Extensibility, limits, and cost of NGL; 6) Design for patterning, concurrent design, and defect tolerance.

With exponentially rising exposure tool and mask set costs, discovery and innovation are needed to extend the feasibility and affordability of optical patterning options into the deep nanometer domain. For more than a decade, SRC has supported seed research projects that explore new families of imaging materials as well as novel approaches to and useful applications of directed self-assembly. Researchers at the Univ. of Wisconsin-Madison demonstrated near perfect epitaxial assembly of block copolymer films over arbitrarily large areas. An early example (Figure 2b) is shown, which shows long-range order in a phase segregating diblock copolymer film on a templated substrate, versus the corresponding random spaghetti-like strings of symmetric poly (styrene-b-methylmethacrylate) on a bare substrate (Figure 2a).

In July 2004, the team at the University of

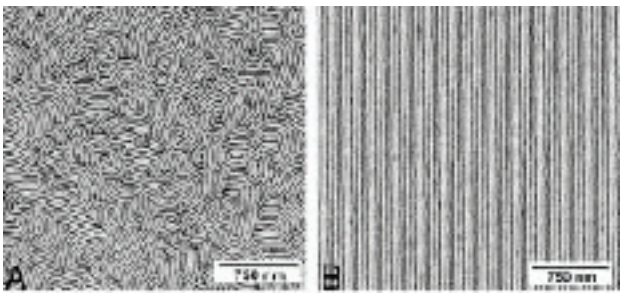


Figure 2. Phase segregated film of symmetric poly (styrene-b-methylmethacrylate), Lo~48 nm, on: a) an unpatterned surface and b) a patterned surface, for which Ls=Lo. The long-range homogeneous ordering in image B was achieved by lithographically templated self-assembly.

Wisconsin-Madison demonstrated the feasibility of combining top-down lithography with bottom-up self-assembly to pattern a desired heterogeneous structure. An L-shaped surface template (Figure 3b), was lithographically patterned into an activated self-assembled monolayer. Subsequently, a 60 nm block copolymer film was deposited and annealed to achieve phase segregated L-shaped patterns, with period of ~49 nm (Figure 3a).

In principle, it should be possible to pattern any shape that appears in the spaghetti-like array of lines that appear in the unpatterned block copolymer film (Figure 2a). Other results (C. Ross and A. Belcher of MIT, presented at the SRC/NASA Workshop on Novel Materials and Assembly Methods for Extending Charge Based Technology and Beyond) suggest that lithographically or biologically templated self-assembly may enable the patterning of heterogeneous features with sub-lithographic dimensions. These recent accomplishments suggest that directed self-assembly may enable the extensibility of affordable optical patterning to the 10 nm regime.

The Patterning thrust established a Directed Self-Assembly Program with thirteen new projects consisting of eight one-year, high risk, seed projects and five multi-year research tasks. This initiative addresses fundamental materials issues that threaten resist extensibility. It also provides an initial response to the #1 strategic research horizon identified at the 2003 ETAB Summer Study, i.e. directed self-assembly methods to extend digital and analog technologies to their ultimate limits. These novel hybrid [top-down and bottom-up] patterning projects explore how directed self-assembly could reduce line edge roughness and dimensional variability and enable the direct patterning of electronically useful materials. The projected challenges of

Figure 3. (a) Epitaxial assembly of block copolymers in 'L' patterns on (b) chemically nanopatterned substrates. (Nealey, Kim, Solak; Univ. of Wisconsin-Madison; unpublished results.)

LER and dimensional variability require a fundamental understanding of how molecular-level structural elements, local environments, and film dynamics impact measured dimensional and positional variability. A key goal of this research is to establish guiding principles that enable the inverse design of new materials systems and synthetic paths, which are compatible with silicon process technology and enhance line edge planarity, abruptness, resolution, positional control, and pattern transfer throughput.

Figure 4. Piston mirror fabricated for use in arrayed optical maskless patterning technology.

In the area of maskless patterning, researchers at the SRC/DARPA Advanced Lithography Research Network successfully fabricated 3-D double-flexure piston mirror structures for Low Volume Patterning (mirror: 0.5 um - 4 um, without interconnect) (Figure 4).

Researchers at Cornell University continue to develop novel families of resist systems and recently demonstrated solventless patterning of an hot-filament chemical vapor deposition (HFCVD) deposited positive tone e-beam resist using supercritical CO2.

Factory Systems

FORCe I successfully completed five research programs in factory operations and supply chain modeling that were conducted by US and international universities. This resulted in several internships and a number of FORCe students were hired by member companies.

Researchers developed architecture for interfacing the shop floor control software and the FORCe fab scheduler via a data model that also interfaces with the fab's planning system and simulation environment. Guidelines were developed on the use of the scheduler for an event-driven or time-driven shop floor control system. A scheduling testbed has been developed to simulate and test the scheduling algorithms. The new approaches to the simulation

task team favorably compared performance of job-driven simulation with resource-driven simulation methods. This research has led to the initiation of commercialization efforts by SEMATECH.

SRC researchers used optimization to derive preventative maintenance (PM) policies that optimized the PM window based on equipment and process information to improve operational performance. The project developed good maintenance policies that integrate this information, as opposed to the rigid calendar-based or wafer count-driven methods typically used in industry. Outcomes included a PM optimization tool (PMOST) and several internships to implement this approach in member company pilot projects.

The demand data mining project developed disaggregation methodologies and tested them on actual semiconductor data. Results show good improvement over the conventional methods. Demand forecasting algorithms were developed and these techniques are being evaluated by member companies for possible implementation.

A new program in factory operations (FORCe II) was defined and launched for the 2005-2008 period. The program will conduct research on factory operations, process control, and supply chain management. SEMATECH, NSF and SRC are providing support for the new program comprising seven research programs across nine U.S. and international universities.

Environment, Safety, and Health

The NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing remains the primary focus of research in the SRC Environment, Safety, and Heatlh (ESH) research portfolio, and ESH research continues to be an important element of the overall Nanomanufacturing Science area. In 2004, the ESH center was in its ninth year of a 10-year agreement between NSF and SRC. There are four process related thrust areas:

1. In Back-End Processes, the Center has recently emphasized fundamental studies of chemical mechanical polishing (CMP) tribology, fluid effects, and pad properties in the Back-End Processes Thrust. Innovation in this area includes work on new techniques of CMP process end-point detection. For example, modeling of polish motor current has shown promising correlation with evolving wafer topography.

2. In Front-End Processes, the focus is on novel cleaning and surface conditioning as well as the cleaning of new materials such as gate-stacks. One innovative approach involves the use of UV irradiation in ammonia to produce a single layer of silicon nitride on a silicon surface. Other work focuses on cleaning germanium surfaces.

3. Factory Integration focuses significantly on the use reduction of ultra-pure water in the wafer fab. An example of innovation in this area is the development of a sensitive rinse monitoring system that has the potential to dramatically reduce water usage.

4. Patterning research continues on solventless deposition of resists primarily with chemical vapor deposition (CVD) processes. These resists can be conventionally developed, but work has also been done on super-critical CO2 development.

As the Center approaches the end of its NSF funding cycle, SRC members have developed a plan for continuation of the ESH Research Center. The details of the research program for the new center are being developed. Financing may involve co-funding with SEMATECH.

Metrology

SRC established a cross-science area technical advisory board (TAB) in metrology, with representation from the Device, Interconnect and Packaging, and Nanomanufacturing Science Areas. The TAB drafted and posted a common set of emergent nano-characterization research needs that emphasize three research themes of particular interest to our members: dimensionality and defects, intrinsic nanoscale material properties, and electrical characterization. Crosscutting dimensional and defect characterization research needs include:

- dimensional and positional characterization,
- line edge roughness,
- high-resolution surface roughness and sidewall measurement, and
- novel approaches to patterned wafer defect detection for 32 nm and beyond technologies.

Similarly, intrinsic material characterization needs are identified in the following areas:

- ultra thin film characterization,
- stress monitoring,
- 3-D measurement, and
- metallic contamination.

Finally, strategic research in electrical characterization is needed that explores:

- extrinsic and intrinsic nanoscale device properties,
- leakage measurements and interface characterization,
- mobility measurements, and
- reliability imaging.

This document is well-scoped to guide future cross-Science Area support for research on robust sub-10 nm characterization and metrology tools.

Interconnect and Packaging Sciences

Interconnect and Packaging Sciences (IPS) is a new science area launched in 2004. IPS is a broadly based activity with current thrusts in Back-End Processing (BEP) and Packaging. A primary rationale for combining these two activities in one science area is to encourage innovative solutions to address the critical science and technology needs at the interface between these two areas.

IPS accomplishments include both operational and technical activities. One significant honor for IPS was having Jim Meindl selected as the winner of the 2004 Aristotle Award. In the operational arena, IPS has solidified the organizational structure of the unique BEP and Packaging combination. A major operational accomplishment has been the solicitation and final selection of new programs representing approximately 55% of the IPS portfolio. This program renewal has placed special emphasis on opportunities for research scope expansion according to SRC Board of Directors-recommended directions (interconnect technology and materials, power delivery and thermal management, optical interconnect and devices, heterogeneous system integration, interconnect reliability, interconnect exploitive architectures), new concepts, and cross-cut programs.

IPS technical highlights include:

- finalization of two innovative approaches to non-contact signal transmission possibilities for global interconnects
- a patented approach to pore sealing for optimum use of porous low-κ dielectrics
- identification of a unique limitation of nanotubes for global interconnect
- demonstration of an “ion wind” approach to chip cooling.

The work on non-contact signal transmission for global interconnects involves two programs, one using microwave transmission and the other using RF coupling of signals from the chip to conductors in the lid of the package, and return coupling to another part of the chip. Both of these capabilities can be used for intra-chip and inter-chip global interconnects. In the case of microwave interconnect, integrated transmitters, receivers and antennas are placed on a chip. Signals representing clock or data are generated at one location on the chip, and transmitted through the circuit substrate as well as the chip dielectrics and the package, to other locations on the chip. An integrated antenna and receiver are used to restore the data or clock signal for use in this new location. The advantage of this approach is that the signal travels at microwave rates across the chip, rather than being limited by transfer through wires. Signals are either capacitively or inductively coupled from the chip to a waveguide inside the lid of the package. The waveguide then carries the signal to another location where it is coupled back to the chip. The advantage of this novel approach is that the conductors on the lid of the package can be made much thicker than the metallization on the chip, thus providing much faster signal transmission needed for global interconnects. Each of these programs provided hardware demonstrations of their capabilities for use in both intra-chip and inter-chip applications.

Porous dielectrics are the material of choice to replace silicon dioxide as the inter-metal insulator in advanced Cu low-κ metallization schemes. A major problem that has been found with the use of porous dielectrics is the deleterious effects of open pores on the surface and etched edges of these materials. The open pores allow penetration of moisture and other contaminants into the interior pore structure of these materials, causing degradation of dielectric

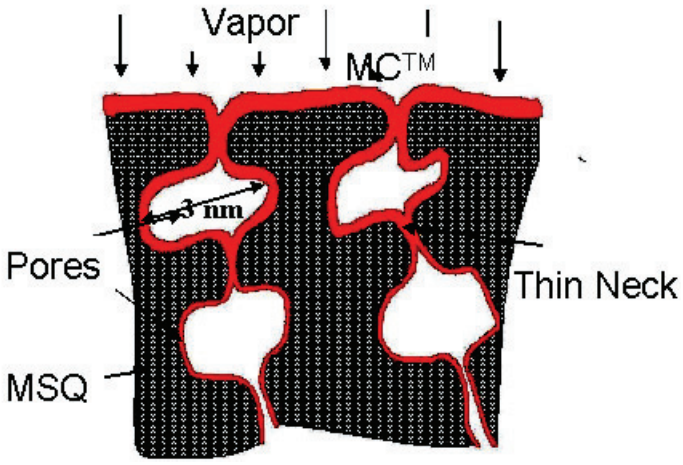


Figure 5. Unique pore sealing process isolates the interior of porous materials from deleterious external environments

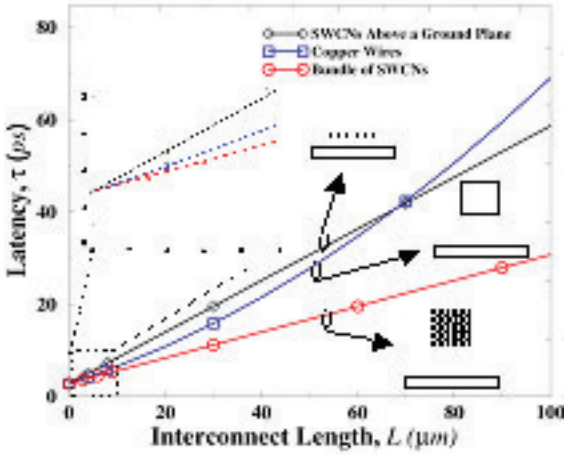


Figure 6. Comparison of the latency of 22 nm node Cu lines, single carbon nanotubes, and bundles of nanotubes as a function of line length. Bundles of nanotubes perform better at all lengths.

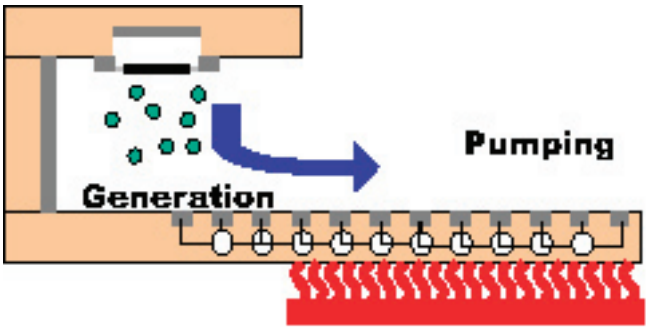


Figure 7. Novel "ion wind" cooling device with possible application to packages or directly to ICs.

properties as well as reliability concerns. IPS researchers have recently produced a unique "pore sealing" process (Figure 5) that allows a protective material to be deposited only on the outside surface of the porous material, thereby isolating the interior of the porous material from deleterious external environmental effects.

Carbon nanotubes have recently been proposed as a possible solution to the global interconnect problem. Carbon nanotube features of high electrical conductivity, high current carrying capacity, and high thermal conductivity have implied availability of many of the properties needed for long on-chip interconnects. Careful studies of the unique conduction mechanisms in carbon nanotubes, and investigation of the implications of such conduction for applications in real circuits, have been carried out by SRC researchers. Using a novel concept of "kinetic inductance," it has been shown that the wave propagation speed in a single carbon nanotube is more than 100 times smaller than previously expected, resulting in predictions that single carbon nanotubes will be no better than copper interconnects for future generations of IC technology. However, it has also been shown that this effect can be minimized by the use of bundles of carbon nanotubes (Figure 6). This innovative work provides key guidance for future research directions regarding the nature of carbon nanotube technology development needed for improving interconnect performance.

Chip cooling has become recognized as one of the major technologies required for continued scaling of ICs. In response to this need, the Packaging Thrust of IPS has initiated several programs to identify and develop unique approaches to cooling and thermal management. One such program uses the radical approach of providing a miniature ion generator and electrically driven "ion wind" to extract heat from surfaces (Figure 7). These "ion wind" heat removal devices are made with standard IC processes and use geometries comparable to IC manufacturing. It is possible that such structures could be placed on a package or directly on the top (or bottom) of ICs to provide coolers intimately connected to the chip. Work on this unique approach to cooling is ongoing. This work has achieved the key goals of demonstrating the ability to generate ions as well as the cooling capability of this process.

Computer-Aided Design and Test Sciences

As the SRC technology areas pursue research to further shrink feature sizes and we approach the limit of scaling, the pressure increases in the areas of design and design tools to extract more performance from this technology. Since the days of manual design, at least in the digital arena, are long over, advances in computer-aided design and test tools must necessarily accompany design innovations. And in addition to continuing to obtain increased performance from the underlying technology, Computer-Aided Design and Test Sciences (CADTS) research also must deal with the additional challenges brought on by scaling: increased variability in a multitude of ways, power limits, verification of functional and other properties, and test for digital and mixed signal circuits. Demand for mobile products and the very short window from development to market also increase the pressure on design and test tools. Increasingly, systems integrate not only mixed technologies, but also various hardware/software combinations and IP cores from multiple sources. These factors all demand advances in design and test tools.

CADTS continued to produce innovations that help SRC member companies. With a significant presence at the Design Automation Conference, the International Conference on Computer-Aided Design, and the International Test Conference, SRC-sponsored researchers reported outstanding work made available earlier to, and in many cases done in collaboration with, SRC member companies. As outlined elsewhere in this report, SRC Technical Excellence Awards and Mahboob Khan Outstanding Mentor Awards all went to CADTS participants in 2004.

Logic and Physical Design

Power analysis and reduction continues to be a focus of design tools at all levels. High-level approaches monitor activity and reduce or turn off power to subsystem blocks. Power grid design tools and clock gating approaches can work together to maintain the power grid integrity in the face of spikes caused by gating. Synthesis techniques at the logic and physical level change library choices, placement, or routing to reduce power. At a lower level of abstraction, SRC researchers have developed tools using simultaneous dual V_t and dual T_{ox} technology to reduce leakage current. Improved leakage-delay trade-off can be obtained with knowledge of state probabilities, leading to the development of specially tailored cell libraries. Simultaneous V_t, T_{ox} and state assignment techniques have shown a nine times leakage reduction over average leakage.

Basic enhancements to placement and routing, in the past thought to have been a "solved problem," have continued as part of innovative SRC research. Investigations into benchmarks showing that existing place/route tools leave much room for improvement have led to new floor-planning tools. A fast, scalable floorplanning technique using recursive bipartitioning achieves a 20% wire length improvement, and a 200 times runtime improvement over existing methods. These benchmarks and tools have been downloaded over 200 times by SRC members and other universities.

In recent years, the CADTS program has seen an increase in projects going beyond digital design into the analog and mixed signal spaces. Mixed signal designs bring with them not only the usual problems with integrating multiple blocks on a chip, but also the interference of digital switching and supply noise, which can degrade analog/RF circuit performance. A new, fully automated, schematic-driven substrate noise coupling analysis tool developed by SRC researchers can be used for analyzing noise coupling to sensitive circuitry in a mixed-signal chip at different stages of design and layout development (Figure 8).

Test

In the increasingly cost-aware environment of analog/mixed signal test, SRC researchers have developed test strategies for enhancing performance and reducing test costs in data converters. Large, expensive testers contribute

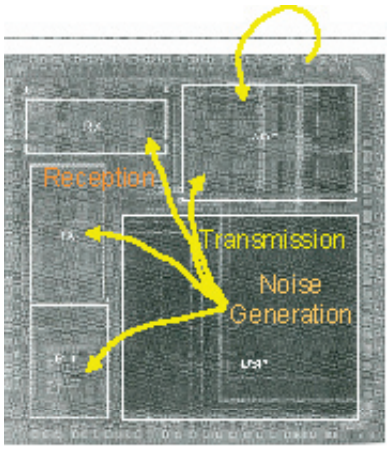


Figure 8. Illustration of on-chip transmission noise coupling.

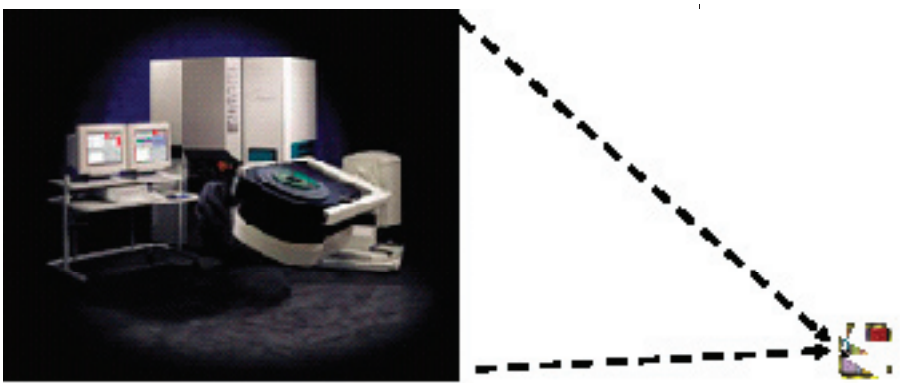


Figure 9. Illustration of the impact on hardware from incorporation of test onto the chip.

to high test cost, but analog/mixed signal BIST approaches to integrate testers on-chip with small tester area have encountered barriers: it is difficult to make precision testers on silicon and to make these testers small. An approach has been developed using imprecise excitation/measurement instruments and redundant information and system identification methods to achieve accurate test, which is test time, hardware, and computation efficient (Figure 9).

Decreased feature sizes and the accompanying increased variability have also had an influence in the test area, increasing the number and types of faults as crosstalk and other effects become significant. Innovations developed by SRC researchers include precise fault models that capture crosstalk effects as aggravated by process variations and manufacturing defects. A prototype framework for test generation and fault simulation was developed that targets crosstalk slowdown effects in the presence of variations and defects, and incorporates weak resistive bridges, capacitive couplings, and crosstalk to accurately capture the logic and timing characteristics of a circuit.

Verification

It has long been a goal of verification research to make formal techniques more widely available without requiring specialized skills. There is increasing emphasis on techniques that combine formal methods and dynamic or simulation-based verification. SRC researchers have been able to achieve orders-of-magnitude reductions in time and space requirements for verification techniques by using automatically generated hints and program analysis techniques. Hints are expressed as constraints on the primary inputs and states of a circuit and can often be found with the help of simple heuristics by someone who understands the circuit well enough to devise simulation stimuli. This research, helping to extend these techniques by automatically generating hints for larger designs, has been incorporated into software tools available to SRC members. It also is an indication of a growing future role for program analysis techniques as the design space increasingly encompasses combined hardware and software systems.

In all areas of CADTS research, there has been a growing interest in extending tools beyond purely digital and processor-oriented techniques into the mixed signal arena. SRC research that is now applying formal verification techniques to analog circuits can help answer system behavior questions not answerable by simulation alone. Beginning with a MATLAB/Simulink model describing continuous transitions of an analog system, this hybrid verification tool constructs a finite-state abstraction with a transition relation based on polyhedral representations of continuous flows, refines the abstraction if necessary, and applies model checking to the resulting transition system. Work in the increasingly important heterogeneous system area includes efforts at hazards-based verification of pipelined circuits and systems (generating a synthesizable VHDL description of a pipeline) and an extension of work in system-level timing verification with automatic abstraction to include continuous variables to support analog and mixed-signal components. Verification is increasingly being extended to non-functional areas, applying formal methods to check power, reliability, and other characteristics of designs.

Integrated Circuit and System Sciences

While SRC process research addresses the manufacturing requirements down to the 22 nm node, the design community is still grappling with the technology at the 45 nm, 65 nm, and even the 90 nm nodes. Each new processing node brings different transistor characteristics that can have huge

impacts on IC design flows. Power has been and continues to be a major issue in design, especially with the proliferation of portable wireless devices. Other issues gaining prominence include both variability and reliability effects that previously were of secondary or tertiary concern. Mitigating these effects at the process level is sometimes not possible so the design community addresses them with novel techniques at both the circuit and system level. On the positive side, designing at the smaller process nodes is the overwhelming abundance of devices. Many member companies are already using digital transistors to implement signal-processing algorithms that improve high-level analog functions. This, however, points to the increasing importance of mixed-signal design and associated tool flows. What we continue to see in the design space is a re-engineering of the design process as device dimensions shrink and this drives the ever-increasing cost of design.

Leading edge design takes advantage of technology scaling to deliver value-added products at cost-effective price points. Innovations within ICSS encompass various sub-categories that bring value to products. Examples are: low-power, decreased sensitivity to variations, integration of analog blocks within digital processes, high-performance, wireless/RF, technology advancement impacts, and hardware/software system design tradeoffs.

Circuit Design

As process technology progresses down to the 22 nm node the leakage of the individual transistors will have a larger and larger role in determining circuit power characteristics. Addressing the fast-arriving leakage problems has been part of the ICSS portfolio for several years and current research takes place on several levels. More generally, portable applications drive the general need for power-aware design methodologies. For example, an SRAM cell-level circuit architecture project has demonstrated a design methodology that reduces leakage power 64% compared to a state-of-the-art low-leakage cell design. Research on a resonant architecture for distribution of the global clock signal has demonstrated a 10 times reduction in jitter and a three times reduction in power when compared to a non-resonant clocking architecture. SRC researchers have also investigated the use of adaptive techniques to control the power consumption at the system level.

Logic/memory styles and design methodologies tolerant to leakage (subthreshold, gate, bond-to-bond tunneling) while maintaining high-performance characteristics, including being robust to variations in process parameters, have been developed. The circuit style and design methodologies are expected to be very useful for technologies beyond 65 nm. Novel circuits and design and test methodologies for multi-bit signaling circuits based on multi-level current and phase-coding representations were developed.

Low-power mixed-signal research is investigating the potential of continuous-time oversampling modulators for digitizing 10 MHz bandwidth signals with a dynamic range of at least 70 dB and is developing new architectures and mixed-signal circuit design techniques to enable the CMOS implementation of those modulators for operation from supply voltages as low as 1.2 V with minimum power dissipation. New techniques and associated power modeling methodologies for reducing power dissipation in the memory hierarchy of high-performance SMP servers have been developed. Knowledge of how to manage microprocessor power and performance through adaptive dynamic control methods at multiple timescales has proved useful in actively controlling system power.

Designers are challenged to design circuits that will function properly given increased variability of scaled technologies. One research project investigates and develops accurate, low-cost mismatch test methodologies and structures to verify the effect, along with the characterization of analog and mixed signal libraries and system blocks specifically accounting for mismatch. New calibration methods for differential and integral non-linearity and gain errors in pipeline analog-to-digital converters have been developed. A new statistical VLSI design methodology has been developed that accounts for both spatial (process-related) and temporal (stress-induced) variation of transistor parameters to achieve higher yield and to better utilize the performance-reliability budget. In support of this research, well-calibrated compact device models (for parameter shifts) have been developed to support the design tools.

As new digital technologies scale, it is important to

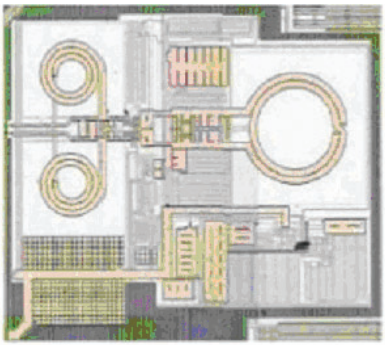


Figure 10. Layout of 4 GHz PLL

integrate analog and RF into these technologies without the cost of added levels in the technology. New low voltage techniques were developed that can be used for the design of noise tolerant phase-locked loops (PLLs) and frequency synthesizers. Self-calibration methods were also developed to tune out process/temperature and voltage variations yielding a robust design. The design target is a 1.2 volt PLL for a 5 GHz wireless LAN application demonstrated in a 0.1 µm CMOS process. The resulting knowledge base of noise tolerant PLL architectures, low-voltage circuit techniques, and self-calibration methods will facilitate IC implementations in CMOS processes beyond 0.1 µm with sub 1 volt operation (Figure 10).

Advances in technologies have two main objectives: to reduce end product costs and to increase performance. Several research programs in the digital area take advantage of the latest technologies to create very high-speed logic while maintaining minimum power. As technologies scale, voltages decrease and leakages increase; both are disadvantages with respect to high-speed digital circuits. Researchers are inventing new forms of logic that will overcome these difficulties and make maximum use of the technology improvements. This year researchers have designed new approaches to high-speed logic including a dual-edge triggered clock storage element that results in a 50% savings in clock power. Researchers have also created novel techniques for improving high speed signaling, and designed novel circuits for clock and data recovery, including techniques for transmitter pre-emphasis, receiver equalization, and far-end crosstalk (FEXT) cancellation to reduce intersymbol interference (ISI) and increase maximum data rates to over 20 GB/s per line pair. Several novel data coding techniques have been developed, including the world's first low-density parity-check convolution code (LDPC-CC) encoder and decoder implemented in FPGAs.

Analog-to-Digital Converters (ADCs) are one of the primary building blocks of advanced wireless circuits and much SRC research has been directed toward design of high-performance ADCs. Researchers have developed a novel digital calibration technique for time-interleaved ADCs in orthogonal frequency division multiplexing (OFDM) systems. New techniques to achieve high-performance ADCs with adaptive calibration have been developed. A novel track-and-hold circuit key to high-performance ADCs has been designed and research to understand and deal with substrate noise has been implemented. Novel techniques for integrating electrostatic discharge (ESD) protection into high-performance wireless circuits with minimal performance impact to gain linearity, and power output have been developed. Researchers have developed a novel RF front-end receiver technology for 24 GHz appropriate for multifunctional communications applications that consumes very little power, is highly compact, very low-cost and high-performance.

At the most advanced CMOS nodes, not all components of a large die are expected to function properly. Several SRC programs at the circuits and systems level are directed towards design with unreliable components. With the availability of several millions of transistors on one circuit, the numbers of I/Os are expected to drastically increase as well. This presents a problem for making a package with enough pins to get all the signals off and onto the chip. A novel technique has been developed that can significantly reduce the area of each package pin by capacitive coupling all of the signal pins. This technique has been proven in silicon and works well for both very fast and very slow signals.

Integrated Systems Design

In the Systems Design thrust, research that encompasses a system's IC hardware and software can make a large impact on overall design efficiency. Maintaining user satisfaction for wireless multimedia applications can depend on the application constraints, service requirements, channel conditions, and available networks. Thus, design optimality in the global sense depends on being able to adapt to different conditions and this can be done with hardware, software, or a combination of the two. One project addresses this problem by showing that reconfiguration of both hardware and software for an image server can reduce the maximum

server-side latency by 77% under heavy loading conditions. Another part of the same project addresses the problem of dynamically reconfiguring an image stream with out-of-order frame buffering so that image quality is not degraded as distortion changes the channel characteristics. This technique relies on a new method that is 3000 times faster than the standard approach to accurately estimate the image distortion in real time.

Other projects in this thrust address aspects of improving design efficiency. The use of CPU cores within embedded applications is well known but optimizing the overall design for different applications (called re-targeting or re-use) may require modifying the CPU's micro-architecture, including the instruction set. Thus, modeling the CPU's behavior in the overall system by back-annotating performance metrics of lower-level models to higher-level models is the theme behind another project, which uses the Xscale and StrongARM micro-architectures as demonstration vehicles. While work in this area is still in the early stages, progress made here can have a substantial impact by increasing system-level performance and decreasing time-to-market.

Cross-Disciplinary Semiconductor Research

One of SRC's missions is to provide strategic vision for the possible scenarios of both technology and application developments in the semiconductor industry in the longer term (i.e., 15 years from today). As part of this effort, SRC launches exploratory research targeting long-term applications and technologies through its Cross-Disciplinary Semiconductor Research (CSR) seed grant program. In 2004, the CSR research emphases were novel memory technologies, heat removal, self-organization for nanofabrication, and nanoscale systems.

Novel memory technologies is a very important topic for semiconductor industry because of new expanding markets for advanced memory devices, especially non-volatile memories. For example, the invention of electrically accessible non-volatile memory with high speed and high density could revolutionize computer architectures. The development of novel memory technologies may require completely new approaches to representing binary states. New concepts, such as non-volatile memory based on ferroelectric nano-crystal assemblies, a Mott-transition memory, and spin-based memory, are being explored.

Thermal management will be the one of the most fundamental priorities for nanoelectonics. Therefore, the studies of the thermal properties at the nanoscale have important implications for the future nanoelectronic systems. There are three important questions to be answered: (1) How can we better remove heat and what are the fundamental limits of heat removal? (2) How can we isolate selected materials subsystems from thermal noise? (3) Are there ways to efficiently control heat flow (e.g. phonon movement) by external stimuli such as electric or magnetic field, light etc.? The possibility for such control would lead to new solutions for heat removal and might result in methodologies for the co-design of electric and thermal circuits. CSR projects on novel phonon engineering concepts for heat removal from nanoscale devices and 3d integrated circuits and opto-therminonic refrigeration for microchip-cooling are exploring entirely different and novel approaches to heat management.

Self-organization of matter in complex structures may provide an alternative way for manufacturing at nanoscale. The building of non-living mechanisms, e.g. electronic or mechanical devices, by emulating biological processes would be a great achievement and could lead to a revolution in device fabrication. For example, the CSR research project on new strategies in self- and directed assembly is exploring the potential of self-assembling methods for nanoscale manufacturing. Today it is not clear that these methods can offer support for practical manufacturing, i.e., achieve minimum feature sizes, achieve overall complexity of the materials system, control manufacturing defects, etc. The grand question is, "Can we encourage matter to assemble in a structure we want?" The key task is to find the information sources and channels to convey the assembly instructions.

An important part of CSR exploratory research in 2004 was focused on nanoscale systems. Research included tasks on heterogeneous integration of post-CMOS technologies with CMOS circuits, design for variability and fault tolerance to address the need to manage increasing on-chip variability of device parameters and increasing operational errors.

FCRP Participating Universities

GSRC
UC/BERKELEY
Carnegie Mellon University
Massachusetts Institute of Technology
Pennsylvania State University
Princeton University
Purdue University
Stanford University
UCLA
UC/San Diego
UC/Santa Barbara
UC/Santa Cruz
University of Michigan
University of Texas at Austin
University of Wisconsin

C2S2
CARNEGIE MELLON UNIVERSITY
Columbia University
Cornell University
Massachusetts Institute of Technology
Princeton University
Stanford University
UC/Berkeley
University of Illinois at Urbana-Champaign
University of Michigan
University of Washington

IFC
GEORGIA INSTITUTE OF TECHNOLOGY
Carnegie Mellon University
Cornell University
Massachusetts Institute of Technology
North Carolina State University
Stanford University
SUNY Albany
Rensselaer Polytechnic Institute
UC/Berkeley
UC/Santa Barbara
University of Central Florida
University of Texas at Austin

MSD
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
California Institute of Technology
Cornell University
North Carolina State University
Pennsylvania State University
Princeton University
Purdue University
Stanford University
SUNY Albany
UC/Berkeley
UCLA
UC/Santa Barbara
University of Florida
University of Texas at Austin
University of Virginia

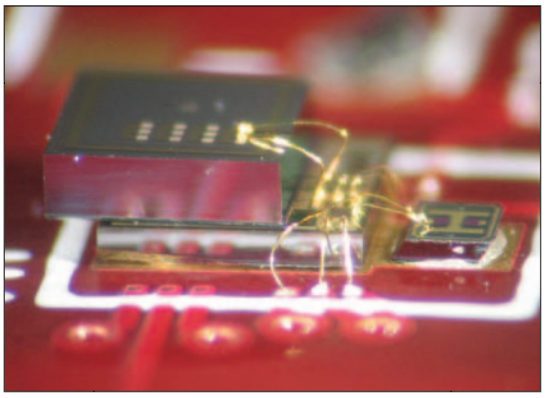
FENA
UCLA
Arizona State University
California Institute of Technology
Massachusetts Institute of Technology
North Carolina State University
Stanford University
SUNY Stony Brook
UC/Berkeley
UC/Santa Barbara
UC/Riverside
University of Minnesota
University of Southern California

The Microelectronics Advanced Research Corporation (MARCO) funds and operates five university-based research centers in microelectronics technology. Its charter initiative, the Focus Center Research Program (FCRP), is designed to expand pre-competitive, cooperative, long-range applied microelectronics research at U.S. universities in those technical areas that are critical to maintaining industry growth within the U.S.

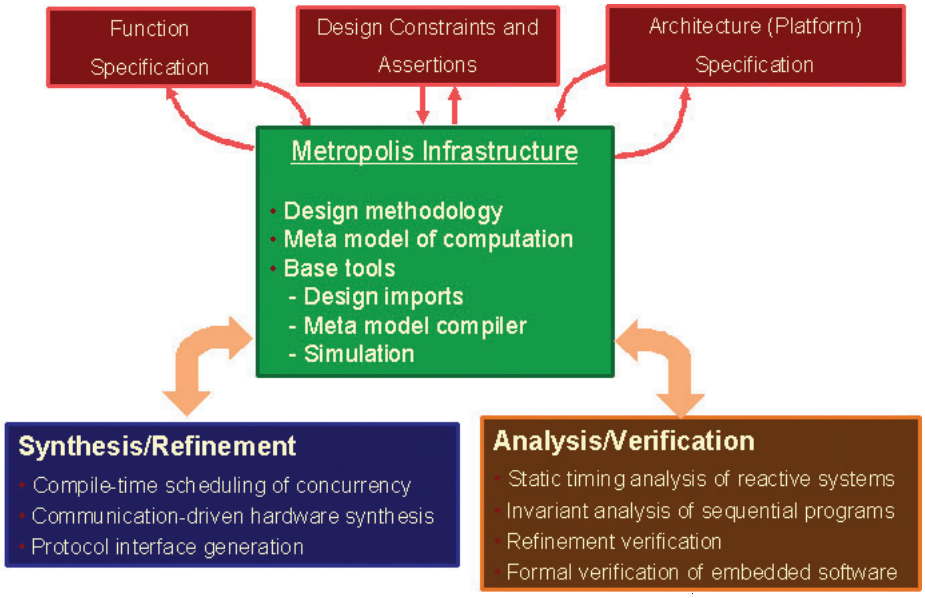
GSRC

The University of California at Berkeley is the lead university for this focus center, the Gigascale Systems Research Center (GSRC), with Professor Jan Rabaey as the center's director. The center's research agenda focuses on pertinent problems the semiconductor industry faces in the next decade in the areas of system design, integration, test and verification. To sustain current growth, the industry requires orders of magnitude of improvement in energy efficiency, cost, reliability and time-to-market.

To address the multiple challenges within this focus, the center is structured along eight interlocking research themes, each led by a theme leader. The horizontal themes, Heterogeneous System Design & Integration and Soft Systems, represent two visions on how integrated systems are to be realized. These horizontal themes are combined with four vertical ones, each of which addresses one particular aspect of embedded integrated system design. The



GSRC developed the world's smallest functioning radio.



Metropolis, a major advance in system design

Power-Aware Systems, Reliable Systems, System Verification and Embedded Self-Test themes, respectively, address the power and energy, reliability, verification and test roadblocks that are looming on the horizon. Finally, the System-Level Living Roadmap provides an environment to explore how the different cost metrics of design will evolve in the next decade, taking a system-level view. This high-level perspective is unique and complements and builds on top of the existing roadmapping efforts. This effort, which encompasses and integrates all the research activities of the center, is essential in identifying emerging challenges and in steering the research evolution of the center.

GSRC's 2004 Research Highlights

• Metropolis, a major advance in System Design: Released version 1.0 of Metropolis, a trail blazing tool suite for heterogeneous system design. DARPA and various companies including Intel, Cypress, and GM, are now working with GSRC to further development.

• New technology to improve power conservation in semiconductor designs through development of the Razor tool suite which identifies and removes non-essential process, temperature, and safety margins, resulting in significant power conservation.

• Validated the center's heterogeneous, power and reliability initiatives by deploying them to develop the world's smallest functional radio.

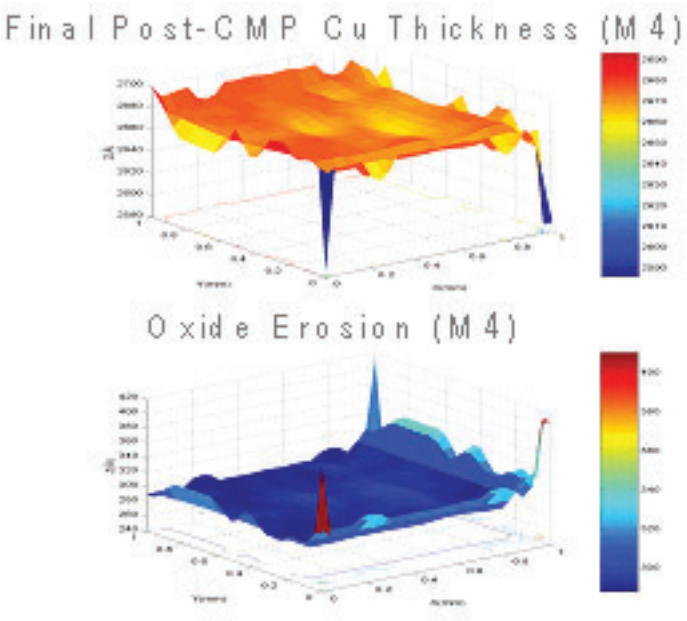
C2S2

The Focus Center for Circuits and Systems Solutions (C2S2) is led by Carnegie Mellon University. Professor Rob Rutenbar is the director. The center aims to develop new circuit design techniques needed to convert novel devices into robust performance across the most diverse range of applications.

Relentless scaling of semiconductor devices toward fundamental physical limits threatens to make obsolete today's most basic circuit design assumptions. Today's landscape of familiar trade-offs (area, speed, power, frequency, noise, reliability, linearity, yield, cost) is shifting radically. To build tomorrow's complex, integrated, heterogeneous systems, the industry requires a foundation of circuit designs it can trust.

Circuits play a unique role in the "food chain" from materials to gigahertz: they hide the physics from designers; they form the most basic system-building blocks; and they provide the essential traction for handling billions of competing system implementation details.

C2S2 research invents the new design techniques



C2S2 demonstrated process variation reduction.

necessary to convert near-limit scaled devices and post-silicon devices into useful system-building blocks. It targets these design innovations across diverse design domains--digital, analog, RF, photonic, and MEMS designs.

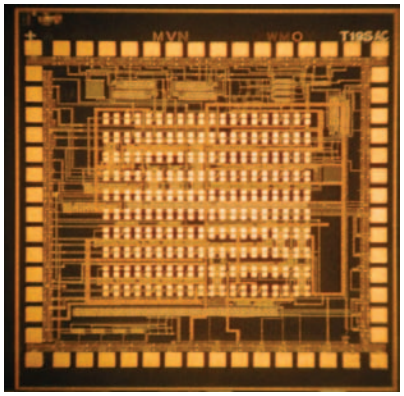
Research in the Circuit Design Center provides the needed link between devices and system design.

C2S2's 2004 Research Highlights

• Designed and fabricated a FinFET test chip using a 35 nm metal-gate FinFET manufacturing process and used it as the basis for comparison of FinFET performance in typical circuit topologies. Circuit performance was shown to be highly dependent on the orientation of FinFETS in the crystal lattice.

• Demonstrated a novel design approach that deploys a range of supply voltages to reduce power consumption by up to 33% and current leakage by up to 42%.

• Demonstrated how process variation in the manufacture of via patterned gate arrays can be significantly reduced by the choice of circuit topology.



Optical clocking silicon test chip

• Introduced the concept of probability intervals into CAD design tools as a substitute for scalar numbers. Demonstrated a 16 times processing speed improvement over Monte Carlo based tools.

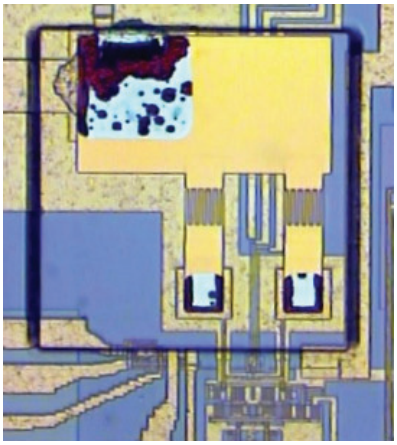
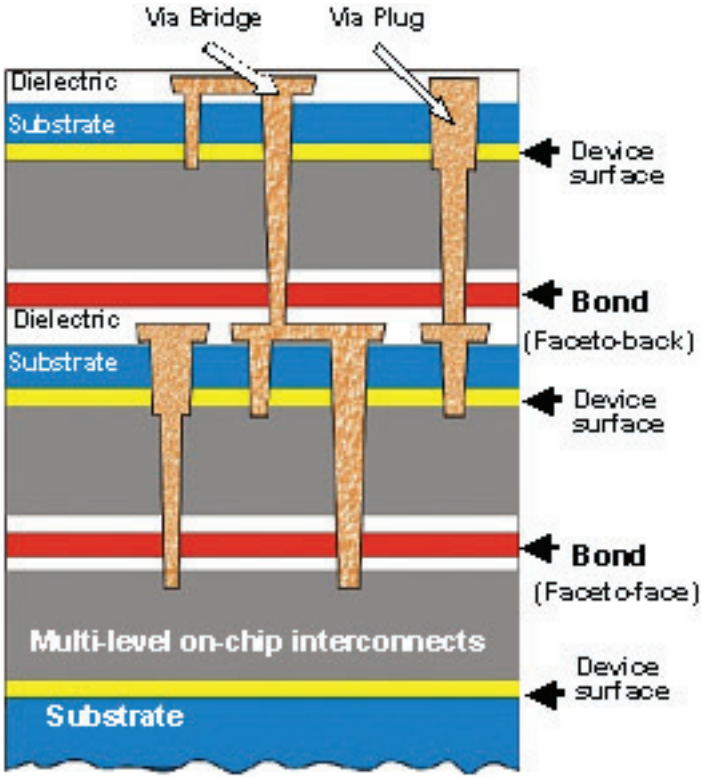


Photo detector CMOS test chip

IFC

The Interconnect Focus Center (IFC) is led by Georgia Institute of Technology. Professor James Meindl is the director. The center conducts research to discover and invent new electrical, optical, and thermal interconnect solutions that will meet or exceed ITRS projections and enable hyper-integration of heterogeneous components for future terascale systems.



Example of 3-D integration for stacked semiconductors

The center focuses on research of all aspects of the wiring that connects the millions of transistors on a microchip, from process to system-level architecture. Today and in the future, the microelectronics and nanotechnology industries will lead the evolution of technology in industries from automotive to medical, and from computing to aviation. IFC strives to stay atop all advances in these fields and play a major role in driving this technology into the future. To that end, the center's research themes have evolved to accommodate this goal.

IFC's 2004 Research Highlights

• Research into the use of carbon nanotubes for interconnect design continues. In 2004, IFC grew the largest self-ordered arrays of uniform aligned carbon nanotubes to date and measured surprisingly high ballistic conductance in a single wall carbon nanotube, highlighting the significance of conductance in nanotube-based design.

• Optical interconnects hold great promise as future high speed interconnects between semiconductors.

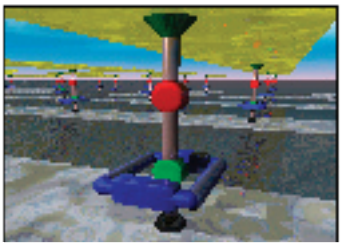
Implementing basic optical components in CMOS is a challenge. IFC has made some recent breakthroughs including optical clock injection directly into CMOS circuits and the first monolithically integrated laser on Ge/GeSi virtual substrate on Si.

• Multiple 3-D semiconductor interconnect technologies have been developed. Research continues into their integration properties, reliability and associated CAD tool extensions.

• Research continues into micro fluidic cooling, a promising technology that may help tame hot running semiconductors. Research includes micro channel fabrication, fluidic CAD development, and experiments on micro-channel convection.

MSD

Materials and Devices research is conducted by the Center for Materials, Structures and Devices (MSD) at the Massachusetts Institute of Technology. Professor Dimitri Antoniadis is the center director. This center's focus is to explore and determine the most promising path for microelectronics in the next two to three decades by pursuing two overlapping approaches: scaling of CMOS to its ultimate limit and interdisciplinary exploration of new-frontier devices.



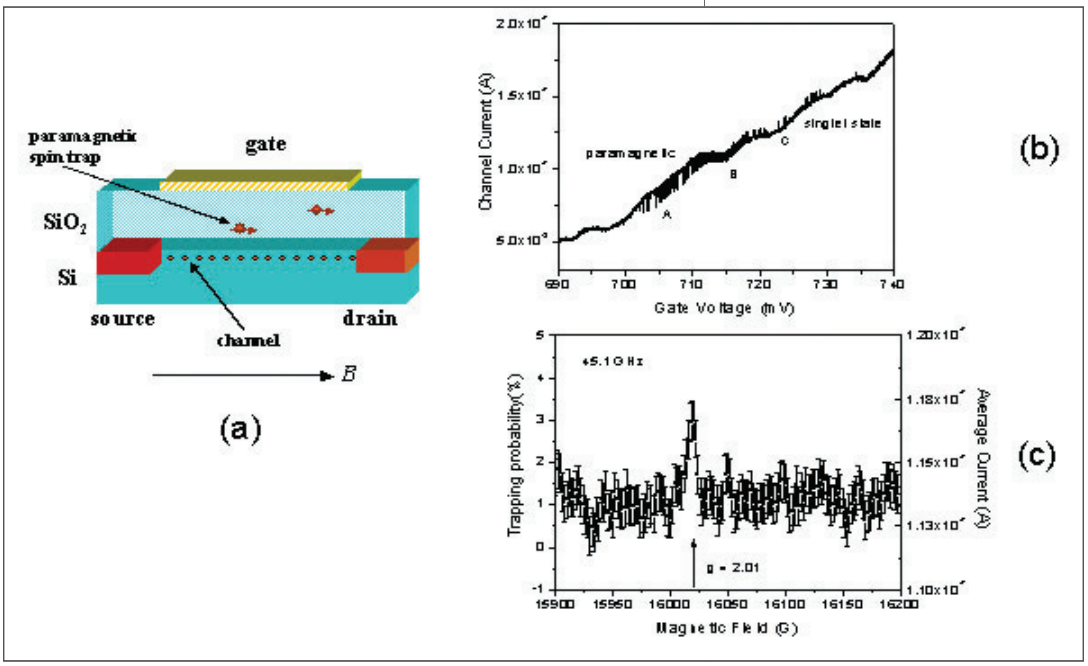
Molecular Switch

Since its inception in 2000, the MSD Center has successfully launched entirely new materials combinations for high performance CMOS applications, while pushing new frontier devices, such as carbon nanotubes, to new heights of performance through the combination of novel chemical synthesis of nanostructures with advanced front-end processes borrowed from silicon technology. In addition, the MSD center is well along its way to establishing realistic benchmarking of highly disparate devices on equal footing via close collaboration of experimentalists from different disciplines with advanced modeling and simulation researchers.

Research in this center is organized into five research themes. Four of the themes concentrate on experimental research in device technology while the fifth collaborates with the other four in addressing key process and device issues by advanced modeling and simulations.

MSD's 2004 Research Highlights

• Research continues into how to deploy carbon nanotubes to improve field effect transistor performance. MSD has developed the first self-aligned ballistic carbon nanotube pFETs with high-κ. An 8 times performance improvement has been demonstrated.



Electron spin resonance measurement

• Improving the performance of CMOS- based semiconductor technology is becoming increasingly challenging as gate sizes continue to shrink. Novel ways to extend the effective life of CMOS are needed. MSD is developing ways to integrate molecular devices with Si. Recent achievements include the integration of two-terminal molecular devices with Si, the devel-

opment of processes for constructing molecular electronic switches, the effective use of nano-patterning methods, and the implementation of devices in cross point array to achieve densities of >1011/cm2.

• In order to manipulate individual spin qubits, one has to at least be able to measure the electron-spin-resonance of a single spin. To this end, electrical detection of electron spin resonance of a single paramagnetic spin center in the gate silicon dioxide (SiO2) of a sub-micrometer CMOS device has been demonstrated for the first time.

FENA

Research in Nano Materials is conducted by the Focus Center on Functional Engineered Nano Architectonics (FENA), the newest focus center. Professor Kang Wang of UCLA is the center director. The center's research is directed at resolving the cross-cutting materials and device challenges related to beyond-CMOS in order to create new information processing paradigms with greater capabilities.

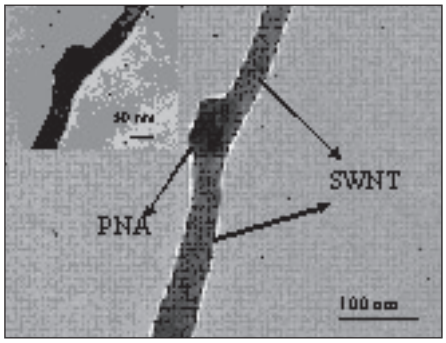
In order to tackle major challenges common to all nanometer scale devices, new nanoscale materials and processes are needed to address the core problems of nanoscale technology. Opportunities exist for creating a new generation of nanoscale materials, structures and devices, which will extend semiconductor technology to CMOS limits and beyond, and provide heterogeneous interfaces of new nanosystems, enabling a combination of biological and molecular functions that lead to new paradigms of information processing and sensing.

Through this new generation of nanostructured materials, the semiconductor industry will continue to expand and create new applications of monolithically integrated (CMOS, molecular and biomolecular) nanosystems. FENA focuses on the materials challenges at the nanoscale for fulfilling these opportunities.

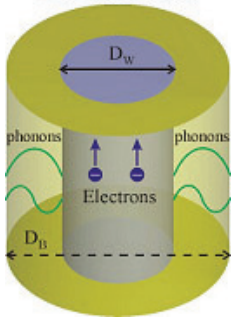
FENA's 2004 Research Highlights

• FENA has demonstrated that self-assembling polymer nanorods, can be switched between rigid and flexible forms, a promising step towards the self assembly of molecular structures.

• Another breakthrough has been the demonstration that peptide nucleic acids (PNA) can be used to link carbon nanotubes together, possibly enabling the assembly of complex nanotube structures.



• Phonons, waves that naturally occur in molecular lattice structures, have a significant impact on semiconductor performance. Research is being conducted to see how phonon tuning can improve this performance.



FCRP Sponsors

Semiconductor Industry Association (SIA):

Advanced Micro Devices, Inc.
Agere Systems
Analog Devices, Inc.
Conexant Systems, Inc
Cypress Semiconductor
IBM Corporation
Intel Corporation
LSI Logic Corporation
MICRON Technology, Inc.
Motorola, Incorporated
National Semiconductor Corporation
Texas Instruments
Xilinx, Inc.

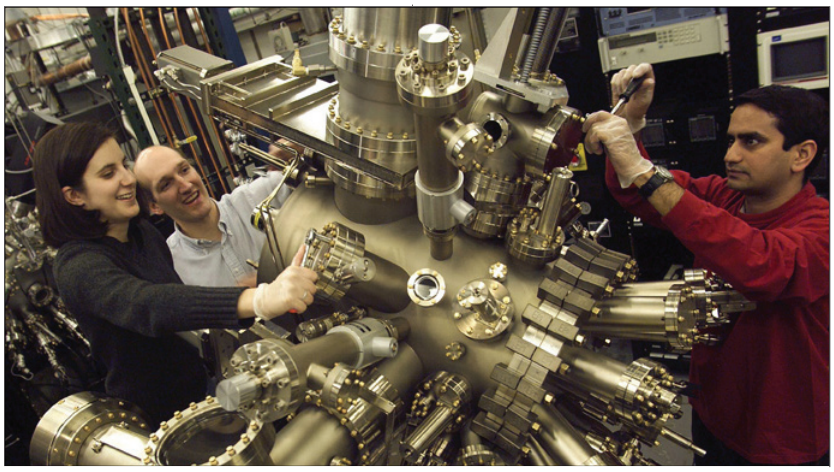
Semiconductor Industry Suppliers:

Air Products & Chemicals, Inc.
Applied Materials, Inc.
Cadence
KLA-Tencor Corporation
Novellus Systems, Inc.
Synopsys
Teradyne, Inc.

Department of Defense:

Deputy Undersecretary of Defense for Laboratories and Basic Sciences (DUSD/LABS)
Defense Advanced Research Projects Agency (DARPA)

More than 1,000 students participated in SRC-funded research in 2004; another 450 participated in MARCO/FCRP-funded research. Of SRC students graduating in 2004, 70% went to work for SRC member organizations or are undergraduate or master's students continuing to higher degrees, further strengthening the links within the SRC community. Of MARCO students graduating in 2004, 74% went to work in sponsoring organizations or are continuing to a higher degree. Other 2004 accomplishments include:



From l-r: Lisa Edge, Darrel Schlom, and Venugopalan Vaithyanathan with an oxide molecular-beam epitaxy (MBE) system, in which high-k alternative gate dielectric materials are grown on silicon. Photo by Cramer Studio.

• One new Core Fellowship, four new Company-Named Fellowships, and one new International Fellowship were awarded through the Graduate Fellowship Program (GFP) to bring the number of fellowships at the beginning of the 2004 fall term to 37. Sixteen SRC Fellows graduated in 2004.

• The first International Fellowship was awarded outside the United States to a student at National Taiwan University.

• Fourteen new Company-Named Master's Scholarships were awarded, for a total of 22 at the beginning of the 2004 fall term. Ten Master's Scholars graduated in 2004.

• The Graduate Fellowship Program Annual Conference was held in San Francisco with 16 student papers and 49 posters presented. Five students from the Undergraduate Research Assistants Program at Union College participated in the poster session. The keynote address was by Dr. Sunlin Chou, Intel Senior Vice President and General Manager, and the Awards Luncheon address was by GFP Alum Dr. James Comfort, IBM Vice President, Systems and Technology Group. Very positive feedback was received from companies, students, and faculty.

• The SRC Web site published 703 student resumes and the MARCO Web site another 293.

• The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars. A copy may be obtained by contacting SRC Student Relations.

• The third and fourth Simon Karecki Awards were made from the Simon Karecki Fellowship Fund to April Ross, TI/SRC Fellow at MIT, and to Hyoungsub Kim at Stanford. This award recognizes outstanding student performance through the SRC/NSF Center for Environmentally Benign Semiconductor Manufacturing, centered at the University of Arizona.

• MARCO/FCRP student/industry networking events were held in conjunction with the annual research reviews for the C2S2, MSD, IFC, and GSRC Focus Centers.

• TechConnects for SRC students were held at the University of Arizona, University of Wisconsin, The Ohio State University, North Carolina State University and in conjunction with the ADT/FEP Compact Modeling/Modeling and Simulation Review in NC.

SRC Education Alliance

The SRC Education Alliance (SRCEA), a wholly-owned subsidiary of SRC, is a non-profit private foundation under IRC sections 501(c)3 and 509(a). The Undergraduate Research Assistants (URA) program is managed through the SRCEA with funding from the Department of Defense and MARCO. The URA Program targets academically qualified students early in their undergraduate careers and seeks to build their enthusiasm for disciplines of interest to the semiconductor industry. Twenty students at 11 universities began this program in the fall of 2004, including three outreach students at Union College in Albany, New York.

Award Programs

James Meindl with SRC President Larry Sumney.

Aristotle Award

The 2004 Aristotle Award was presented to Professor James Meindl of Georgia Institute of Technology. The Aristotle Award recognizes SRC-supported faculty whose deep commitment to the educational experience of SRC students has had a profound and continuing impact for SRC members over a long period of time. The award acknowledges outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project.

Mahboob Khan Award

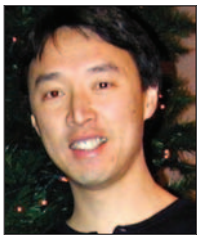
The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as industrial liaisons. Recipients represent "ideal mentors" whose commitment more than enhances the SRC research program.

The 2004 award recipients were:

James Egley

James "Skip" Egley of Motorola/ Freescale Semiconductor "incarnates the very spirit of an SRC industrial liaison," according to Professor Umberto Ravaioli of the University of Illinois/Urbana-Champaign. He became a collaborator with SRC student Gulzar Kathawala in the development of a new 3-D Monte Carlo Simulation program, providing both an industrial perspective and technical expertise. Colleagues Clarence Tracy and Ramachandran Muralidhar acknowledge that "Skip's contributions and his mentorship have been key in motivating students and helping them realize the value of their contributions."

Steven German of IBM is serving on the Ph.D. thesis committee for SRC student Ritwik Bhattacharya at the University of Utah. According to Professor Ganesh Gopalakrishnan, Steve is a mentor who directly interfaces with the students, spends quality time discussing over the phone on a regular basis with them and offers specific direction to their research project. John Darringer of IBM indicates that Steve's involvement has brought a deeper insight into and appreciation of university research, and the results are helping IBM keep up with today's technology.



Timothy Kam

Timothy Kam and **Michael Kishinevsky** of Intel served as a team with Professor Rajesh Gupta at the University of California/Irvine in the SRC- sponsored SPARK project, a new high-level synthesis methodology that is based on aggressive parallelization of the source code. Former SRC student Sumit Gupta spent the summer of 2001 with Tim and Mike at the Strategic CAD Lab in Oregon, enabling him to define the future course of the SPARK project. The work received a best paper award at the VLSI Design Conference in 2003.

T.M. Mak

T.M. Mak of Intel has a long history of providing a real-life view to the academic community. Professor Li-C Wang of the University of California/Santa Barbara notes that over the last three years, T.M. has visited the campus at least 17 times. T.M. prepared a presentation for each visit and led a follow-up discussion regarding possible research directions. According to Dr. Wang, "Several of his students have sought technical advice, advice which has had considerable influence in shaping the direction of some projects."

Sani Nassif

Sani Nassif of IBM has participated as an industrial liaison at the University of Minnesota with Professor Sachin Sapatnekar's research team for a number of years. Currently, the group is working on a project in circuit optimization for low power and

high speed in the presence of uncertainty. Sani has made an exceptional bridge between industry and the academic community. He significantly influenced the direction of former SRC student Haihu Su's research on power grid analysis and optimization, along with enabling several students to have "real-life" experiences at IBM's Austin Lab.

Technical Excellence Award


Rob Rutenbar


Richard Carley


Mani Soma

The SRC Technical Excellence Award is given annually to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research; who are ground-breakers and leaders in their fields; and who are regarded as model collaborators with their colleagues in the SRC member community. The Award is shared among researchers who have made key contributions to technology that significantly enhance the productivity of the semiconductor industry. The award consists of a $5,000 cash award which is divided equally among the research contributors.

The 2004 Technical Excellence Award was presented by SRC Board of Directors Chairman Craig Sander at the November 2004 Board of Directors' meeting.

This year SRC selected three professors who lead two technical programs, one at the University of Washington and the other at Carnegie Mellon University. All three have long-term relationships with SRC. Collectively, they have influenced nearly a generation of students who now are making a difference within the SRC member community. They have consistently tackled tough, real-world issues and offered creative technical solutions that are transferred into many member company processes.

Professors Rob Rutenbar and **L. Richard Carley** have been part of SRC's research team for more than 20 years. During that time they have been pioneers in the field of electronic design automation for analog/mixed-signal design. According to William Joyner, an IBM assignee to SRC and director of CADTS, SRC member companies, most notably Texas Instruments and Cadence Design Systems, have applied the innovation techniques developed in this research to production circuits.

John Cohn's (IBM) nomination of Professors Rutenbar and Carley describes the relationship "as one of the most enduring and productive collaborations in the history of SRC-funded research." According to Dr. Cohn, "Their work has set the groundwork for the entire emerging analog CAD industry." In conclusion, he shares that "the collaboration has been so sweet and productive that it's tempting to think of Rob and Rick as the Ben and Jerry's of analog CAD."

Professor Mani Soma of the University of Washington has been part of the SRC design community for more than ten years. His work in the area of test methods for RF systems has influenced many within the SRC community. Nominator Dr. Hosam Haggag of National Semiconductor Corporation writes that one of the strongest values of Dr. Soma's work "is that he bases his research on specification of real products and realistic case studies and not on a hypothetical matrix of parameters; in addition, he delivers his solutions ready to be implemented on silicon form processing and not merely a simulated file.

Dr. Soma's students are in great demand by SRC member companies, as they "have a strong unique technical and practical knowledge in the difficult field of analog/mixed signal and RF built-in self test." Professor Soma makes a special effort to encourage direct interaction between current students and the SRC member community. Over the years, his students have spent many internships at member company sites; the positive impact of these internships has been felt by both the students and the member companies.

Intellectual Property

Intellectual property (IP) assets emerging from SRC-sponsored university research programs are provided by SRC to its members to protect and enhance the value of SRC membership. IP assets serve to support SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs to SRC member companies. SRC's significant portfolio of intellectual assets minimizes the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship. IP assets are integrated with the SRC research catalog and complement the value chain as an important benefit of SRC membership.

In return for sponsorship, SRC receives non-exclusive, worldwide, royalty-free licenses to IP from university research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results may be investigated, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to provide a level playing field for members by ensuring that those who utilize SRC sponsored technologies do so only within the scope of a valid license. SRC also seeks to ensure that members receive and benefit from all IP rights from SRC research to which they are entitled.

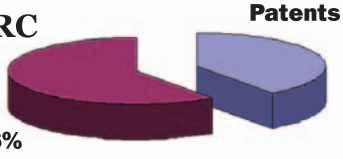
SRC continually investigates ways in which IP assets can provide new and additional sources of value to the SRC member community. In 2003, SRC pioneered an innovative joint licensing and commercialization partnership focused on commercializing selected inventions. The Exclusive Licensing Model has received strong support from several universities and member companies. This new program significantly benefits SRC members by increasing their potential competitive advantages while also providing for a possible new source of royalties. Under this new licensing model, select SRC and university intellectual property rights are combined and licensed to SRC. The formerly separate IP rights have greater value once combined in an escrow managed by SRC. As a result, enhanced commercialization prospects and greater licensing value can be provided as compared with the traditional SRC-university licensing model. The university, SRC, and SRC member companies agree on terms to sublicense one or more companies able to commercialize the invention and share the royalties collected. SRC, SRC member companies, and several universities are working together to implement this new experimental licensing model, seeking to build themed IP portfolios.

SRC's IP Advisory Board (IPAB), comprised of several SRC member company representatives, works closely with SRC on IP matters. In 2004 SRC and the IPAB identified inventions that could provide a substantial competitive advantage to member companies directly or through the availability of commercialized product. These inventions are excellent candidates for the Exclusive Licensing Model.

During 2004, a record twenty SRC-sponsored U.S. and foreign patents were issued, more than in any other year in our history. This brings the total portfolio of SRC issued patents to 233. SRC's significant patent portfolio supports both U.S. and international member company operations in numerous countries around the world. SRC's Web site permits members to submit real-time queries into SRC's IP database to obtain status on pending and issued patents as well as information about SRC-sponsored software provided to SRC members.

SRC's IP portfolio also provides over 453 software programs, software models, and technical databases to member companies. Software and database licenses from SRC-sponsored research programs represent a growing and complementary part of SRC's IP portfolio. Members are directed to the online software directory at www.src.org for further details. SRC members receive non-exclusive, worldwide, royalty-free intellectual property licenses in applicable software programs and technical databases.

Composition of SRC IP Portfolio



Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Multiple-thickness Gate Oxide Formed by Oxygen Implantation	Chenming Hu Tsu-Jae King	24-Nov-99 22-Jun-04	6753229	University of California at Berkeley
Patterning Methods and Systems Using Reflected Interference Patterns	David Joy Daniel Herr	12-Feb-01 4-May-04	6730443	University of Tennessee & SRC
Method and Apparatus for Providing Film Stress Measurements Based on Substrates Displacement	Anton Jachim	17-Jun-01 30-Nov-04	6826491	University of Wisconsin
Novel Non-crystalline Oxides for Use in Microelectronic, Optical and Other Applications	Gerald Lucovsky Gregory Parsons	25-Jun-01 7-Sep-04	6787861	North Carolina State University
Process for Forming Hafnium Oxide Films	Stephen Campbell Wayne Gladfelter	14-Nov-01 27-Jan-04	6683011	University of Minnesota
CMOS Parallel Dynamic Logic and Speed Enhanced Skewed State Logic	Sung Mo Kang Chulwoo Kim	7-May-01 21-Sep-04	6794903	University of Illinois
Micromachine Scanning Thermal Probe Method and Apparatus	Yogesh Gianchandani Mo-Huang Li Julius Wu	31-Oct-01 17-Feb-04	6692145	University of Wisconsin
Methods, Systems, and Computer Program Products for Modeling Inductive Effects in a Circuit Combing a Plurality of Localized Models	Michael Beattie Lawrence Pileggi	12-Mar-02 16-Nov-04	6820245	Carnegie Mellon University
Step and Flash Imprint Lithography	Matthew Colburn Grant Willson	19-Jul-01 13-Apr-04	6719915	University of Texas at Austin
Correction for Pipelined Analog to Digital (A/D) Converter	Ramesh Harjani Kavita Nair	7-Mar-03 31-Aug-04	6784814	University of Minnesota
CMOS Sequential Logic Configuration for an Edge Triggered Flip-flop	Sung Mo Kang Chulwoo Kim	18-Apr-02 31-Aug-04	6784694	University of Illinois
Guided Self-assembly of Symmetric Diblock Copolymer Films on Chemically Nanopatterned Substrates	Paul Nealey Juan De Pablo Franco Cerrina	5-Oct-01 8-Jun-04	6746825	University of Wisconsin
Reverse Biasing Logic Circuit	Sung Mo Kang Seung-Moon Yoo	21-May-01 6-Jul-04	6759873	University of Illinois

Intellectual Property

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Methods of Forming Nano-Scale Electronic and Optoelectronic Devices Using Non-Photolithographically Defined Nano-Channel Templates	Ozturk Mehmet Salah Bedair Veena Misra Zhibo Zhang	24-Jun-02 23-Mar-04	6709929	North Carolina State University
Submicron MOSFET Having Asymmetric Channel Profile	Sanjay Banerjee Xiangdong Chen	1-Oct-02 1-Jun-04	6744083	University of Texas at Austin
Method and Circuits for Reducing Dead Time Reverse Recovery Loss in Buck Regulators	Yuming Bai Alex Huang Nick Sun	11-Oct-02 18-May-04	6737842	Virginia Polytechnic Institute
Binary Non-Crystalline Oxide Analogs of Silicon Dioxide for Use in Gate Dielectrics and Methods of Making the Same	Gerald Lucovsky	13-Jan-03 3-Feb-04	6686264	North Carolina State University
Lanthanum Oxide-Based Gate Dielectrics for Integrated Circuit Field Effect Transistors and Methods of Fabricating Same	Angus Kingon Jon Paul Maria	12-Jan-03 22-Jun-04	6753567	North Carolina State University
Methods for Characterizing, Generating Test Sequences for, and Simulating Integrated Circuit Faults Using Fault Tuples and Related Systems and Computer Program Products	Shawn Blanton	25-May-01 28-Dec-04	6836856	Carnegie Mellon University

Foreign Patent

Novel Non-Crystalline Oxides for Use in Microelectronic, Optical and Other Applications	Gerald Lucovsky Gregory Parsons	issued on 2-Nov-04	NI-195870 (Taiwan)	North Carolina State University

Office of the Chief Executive

Larry Sumney
President and CEO

Ralph K. Cavin, III
Vice President,
Research Operations

Dinesh Mehta
Vice President,
Business Operations
& Strategic Initiatives

2004 Board of Directors

Chairman
Craig Sander - Advanced Micro Devices, Inc.

Steven J. Hillenius - Agere Systems

Walter Class (January-March) - Axcelis Technologies, Inc.

John Poate (March-) - Axcelis Technologies, Inc.

S. C. Sun - Chartered Semiconductor Manufacturing

Pawitter Mangat (January-June) - Motorola, Inc.

Claudine Simson (June-) - Freescale Semiconductor, Inc.

John Warlaumont - IBM Corporation

Sunlin Chou - Intel Corporation

Richard D. Schinella (January-October) - LSI Logic Corporation

Joseph Zelayeta (October-) - LSI Logic Corporation

Walden C. Rhines - Mentor Graphics Corporation

Mohan Yegnashankaran - National Semiconductor Corporation

Wilbert van den Hoek - Novellus Systems, Inc.

Larry W. Sumney - Semiconductor Research Corporation

Hans Stork - Texas Instruments Incorporated

S. W. Sun - United Microelectronics Corporation

Financial report available on request.

Semiconductor Research Corporation®
http://www.src.org

Brighton Hall, Suite 120, 1101 Slater Road
Durham, North Carolina 27703
(919)941-9400