INDISPENSABLE RESEARCH

2006 ANNUAL REPORT

Semiconductor Research Corporation

"When the SRC began operations almost 25 years ago, the concept of close university-industry cooperation was new and at times viewed with skepticism. Further, the US semiconductor industry was suffering from stiff competition from abroad and directing valuable industrial resources to universities was thought foolish by many in industry. Nevertheless this bold experiment has proven to be more successful than anyone could have imagined and transformed the way industrial sponsored university research is carried out. Today, the SRC and its various programs, still stand as a model for productive industry-university cooperation."

Stephen W. Director
Senior Vice President & Provost, Drexel University
SRC University Advisory Council

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Overall SRC Snapshot of 2006

- *3,829 Technical Documents*
- *116 Contracts Launched in 2006*
- *147 New Tasks*
- *1,485 Students*
- *774 Industrial Liaisons*
- *4,286 Event Attendees*
- *23 New Patents in Portfolio*
- *75 Inventor Recognition Awards*

Thanks to the foresight of SRC's founders nearly a quarter century ago, combined with the insight gained from other industry leaders who have since joined with them, SRC, the industry, and the world's leading universities are keeping pace with Moore's Law.

When the Semiconductor Research Corporation began in 1982, the consortium was formed by the leading U.S. semiconductor companies as a university research arm for the industry. The world semiconductor market was about $20 billion. SRC has rapidly evolved as a provider of indispensable collaboration among industry and academic resources and now serves as a global research facilitator for a market that has grown by an order of magnitude.

The members increasingly rely on SRC for vital research contributions to their technology infrastructure.

Among the lessons that the members have instilled in their consortium is that the world becomes more of a global village every year. The ability to collaborate across time zones and technologies becomes more pressing. During 2006, Applied Materials and Tokyo Electron committed to membership in the SRC's global program, creating an unprecedented forum for the industry's leaders.

In 2006, SRC continued its emphasis on extending the range of silicon-based technology and its applications. Non-classical CMOS research, speech recognition on a chip, aggressive advancements in nanoelectronics and even self-healing semiconductors were among the hundreds of SRC-directed projects that responded to this quest. In addition, planning began for a significant new initiative called Functional Diversification that is application-driven and is aimed, at least in part, at developing new system architectures which can potentially deliver immediate benefits in terms of functionality and cost, independent of the dimensional scaling of transistors. We believe that this initiative, combined with traditional programs in support of scaling, will enable a continuation of the ITRS cadence.

Distinguished industry veterans, Ms. Betsy Weitzman, Dr. Steve Hillenius, and Dr. Jeffrey Welser, assumed staff leadership roles for SRC research.

The family of SRC programs, encompassing both domestic and global offerings, was further enhanced through branding of the three research programs and the Education Alliance. Serving the world's industry, the Global Research Collaboration (GRC) now has 15 members and has research contracts with over 100 universities worldwide. The U.S. chip community and the Department of Defense's (DoD) research needs are supported by the Focus Center Research Program (FCRP), that leverages the strengths of more than 38 universities to scale CMOS to its theoretical limits. The Nanoelectronics Research Initiative (NRI) coordinates research at some of the top engineering schools in the U.S. to identify the next "information element" beyond the CMOS transistor.

In order to build the most comprehensive cooperation possible, SRC actively advocated government participation in research and transformation of new ideas into successful business and security applications. With the help of public-private partnerships, scientists and engineers trained in SRC's network of universities – the

world's best – have pioneered key technologies that can enhance the quality of life for everyone.

Having played a role in almost every phase of the members' proprietary approaches to integrated circuit design, simulation, verification, manufacture, testing, packaging and reliability, what is next for SRC? As the cadence of Moore's Law continues and technological

During 2006, Applied Materials and Tokyo Electron committed to membership in SRC GRC, creating an unprecedented forum for the industry's leaders.

complexity increases, the value of effective cooperation also increases. GRC sponsors design and process research programs for the International Technology Roadmap for Semiconductor (ITRS) 22-nm and beyond technology nodes. GRC members increasingly rely on SRC for vital research contritutions to their technology infrastructure. Our members now generate revenues at 45 nanometers - amazing progress since our founding focus on a 16-MB DRAM. And so, looking forward, SRC's research in scaling CMOS will continue and will be complemented by functional scaling research. The overall objectives of SRC's research program include maintaining the vitality of the current industry and providing breakthrough results that will open new technological and marketing opportunities.

As the members begin SRC's silver anniversary year, the consortium's number one deliverable continues to be unprecedented collaboration among all segments of the semiconductor industry with the world's best university research experts. Perhaps more significant than any single technical accomplishment, that cultural deliverable serves as a foundation for a continuing flow of innovations that will serve humankind.

As you review the annual report for 2006, you will see milestones and plans that help describe why SRC will become even more relevant and indispensable for the industry's future.

Larry Sumney
President and CEO

Over the past 24 years SRC member companies have invested $854M in cutting-edge semiconductor research supporting over 5,500 students and 1,244 faculty members at 218 universities worldwide. The marketplace and the complexion of the industry continue to change rapidly, presenting ever-greater challenges to maintain critical research and to sustain SRC's reputation as the preferred sponsor of university research.

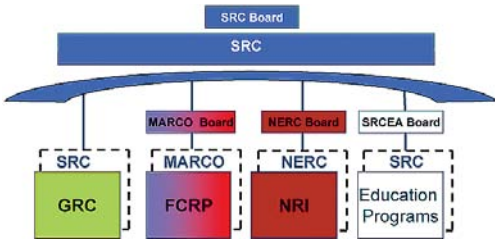
In 2006, an SRC Board of Directors Ad hoc committee developed and executed a branding program for SRC and its programs/entities that will clearly establish SRC as:

- *A powerfully positioned "over-brand," with separately branded, highly differentiated programs*
- *An indispensable research consortium that delivers sustainable competitive advantage to its members through research and students*
- *The dominant leader in management of university research*
- *Difficult to displace; demonstrated ability to remain relevant and relentlessly innovative over time*

Four separately branded, and highly differentiated programs have been established under the SRC umbrella: SRC GRC, SRC FCRP, SRC NRI and SRCEA.

SRC

SRC is the world's leading advanced semiconductor university research consortium, with member companies and research programs spanning the globe. It is an indispensable part of the R&D strategies of the world's leading semiconductor companies and has proven to be a value-added research management model that delivers unsurpassed advantage to its member companies. SRC-sponsored university research is of the highest caliber and creates the knowledge and breakthroughs that will invent the industries of tomorrow.



SRC GRC

The Global Research Collaboration program (GRC) is a unique operational model which harnesses research from the world's top universities and turns it into competitive advantage for its members. This operational model includes intense industry engagement in formulating, shaping and executing the research agenda. It offers a high-leverage, compelling return-on-investment to its members.

GRC programs address the critical challenges on the International Technology Roadmap for Semiconductors (ITRS), and are delivering the solutions that sustain Moore's Law and provide competitive advantage to the leading-edge member companies. One of its unique features is the Research Customization Program, that ensures the research program meets individual member's needs. Additionally, GRC offers two optional programs; Topical Consortia and Member Specific Programs provide exclusive benefits to individual members while leveraging the infrastructure and core competencies in place.

Member company representatives comprise five Science Area Coordinating Committees (SACCs) and 15 Technical Advisory Boards (TABs), that develop research needs statements and evaluate and select programs proposed by the university community. In 2006, 132 worldwide universities investigated a full spectrum of semiconductor technologies through 561 funded research tasks. Each task is evaluated during an annual research review attended by SACC and TAB members, Industrial Liaisons, university faculty, and GRC-funded students.

GRC continued to emphasize student programs as nearly 1,000 students participated in GRC-funded research in 2006. Of the GRC students graduating this year, 60% went to work for GRC members or are pursuing advanced degrees. (See page 24 for more information about student programs).

Our Web site continues to be the "go to" place for all information related to GRC. The electronic document library houses more than 18,000 documents, including over 2,200 new titles added this year. The research engine continues to be the primary method for extracting targeted information for member company professionals. Twenty-nine new software programs were added to the software directory (for a total of 518 software programs), 17 new on-line Technology Transfer e-workshops were conducted and 16 new patents were added to the GRC intellectual property portfolio. In 2006, the Executive Technical Advisory Board reviewed research output and identified more than 118 "nuggets" of compelling research, which has or will provide significant impact on our members' business, technology and/or product success. (See page 6 for critical research highlights).

SRC FCRP

The Focus Center Research Program (FCRP) is a pillar of the U.S. semiconductor research strategy. This entity is a natural extension of the historic strong relationship between the U.S. industry, government, and the U.S. university research community. FCRP, co-funded by the U.S. semiconductor industry and the U.S. government, was established to break through the "red brick walls" of the International Technology Research Roadmap by creating options to extend CMOS to its ultimate limits. Its unique management model is designed to allow much greater autonomy to the university researchers to facilitate more rapid creation of breakthrough options.

U.S. university research experts have assembled themselves into the best research teams available since FCRP has been organized to foster multi-university, multi-disciplinary collaboration. The resulting five Focus Centers address broad-based research needs spanning the entire spectrum of semiconductor technology. FCRP offers leverage to both industry and government sponsors. FCRP gives U.S. companies a significant competitive advantage in the race to lead the technological revolution by innovation. This university research program gives the U.S. DoD one-to-one leverage, resulting in a high payoff. FCRP research helps to create the breakthroughs that are critical to the U.S. security and economic competitiveness goals. (See page 16 for critical research highlights).

SRC NRI

The Nanoelectronics Research Initiative (NRI) is establishing the U.S. as the world leader in the nanoelectronics revolution. It is leading the nation in developing the next information element, beyond the CMOS transistor. NRI collaborates with national nanotechnology efforts to produce fundamental breakthroughs in physical sciences and engineering. Structure and execution of this entity are designed to move research results more successfully and smoothly from the laboratory into cost-effective production. Fundamental breakthroughs in physical sciences and engineering resulting from SRC NRI will ensure that the U. S. is a world leader in high-tech manufacturing. (See page 22 for highlights of NRI accomplishments).

SRC EA

The SRC Education Alliance (SRCEA), a wholly owned subsidiary of SRC, is a non-profit private foundation under IRC sections 501(c)3 and 509(a). (See page 24 for details).

The GRC partnership leverages the world's university research capabilites to meet the needs of the global industrial partners. In the following paragraphs, we give a brief sample of the many research results that are of significant value to the member companies. We gratefully acknowledge the support of our partners in this research, including Defense Advanced Research Projects Agency (DARPA), National Science Foundation (NSF), and the State of New York.

SRC's overarching goal is to conduct university research that not only sustains the ITRS rate of progress in integrated semiconductor technologies but reaches beyond CMOS to identify the next information element. GRC research will continue its traditional emphasis on feature scaling and on functional scaling including the addition of new integrated circuit materials. An expanded effort in functional diversification research is planned to develop basic concepts leading to new applications. A brief description of a few of the research results that have had an impact on the industry follow.

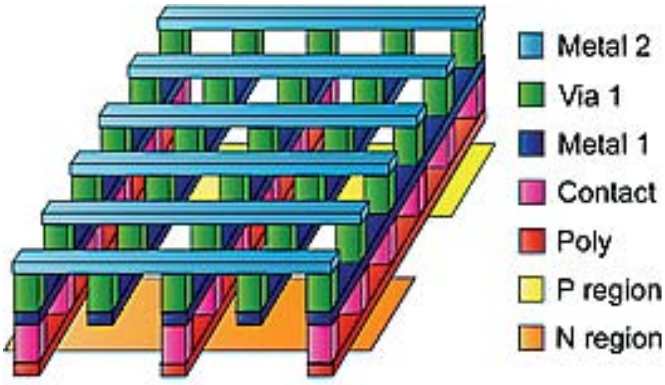
GRC Snapshot of 2006

- *2,271 Technical Documents*
- *116 Contracts Launched*
- *147 New Tasks*
- *906 Students*
- *774 Industrial Liaisons*
- *2,631 Event Attendees*
- *16 New Patents in Portfolio*
- *24 Inventor Recognition Awards*

Integrated Circuits and Systems Sciences

Two thrust areas in Integrated Circuits and Systems Sciences (ICSS), namely Circuit Design and Integrated System Design, addressed research priorities in the areas of low power, design robustness, and high performance.

As the ability to manufacture circuits with smaller feature sizes progresses, the variability of the required patterns is increasing. This increase makes it more difficult to design circuits that take advantage of advanced process capabilities. To help minimize the effects of this lithographic variability, researchers from Carnegie Mellon University have pioneered work on "Circuit Primitives for Regular Logic Bricks." This ICSS project uses geometric pattern regularity in conjunction with complex logic functions to minimize the effects of process variation but does so with minimal impact on the overall area of the design. Members see this regularity approach as a critical enabler for advanced designs with hundreds of millions of transistors.



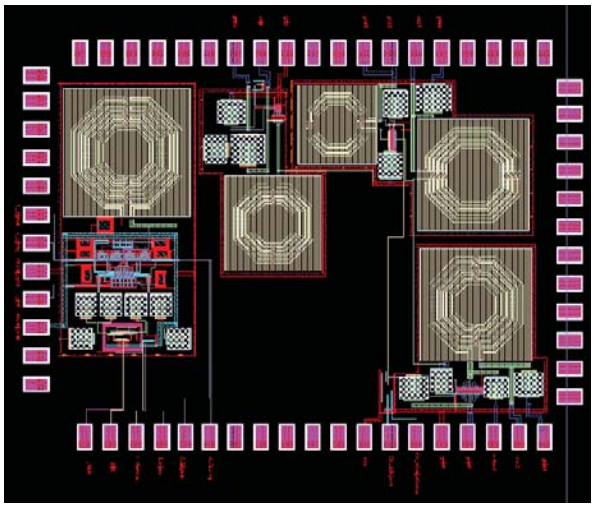
Regular Logic Fabric

Another challenge facing microprocessor chip designers is managing the heat generated during operation. If the heat is not effectively controlled, the chips may get hot enough to self-destruct. At the University of Massachusetts, researchers are addressing the thermal

aspect of circuit robustness. This ICSS project addresses power-efficient on-chip thermal sensor circuits that will operate very quickly and can be used as part of a comprehensive approach to dynamically change either the voltage or frequency of operation to prevent overheating and self-inflicted damage.

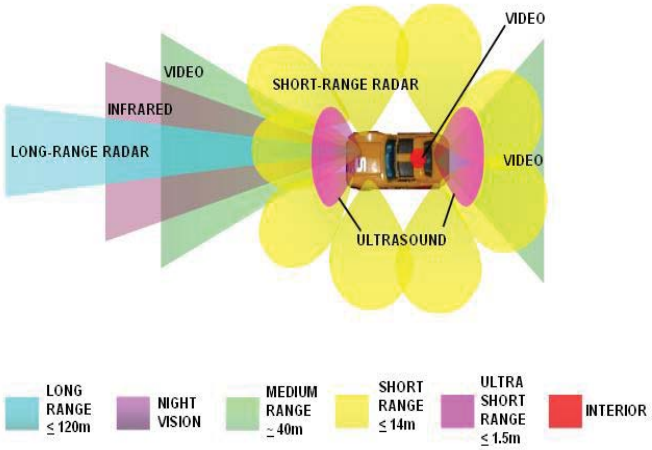
As chip design makes more processing power available within the die, system designers are challenged to make the increased performance noticeable to the end user. One of the greatest difficulties in doing this is the ability to design very high speed output transmitters and input receivers capable of moving large amounts of data between microprocessors and memory at high data rates with extreme reliability and low power. Researchers at the University of Minnesota have designed high speed clock and data recovery circuits using injection locking techniques that enable input receivers to handle very high speed data upwards of 20 Gb/s. Key to this ICSS project are new receivers with cross-talk cancellation (XTC) circuitry. By cancelling the cross-talk from adjacent channels, significant increases in data rate can be achieved. These new techniques are already being employed in member company designs.

Wireless data transmission abounds in modern applications such as cell phones, and member companies are working to develop new products in this area that are cost and power efficient but still have high performance. Researchers at North Carolina State University have developed an advanced RF transmitter design targeted for deep submicron CMOS that is a lower cost alternative to the often-used silicon-germanium (SiGe) technology. With CMOS technology, performance parameters such as high-output power in combination with high-linearity are difficult to achieve. This work is the first to achieve +10dBm output power with high linearity for 3G WCDMA transmit applications through the use of novel predistortion techniques.



WCDMA Transmitter Testchip

Another wireless research project has focused on extending the use of CMOS technologies at 77 GHz. Understanding the limitations of circuits at these high frequencies will help designers push cost-effective silicon into new applications such as vehicular radars, wireless local area networks, and Instrument Scientific and Medical (ISM) bands. This ICSS project at the University of Florida targets use of radar in collision avoidance systems and could increase automobile safety worldwide.

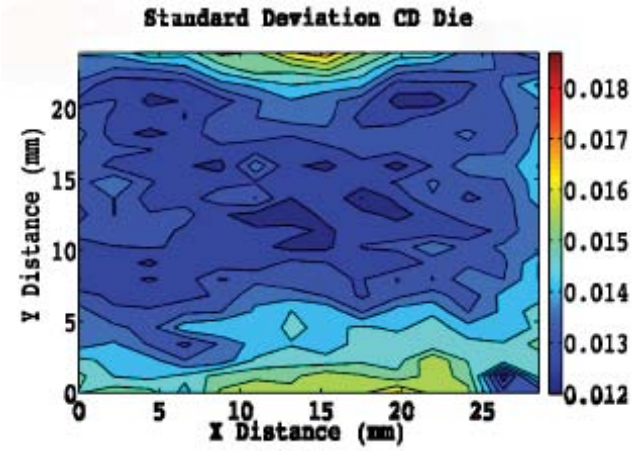


Automotive Radar Application

Computer Aided Design and Test Sciences

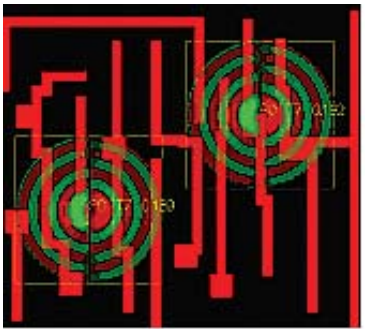
Three thrust areas in Computer Aided Design and Test Sciences (CADTS), Verification, Test and Testability, and Logic and Physical Design, addressed research challenges for tools that increase design productivity, assure correctness, improve manufacturability, minimize power and reduce cost.

In CADTS progress has been made in research for tools that will help designers increase productivity while generating higher performance circuits that are more robust and more manufacturable. Researchers at the University of Michigan have demonstrated a productive simulation tool and flow to link multiple sources of lithography variability to performance metrics. The new



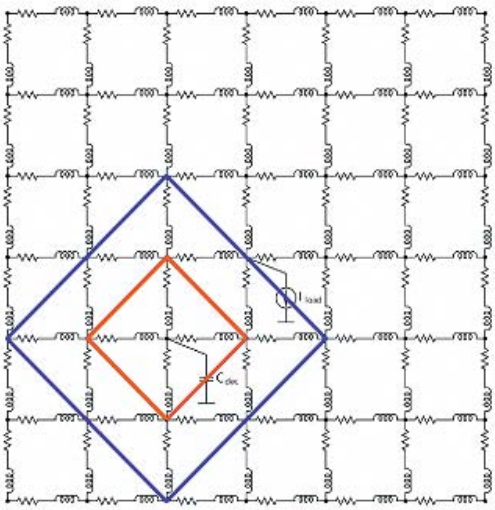
methodology has helped GRC members to understand the impact of variability in neighboring cell structures due to focus variations and then to make improvements in layouts that will result in increased yield and performance.

A team at the University of California/Berkeley is developing a process-aware EDA tool kit that will also help couple design tools to manufacturing. This research looks at the proximity effects in layouts that cause undesired aberrations during patterning due to diffraction, defocus and coma and provides tools to recognize and avoid these effects during physical design. Members see this as providing key insights into how to couple EDA design tools to DFM requirements.



Proximity Effect Influence Function for Coma

As technology nodes advance, power is saved by voltage scaling. An undesirable side effect, however, is that circuits are more susceptible to noise generated by logic transitions on the chip. Designers add decoupling capacitors to the power rails to reduce this noise; however, this is one of the more difficult design problems of large-scale mixed-signal circuits.



Effective Radii of On-Chip Decoupling

Researchers at the University of Rochester have created a novel design tool that enables members to automatically place decoupling capacitors optimally within their power distribution grids.

At Portland State University researchers have developed test methods aimed at improving final test yields by applying statistical post-processing for outlier

screening. GRC members expect cost savings by being able to reduce product burn-in requirements. Burn-in has historically been the most effective method for screening parts susceptible to infant mortality. These defect-based testing methodologies using canonical correlation are capable of reducing the infant mortality rates and reducing or eliminating the need for costly burn-in.

Statistical static timing analysis (SSTA) has been very important to designers in recent years that accurately and efficiently captures impact of process variations on circuit timing. Most approaches make simplified assumptions using basic statistical delay models that reside in the simulator. Researchers at Texas A&M University have developed a new statistical timing analysis tool, employing accurate delay models, that not only give designers more accurate results but also help guide designers on how to best define the inputs to the tool. Members see these models as filling the gap between SSTA tools and real circuits. The final result is that members can use this tool to develop products with higher performance.

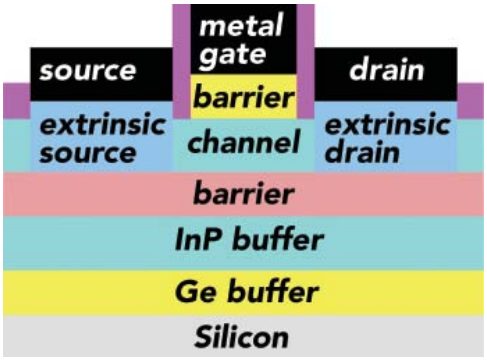
Device Sciences

Schematic of a High-k, Metal Gate "Stack" with an SiO_2 Interfacial Layer

Device Sciences (DS), in collaboration with university and industry partners, is playing an essential role in the conduct of research to sustain the unprecedented progress in scaling of semiconductor technology to attain giga-scale transistor densities and performance. Traditionally, the recognized enabler for these exponential gains in performance per unit cost and transistor density has been feature size scaling of the MOSFET. Recently, however, introduction of material innovations has played a major role in scaling, e.g., strained silicon.

The Digital CMOS Thrust executed a major change in programs in 2006 by transitioning research from the highly successful Front End Process Transition Center into the new Non-classical CMOS Research Center. The Front End Transition Center, and its predecessor, the Front End Process Research Center, led by North Carolina State University, played a pivotal role over a combined period of eight years in the exploration and development of the new high-k, metal gate stack technologies recently announced by two companies within the industry.

Major contributions for hafnium-based high-k dielectrics include i) development of a complete energy band model for the high-k gate stack, ii) first use of nitridation block boron diffusion to enhance stability, iii) first demonstration of channel mobility > 90% of the mobility associated with silicon dioxide on silicon, iv) first observation of nano-crystallization and phase separation in hafnium and zirconium oxides and silicates, v) invention and development by Yale University of the Inelastic Electron Tunneling Spectroscopy (IETS) metrology, vi) first observation of de-trapping in a high-k gate stack giving insight to issues related to the stability of the gate stack dielectric films, and vii) develop-



Materials Integration Substrate: III-V Growth on SI

ment of the internationally used Hauser CV analysis program and companion program to extract channel mobility.

As the recent industry announcements indicate that new high-k, metal gate stack technology will provide MOSFET scaling to and beyond the 45 nm technology node, Device Sciences is now directing research to explore new approaches to scale MOSFETS to beyond the 22 and 16 nm technology nodes. The new Non-classical CMOS Research Center, led by the University of California/Santa Barbara features a major new effort to explore and use extremely high mobility III-V compound semiconductor materials in the channel and source/drain regions of an otherwise silicon MOSFET to further increase the speed of an ultimately scaled MOS transistor.

Three major challenges must be addressed and solved in order to realize the potential offered by the III-V compounds. First, high quality III-V heteroepitaxial films need to be grown on silicon. Second, the high density of native defects prevalent on the surface of most of the III-V's needs to be passivated or reduced such that application of a high-k gate dielectric on the III-V surface yields an acceptably low density of dielectric – semiconductor interfacial defects. The third challenge is to develop a p-channel MOSFET having performance comparable to the expected performance of the n-channel device. Because the hole mobility in most III-V semiconductor materials is quite low, researchers will need to either exploit strained p-channel devices, where strain p-type material might increase the hole mobility, or use a germanium p-channel device which does offer an excellent hole mobility.

The Non-classical CMOS Research Center initially is focused on the first two challenges. To address the problem of realizing a well-passivated gate dielectric/semiconductor interface, the Center is working to understand the nature of the interfacial defects and how to remove them. Experimental tools such as scanning tunneling microscopy and scanning tunneling spectroscopy are being combined with theoretical analyses using Density Functional Theory to gain insight to the removal of these defects.

In summary, in 2006, Device Sciences concluded its research on high-k gate stack dielectrics and metal electrodes and began a new Center to aggressively pursue III-V compound semiconductor MOSFET device

technologies and structures to scale silicon CMOS to its ultimate limit.

Nanomanufacturing Science

The semiconductor industry's growth relies on the rate of increasing functional density and delivered value. This raises serious scaling and scaling independent challenges in manufacturing variability, cost, reliability, yield, sustainability, and factory operations. Nanomanufacturing Sciences (NMS) explores and enables affordable breakthrough nanomaterial design, integration, and fabrication options which circumvent Moore's second law, i.e. the rapid growth in the cost of fabrication facilities.

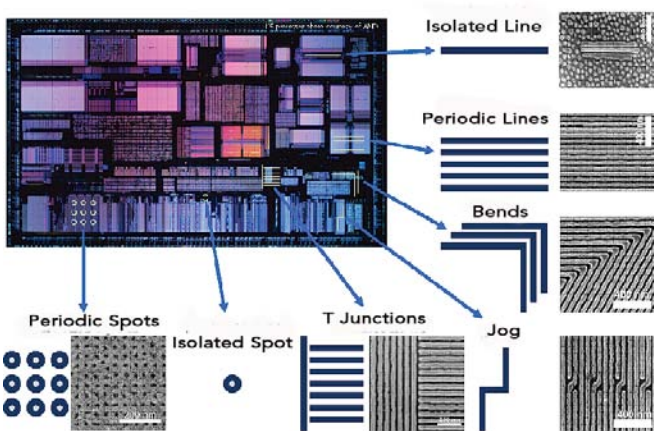
The research portfolio in novel materials and patterning methods for extending charge-based CMOS technology is strategically positioned to address member identified mission-critical challenges in the thrust areas of patterning, nanometrology, factory systems, and environment, safety, and health. Key growth areas include emerging research materials and processes, low variability nanomanufacturing for design, and simulation for CMOS extensibility.

Patterning

Patterning variability need not increase with decreasing circuit size. Two years ago, the University of California/Berkeley reported that defect-like structures, at layout, induce downstream process variability. Com-

puter Aided Design and Test Sciences is now addressing this upstream issue. In 2005 SRC demonstrated the feasibility of designed nanomaterials and nanofabrication methods that exhibit enhanced dimensional control, self healing properties, reduced process noise, and take advantage of the regular fabric architectures emerging from the design community as addressed in the Integrated Circuits and Systems Sciences section.

Recent results from the University of Wisconsin/Madison, demonstrate the feasibility of templated self-assembly to pattern six of the seven shapes deemed essential by the design community.

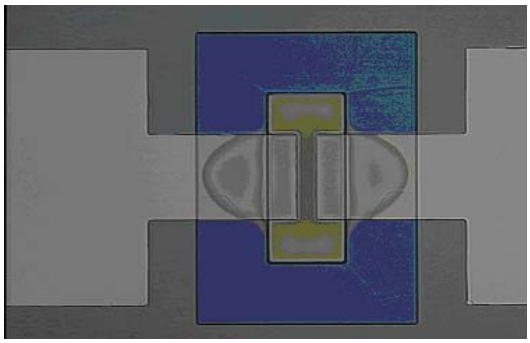


Self-assembled Six Essential Shapes

Member companies value this work to enable candidate options for extending photon-based lithography through the end of the ITRS, with the first real impact likely in memory, followed by logic.

Other resist-related research addresses the challenge of designing chemically amplified systems which satisfy projected photospeed and resolution requirements. The Cornell University group's exploration of molecular glasses and the University of California/Berkeley formulation of novel families of non-chemically amplified resists are particularly promising. This work "has signficant potential to address the current acid diffusion problem causing significant image blurring" in the words of one GRC member company representative.

Recent breakthroughs in Droplet-on-Demand patterning may enable low cost maskless printing of ~ 50 nm features for a number of applications. University of California/Berkeley colleagues recently reported Droplet-on-Demand patterning of organically coated metal nanoparticles, which sinter below 130ºC, for bonding applications. Initial results demonstrate a 5 times improvement in joint conductivity relative to a sampling of conventional Pb-based solders.



Droplet-on-Demand Enables Low Temperature Sintering and Enhanced Conductivity

Member companies value this research for its significant potential to enable low cost applications in electronics, biotech, and packaging areas.

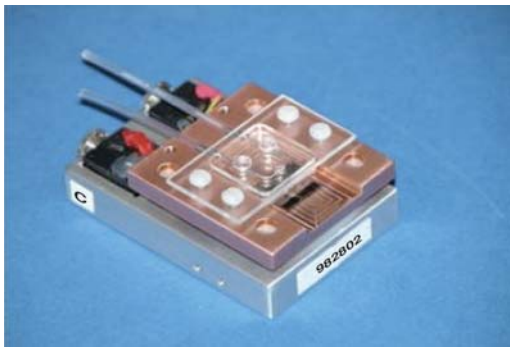
Environment, Safety, & Health

When GRC members speak of the value of cooperative Environment, Safety, and Health (ESH) research, two categories are particularly noteworthy. Member companies value the ESH focus on new materials, because it provides fundamental understanding of key ESH and technical issues associated with new process and materials technologies. The timely delivery of this knowledge enables the development and selection of new process chemicals which have minimal adverse EHS impacts. This thrust continues to address strategic issues in new materials, which range from the innovative, high-risk CMOS biosensor work at The University

of Arizona to low environmental impact super-critical CO_2 processing for patterned low-k dielectrics at Cornell University.

Member companies also find significant value in the optimization of materials and process chemistries. For example, new rinses are being developed efficiently and transferred to wafer fabs much more easily, with substantial cost savings for our members.

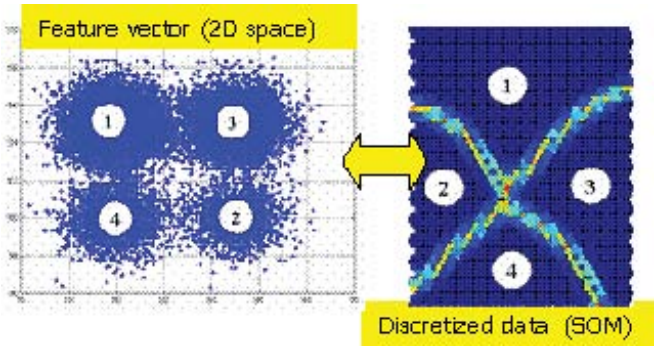
Optimization work is also wide-ranging. The chem-mechanical polish processes are being examined and modeled to reduce water and slurry use at The University of Arizona and Massachusetts Institute of Technology, and fundamental rinsing chemistry of surfaces is being examined at Stanford University.



First Generation Biochamber for Monitoring and Maintaining Cell Health Allows for Injection of Test Materials

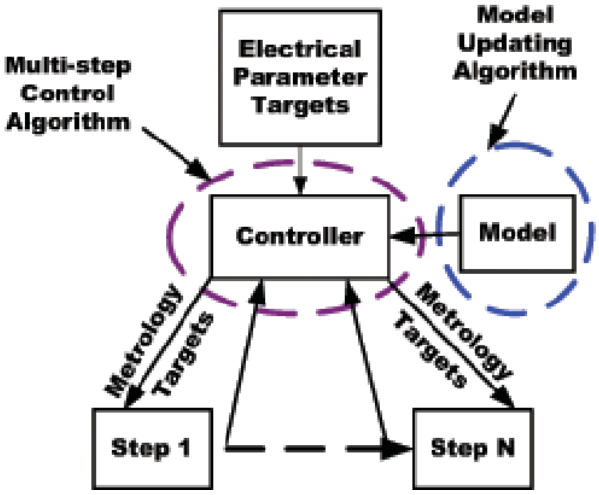
Factory Systems

University of Michigan researchers recently developed an integrated modeling tool, based on Self Organizing Maps (SOM), Bayesian networks, and real-life data, which enables the conversion of database queries into yield predictions. They demonstrated application of SOM and Bayesian network based estimation and prediction on real-life data for intelligent predictive maintenance which is one of the key factory challenges.



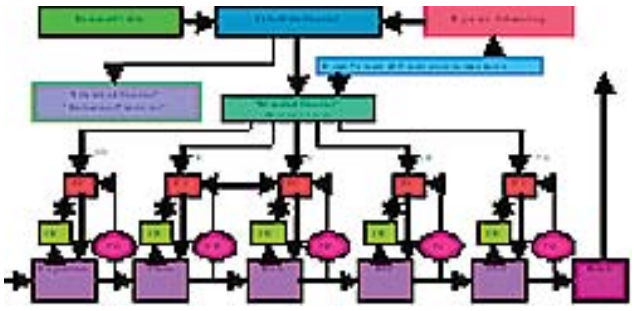
Application of SOM for Intelligent PM

Other GRC researchers at The University at Texas/Austin developed disruption management tools, which integrate operational components. This represents a significant step towards addressing ITRS-identified fab-wide control.



Multi-step Control for Fab-wide Control

Additionally, colleagues at Lehigh University developed a new model for semiconductor demand characterization using leading indicators and technology life-cycles, via S-curves and is based on a game theoretic framework for studying capacity negotiation.



Fab-wide Control Methodology

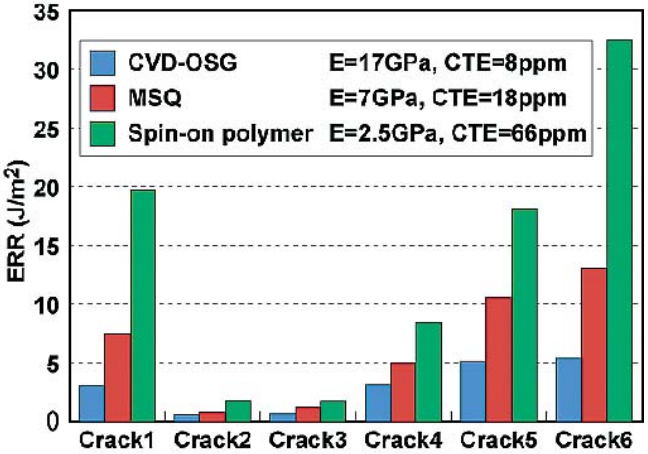
Interconnect and Packaging Sciences

Interconnect has become one of the major issues in continuing progress along the Moore's law curve. The mission of Interconnect and Packaging Sciences (IPS) is to resolve the many issues in the interconnect and packaging areas.

Significant advances were made in 2006 in the key areas of chip-package interactions, metrology, lead-free solders, and Cu/low-k metallization. Each of these areas represents not only challenges in the ITRS, but also opportunities to provide significant value to GRC member companies.

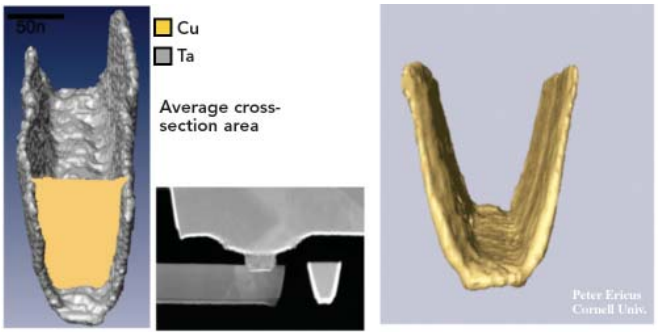
In the area of chip-package interactions, IPS programs also address emerging research topics in chip-package co-design. The first topic addresses modeling and simulation of stress-induced structural failures that occur during the insertion of the chip into the package in the manufacturing process. Second, IPS programs address the important issue of packaging reliability under extreme stress conditions caused by combined thermal and shock loading conditions. This work relates directly to the increasingly important problems of incorporating new materials and new packaging structures into portable and hand-held products. Third, GRC programs address the important area of identification of the susceptibility of chips to chip-package failures at the die level, rather than requiring full packaging to establish the failures.

Among the interesting programs in IPS addressing chip-package interactions are those associated with mechanical properties of the Cu/low-k system. These are the epitome of Back End Processing (BEP) and Packaging interface programs because they combine the BEP issues of mechanical properties of the Cu/low-k system to failures due to packaging stresses and strains that are usually addressed in the Packaging Thrust. At the University of Texas/Austin, metrology has been developed to evaluate interface bonding strengths in the Cu/low-k material system, along with modeling capabilities that use the interface bonding strengths to predict stresses and strains in Cu/low-k structures to predict failure possibilities under various conditions.



Crack Driving Force at the Interface (ERR) Predicts Spin-on-Polymer>MSQ>CVD-OSG

In the area of metrology, two key results were obtained from GRC programs in 2006. First, in Cornell University's program to investigate the critical problem of ultra thin barriers between Cu and low-k materials, supporting metrology has produced more than an order of magnitude increase in 3D resolution capability for nanoscale structures. Enhanced imaging capability is clearly illustrated below in the fine structure shown in the left hand image of a nanoscale barrier.



Advances in 3D Imaging Applied to Cu/low-k Barriers

The second key result is the completion and transfer of technology for ultra high resolution displacement techniques to document deformations of package low-k layers with displacement information in a region of 2 mm by 2 mm with a displacement resolution less than 0.1 nm. This capability, provided by the University of Maryland, addresses the critical need for nm resolution metrology for advanced packaging development.

The 2006 IPS advances in the area of Pb-free solders have included very interesting results on mechanical properties failure models and research results on novel Pb-free solder materials. In addition, an Auburn University research group has established a new capability for evaluating Sn-Pb and Pb-free solder failures under overlapping stress conditions. This group has produced analytical models for common circuit-card assembly architectures in electronic applications; they have identified damage proxies including model parameters, wavelet packet energy, phase-growth parameter, and derivatives. In addition, they have demonstrated a life-prediction methodology for some lead-free area-array packages subjected to high-rate transient shock and thermal aging. These accomplishments demonstrated the capability to bridge fundamental science and modeling and simulation with the practical problems faced by industry today.

Cross-disciplinary Semiconductor Research

Each year, SRC staff, in consultation with the Executive Technical Advisory Board, executes one or more fundamental studies involving SRC staff and, at least, one junior university faculty member. The purpose of these studies is to assess the possible benefits that might be derived from research in selected topical areas and to identify research directions that have the potential to open new pathways for advances in information processing technologies. Several fundamental studies have been conducted including:

Heat Management

A basic physical model was developed that indicates that technologies to cool by air is within a factor of ten of theoretical limits, whereas water cooling technologies offer the opportunities for several orders of magnitude improvement relative to current technologies. This study led us to speculate that a photon 'lens' arrangement coupled with photon emission might provide even greater opportunities for cooling technologies.

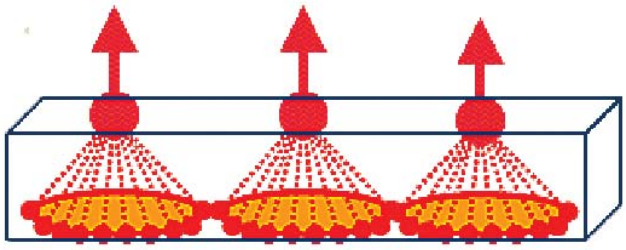
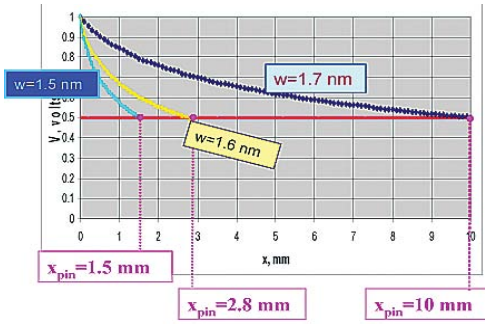


Illustration for Phonon Focusing

Interconnect Technologies

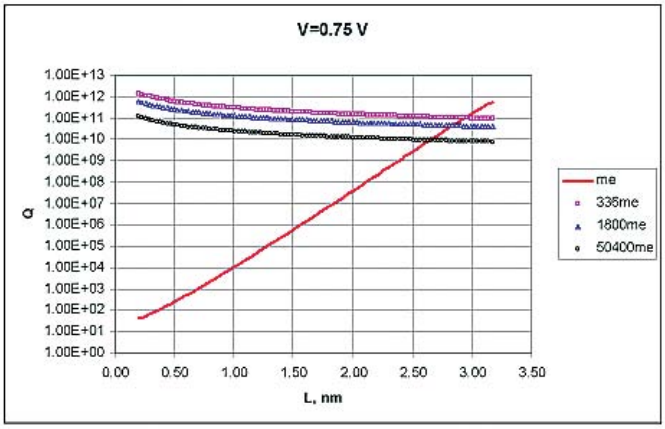
Silicon nanowires and carbon nanotubes were evaluated as possible replacements for Cu/low-k interconnect technologies using both ab-initio simulations and basic physical models. An overall conclusion is that Cu/low-k systems are likely to continue to be the mainstream technology for CMOS for several more ITRS nodes. Surprisingly, the more exotic technologies do not appear to offer significant performance improvements and, in fact, are sometimes inferior in terms of interconnect dimensions.



Voltage Pinning Distances for Various Cu Line Widths

MOSFET Channel Materialst

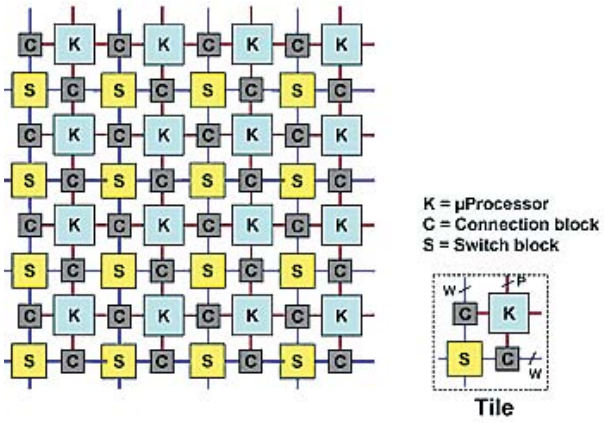
This study led to a counter-intuitive conclusion that as channel lengths approach five nanometers, it may be necessary for the mass of the information carrying particle (normally electrons) to substantially increase if scaling is to continue. The reason for this conclusion is that the heavier particles reduce the prospect for tunneling and over-barrier transitions. A window of opportunity exists for III-V channel materials from about 25 nanometers to 10 nanometers channel lengths.



I_{on}/I_{off} (estimated) vs. Gate Length, L_g, for various masses of information-bearing particles

Many-core Architectures

This study sought to determine whether there are advantages in terms of reliability and energy consumption to placing literally thousands of elementary processors together with a switching fabric and associated memory on a single chip. The study concluded that there may be gains in these areas relative to a large single CPU but they are probably less than one order of magnitude, if it assumed that all elementary processors are active. It was recognized that the problem of programming a massive array of processors to exploit potential parallelism for general computation has not been satisfactorily resolved.



General Structure for a Programmable Processor Array

SRC's subsidiary, Microelectronics Advanced Research Corporation (MARCO), jointly supported by DARPA, funds and operates five university-based research centers in microelectronics technology. Its charter initiative, the Focus Center Research Program (FCRP), is designed to expand pre-competitive, cooperative, long-range applied microelectronics research at U.S. universities in those technical areas that are critical to maintaining industry growth in the United States as well as meet defense needs.

FCRP Snapshot of 2006

- *1,558 Technical Documents*
- *579 Students*
- *1,655 Event Attendees*
- *7 New Patents in Portfolio*
- *51 Inventor Recognition Awards*

GSRC

The University of California/Berkeley is the lead university for the Gigascale Systems Research Center (GSRC). The Center's research agenda focuses on pertinent problems the semiconductor industry faces in the next decade in the areas of system design, integration, test, and verification. To sustain current growth, the industry requires orders of magnitude of improvement in energy efficiency, cost, reliability, and time-to-market.

To address the multiple challenges within this focus, the Center is structured along nine interlocking research themes, each led by a theme leader. The horizontal themes, Heterogeneous System Design and Integration and Soft Systems, represent two visions on how integrated systems are to be realized. A new horizontal theme, Microarchitecture, has been initiated jointly with the C2S2 Focus Center. These horizontal themes are combined with four vertical themes, each addressing one particular aspect of embedded integrated system design. The Power-Aware Systems, Reliable Systems, System Verification, and Embedded Self-Test themes, respectively, address the power and energy, reliability, verification, and test roadblocks that are looming on the horizon. Finally, the System-Level Living Roadmap provides an environment to explore how the different cost metrics of design will evolve in the next decade, taking a system-level view. This high-level perspective is unique and complements, as well as builds, on top of the existing roadmapping efforts. These efforts, which encompass and integrate all the research activities of the Center, are essential in identifying emerging challenges and in steering the research evolution of the Center.

Key contributions from GSRC research are described below:

- *Parallel Computing*

  GSRC has pushed the state-of-the-art in compilers by developing the Impact compiler which significantly improves the automatic exposure and execution of course-grain parallelism in standard C code. This research is expected to have significant impact on the optimization of future multicore applications. (University of Illinois/Urbana-Champaign)

  GSRC has launched the RAMP platform, an array of FPGAs programmed to emulate large multicore processors, with up to 1000 cores. RAMP is being distributed across the research community to enable advanced multicore software design (University of California/Berkeley).

- *Heterogeneous Design*

  GSRC researchers have released a framework (Metropolis) along with tool prototypes that implement a new design paradigm that enables efficient heterogeneous design. A number of sponsor companies as well as the DoD are experimenting with Metropolis for their next designs. (University of California/Berkeley)

- *Power Efficient Design*

  GSRC has explored the limits of power per instruction by prototyping a low energy sub-threshold processor (the Subliminal Processor) that only draws 3 pJ per instruction. The next iteration of this design, scheduled for fabrication next year, will draw only .5pJ and can operate for 41 years on a single, 1gram, Li-ion battery. (Pennsylvania State University)

- *Variability and Decreasing Reliability*

  GSRC researchers are exploring a variety of design approaches intended to overcome the reliability and variability issues associated with future nanoscaled devices. In particular, a project called "Bulletproof" is underway to address the need for reliable, correct and consistent system operability despite the reduced reliability of future transistors. To date, the Bulletproof team has specified a unified model of faults one can expect in future systems due to future transistor realities. This model represents a new level of fidelity in architectural-level fault analysis. (University of Michigan, and University of Texas/Austin)

- *Automatic Test*

  The GSRC has conducted a broad portfolio of research into design verification, automatic test, post silicon validation and system level test. A number of significant advances have been realized. For example, GSRC researchers have demonstrated alternate test solutions for high speed I/O and RF components. Testing these components is typically very expensive. The GSRC approach reduces the test time for components with Bit Error Rates of 10^{-12} or less by an order of magnitude, greatly reducing testing cost. (University of California/Santa Barbara)

C2S2

The Focus Center for Circuits and Systems Solutions (C2S2) is led by Carnegie Mellon University. The Center aims to develop new circuit design techniques needed to convert novel devices into robust performance across a diverse range of applications.

Relentless scaling of semiconductor devices toward fundamental physical limits threatens to make today's most basic circuit design assumptions obsolete. The current landscape of familiar trade-offs (area, speed, power, frequency, noise, reliability, linearity, yield, and cost) is shifting radically. To build tomorrow's complex, integrated, heterogeneous systems, the industry requires a foundation of circuit designs it can trust.

Circuits play a unique role in the "food chain" from materials to gigahertz. They hide the physics from designers; they form the most basic system-building blocks and they provide the essential traction for handling billions of competing system implementation details.

C2S2 research invents the new design techniques necessary to convert near-limit scaled devices and post-silicon devices into useful system-building blocks. It targets these design innovations across diverse design domains—digital, analog, RF, photonic, and MEMS designs.

Research in the C2S2 provides the needed link between devices and system design.

Key contributions from C2S2 research are described below:

- *Power Efficient Design*

  C2S2 has developed the Razor design approach in which design margins are rolled back until errors begin to occur and specialized circuitry is introduced to correct these errors. Substantial power reduction (up to 40%) is achieved. This technology has been transferred to the FCRP sponsors, where it is finding significant traction. (University of Michigan)

- *Variability and Decreasing Reliability*

  C2S2 has created a tool flow that implements a new design paradigm that is likely to save the semiconductor industry billions of dollars. By reducing design libraries to a small number of configurable regular logic bricks, extremely geometrically regular designs can be specified which reduce effective gate length variation. In 2006, 65nm implementation of a regularized circuit fabric on an ARM9 microprocessor core design resulted in 45% reduction in A Cross-chip Linewidth Variation (ACLV) using the same footprint as a std. cell ARM9. (Carnegie Mellon University)

- *Analog Circuit Scaling*

  C2S2 pioneered the use of comparator-based switched capacitor circuits as alternatives to operational amplifiers which do not scale well in CMOS. This research is likely to have significant impact on analog circuit design, allowing it to better scale in synchronism with Moore's law. (Massachusetts Institute of Technology)

  C2S2 has developed an "almost digital" radio in which almost all of the circuitry is digital. The design scales with processes below 65nm and exploits process variation. (Massachusetts Institute of Technology)

- *Mixed Signal Design*

  C2S2 has demonstrated tunable RF Micro-Electro-Mechanical circuitry that enables the integration of multiple radios into a single cognitive radio design. (Carnegie Mellon University)

- *Microarchitecture*

  GSRC and C2S2 researchers are developing novel, on-chip diagnosis circuitry designed to detect transient problems due to device performance variability and noise. These circuits feed information to compensation circuitry. Some of their high resolution sampling circuitry has been deployed in the latest Itanium processor. (Stanford University)

IFC

The Interconnect Focus Center (IFC) is led by the Georgia Institute of Technology. This Center conducts research to discover and invent new electrical, optical, and thermal solutions for interconnect systems that will meet or exceed ITRS projections and enable hyper-integration of heterogeneous components for future terascale systems.

The Center focuses on research on all aspects of the wiring that connects the millions of transistors on a microchip, from process to system-level architecture. IFC strives to stay atop all advances in diverse application areas and to play a major role in driving this technology into the future. To that end, the Center's research themes have evolved to accommodate this goal.

Key contributions from IFC research are described below:

- *Thermal Design*

  IFC is investigating the use of carbon nanotubes (CNT) as thermal vias that can be implanted in chips to help cool hot spots; a serious problem in next generation high density designs. In 2006, prototype vias were constructed. (Georgia Institute of Technology)

  IFC performed first measurements of interface resistances between aligned carbon nanotube nanostructured materials and silicon (chip) and metallization. CNT thermal conductivities > 70 W/mK were obtained; an encouraging result for future heat exchanger materials. (Stanford University)

- *High Speed, Low Power Interconnect*

  IFC researchers have conducted a comprehensive analysis of future candidate interconnect technologies to determine their relative potential. They have mapped out where copper, photonics, nanotubes and nanowires are likely to find applicability. This research has helped to focus the interconnect community on important research for the future. (Stanford University)

  IFC researchers have helped discover a new Si-compatible optical modulation approach which exploits the quantum confined stark effect in Germanium quantum wells. This breakthrough promises to significantly reduce the cost of performing on chip signal modulation in future CMOS designs. (Stanford University)

- *Microarchitecture*

  IFC researchers have released a suite of 3D design tools for integrated systems that are being used by sponsor companies to explore the potential of 3D design. (Massachusetts Institute of Technology)

MSD

Materials and devices research is conducted by the Center for Materials, Structures and Devices (MSD) at the Massachusetts Institute of Technology. Its focus is to explore and determine the most promising path for microelectronics in the next two to three decades by pursuing two overlapping approaches: scaling of CMOS to its ultimate limit and interdisciplinary exploration of new-frontier devices.

Since its inception in 2000, the MSD Center has successfully launched entirely new material combinations for high performance CMOS applications while pushing new frontier devices, such as carbon nanotubes, to new heights of performance through the combination of novel chemical synthesis of nanostructures with advanced front-end processes borrowed from silicon technology. In addition, the MSD Center is well along its way to establishing realistic benchmarking comparisons of highly disparate devices via close collaboration of experimentalists from different disciplines with advanced modeling and simulation researchers.

Research in this Center is organized into five research themes. Four of the themes concentrate on experimental research in device technology while the fifth collaborates with the other four in addressing key process and device issues by advanced modeling and simulations.

Key contributions from MSD research are described below

- *High Carrier Velocity*

  Strain has been adopted by the industry as an effective way to significantly increase carrier velocity in semiconductors. MSD researchers have shown how to maximize the impact of strain in bulk, on insulator and in multi-gate semiconductor designs. This research has been transferred to nearer term

research programs where it continues to have a major impact on the semiconductor industry. In 2006, researchers conducted the most complete study to date of the thickness dependence of the mobility in thin-body biaxially strained MOSFETs. (Massachusetts Institute of Technology)

MSD researchers are engaged in a comprehensive effort to improve the performance of nanoscale MOSFETS. Innovations have been introduced to help overcome transport, electrostatics, parasitics, gate leakage and gate depletion hurdles in future FET designs. A number of the sponsor companies have indicated that this research is having a profound impact on their preparation for future 32nm and beyond manufacturing processes. (Massachusetts Institute of Technology)

MSD researchers have fielded organic FETs near the molecular limits of such devices that enable research into the transport mechanisms in single molecule FETS. This research paves the way for the development of techniques required for the realization of molecular scale devices. (University of California/Berkeley)

Low Energy, Small Footprint Memory

MSD researchers have developed a way to convert DRAM to SRAM using a compact negative differential resistance device. (Stanford University)

MSD and FENA researchers fabricated and demonstrated an ultra-dense moletronic memory array (160K bits, 1011 bits/cm_2) using the Rotoxane molecule as switches and 2-dimensional arrays of nanowires as interconnects. (California Institute of Technology and the University of California/Los Angeles)

Simulation and Modeling

MSD has developed a MOSFET scattering model that enables the prediction of the performance of different channel materials such as new semiconductor materials, carbon nanotubes and molecular wires. This model has become a standard for the quantitative benchmarking of new materials and structures. (Purdue University)

FENA

Research in nano materials is conducted by the newest focus center on Functional Engineered Nano Architectonics (FENA). The Center's research is directed at resolving the cross-cutting materials and device challenges related to beyond-CMOS technologies in order to create new information processing paradigms with greater capabilities.

In order to tackle major challenges common to all nanometer scale devices, new nanoscale materials and processes are needed to address the core problems of nanoscale technology. Opportunities exist for creating a new generation of nanoscale materials, structures, and devices, which will extend semiconductor technology to CMOS limits and beyond, and provide heterogeneous interfaces of new nanosystems, enabling a combination of molecular and biological functions that lead to new paradigms of information processing and sensing. Through this new generation of nanostructured materials, the semiconductor industry will continue to expand and create new applications of monolithically integrated (CMOS, molecular, and biomolecular) nanosystems. FENA focuses on the materials challenges at the nanoscale for fulfilling these opportunities.

Key contributions from FENA research are described below:

Low Energy, Small Footprint Memory

FENA researchers have conducted a comprehensive study of emerging research memory devices to help prioritize research on the approaches showing the most potential. (University of California/Los Angeles)

Self Assembly

FENA researchers continue to investigate bio-assisted self-assembly techniques in which PNA/DNA and viruses are used to direct the assembly of nanoscale components. In 2006, the use of Peptide Nucleic Acid (PNA) to self-assemble single-walled carbon nanotube structures was demonstrated. (University of California/Riverside)

Beyond CMOS Componentry

A large body of research is underway across all five FCRP centers on CNTs. Results of particular significance are:

1) MSD researchers have demonstrated n- and p- doped CNT FETs that exhibit extremely good symmetrical performance, making them excellent candidates for future CMOS implementation. (Stanford University)

2) FENA researchers have shown that CNT growth can be controlled by using sapphire molecular lattices as templates. (University of Southern California)

The goal of the NRI is to demonstrate novel computing devices capable of replacing the CMOS transistor as a logic switch in the 2020 time frame. These devices should show significant advantage over ultimate CMOS transistors in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology. To meet these goals, NRI is focused primarily on research on devices utilizing new computational state variables beyond electronic charge. In addition, NRI is interested in new interconnect technologies and novel circuits and architectures, including non-equilibrium systems, for exploiting these devices, as well as improved nanoscale thermal management and novel materials and fabrication methods for these structures and circuits. Finally, it is critical that these technologies be capable of integration with CMOS, to allow exploitation of their potentially complementary functionality in heterogeneous systems, and to enable a smooth transition to a new scaling path.

Early in 2006 NRI initiated research programs at over 20 universities across the country, organized into virtual centers. The key objectives for 2006 were to complete organization of these centers, launch research programs at the centers on topics of interest to NRI, and to establish an effective framework for delivering results back to member companies.

Three main NRI centers have been established, with universities grouped largely by geography. While all of the centers are working on research aimed at finding a new logic switch, the focus of the programs at each center has its own specific character:

The Western Institute of Nanoelectronics (WIN) in California was the first center to be established at the beginning of 2006. Headquartered at the University of California/Los Angeles Henry Samueli School of Engineering and Applied Science, WIN participants come from three University of California campuses (Los Angeles, Berkeley, and Santa Barbara) and Stanford University. WIN focuses solely on spintronics and related phenomena, extending from material, devices, and device-device interaction all the way to circuits and architectures. In addition to its NRI funding, this center receives additional direct support from Intel and the University of California Discovery Program.

The Institute for Nanoelectronics Discovery and Exploration (INDEX) was established in the second quarter of 2006. Headquartered at the College of Nanoscale Science and Engineering of the State University of New York/Albany, it also includes the Georgia Institute of Technology, Harvard University, Massachusetts Institute of Technology, Purdue University, Rensselaer Polytechnic Institute, and Yale University. INDEX focuses on the development of nanomaterial systems; atomic-scale fabrication technologies; predictive modeling protocols for devices, subsystems and systems; power dissipation management designs; and realistic architectural integration schemes for realizing novel magnetic and molecular quantum devices. INDEX also receives additional direct support from IBM and New York State.

The South West Academy for Nanoelectronics (SWAN) in Texas is the newest of the centers, established in the third quarter of 2006. Headquartered at the Microelectronics Research Center at the University of Texas/Austin, it includes a collective team from the University of Texas/Dallas, Texas A&M University, Rice University, Notre Dame University, Arizona State University, and the University of Maryland. SWAN focuses on a variety of new devices, including spin-based switches, nanowires, nano-magnets, and devices which use electron wave or phase interference. In addition, work is being done on modeling; novel interconnects, such as plasmonics, and nano-metrology techniques. SWAN also received additional support from Texas Instruments and the Texas Emerging Technology Fund.

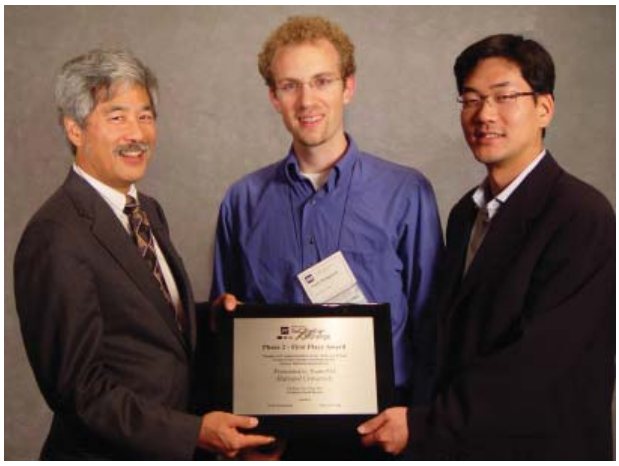
In addition to these centers, NRI joined forces with the National Science Foundation (NSF) and solicited proposals in 2005 from existing NSF nanoscience centers for supplemental funding of NRI-related activities at these centers. Six centers were selected and are jointly funded by NSF and NRI beginning 2006 The goal in making this joint investment with NSF is not only to complement the work in the NRI centers, but also to leverage the research in the NSF centers in a symbiotic manner. The NRI program gains from the knowledge created in the NSF centers and the NSF centers gain from the industry involvement through NRI. This joint program has been so successful that NSF and NRI solicited another round of proposals in the fall of 2006, and intends to fund another set of NSF centers in 2007.

Given the exploratory nature of much of the NRI research as it seeks out entirely new device and computation technologies, it is particularly important that industry and academia work closely as the research paths develop. Each NRI center has an Executive Committee, comprising the center lead professors and representatives from the member companies, which meets regularly to discuss the technical progress in the center as well as logistical issues. For each NRI-NSF project at the NSF centers, an industrial liaison team comprised of members from all participating companies has been established. These teams made on-site visits to all six NSF centers early in 2006, to understand the research in-depth and to give guidance from the industry. They will continue to be actively engaged throughout the three year project cycle. Lastly, NRI has established an industry assignee program, where employees of the member companies work directly at one of the NRI university centers. These assignees participate on behalf of NRI, to assist the center directors in the technical integration of the research programs and to be active participants in specific research projects at the center. At the end of 2006 there was one NRI assignee at the WIN center and two at INDEX, with six or more assignees expected in 2007. This high-level of industry-university interaction is expected to efficiently guide the research in the most promising directions while simultaneously maximizing the ability of the member companies to harvest early research results as they are produced.

The first NRI Annual Review was held in San Francisco, California on November 16-17, 2006. The review was attended by about 100 people from all of the NRI centers, member companies, and government agencies. This was the first opportunity to review in detail all of the NRI research programs. The attendees gave overwhelmingly positive feedback on the review, and were particularly impressed with how quickly the projects had ramped up in a short amount of time and with relatively modest initial resources. The diversity and quality of projects in both the primary NRI centers, as well as the NRI research in the NSF centers, were seen as creating a robust research portfolio, well-positioned to achieve the NRI goals in the coming years.

Nearly 1,000 students participated in GRC funded research in 2006; over 500 participated in FCRP funded research. Of students graduating in 2006, 60% of both GRC and FCRP graduates accepted employment in member organizations or are pursuing advanced degrees. Other 2006 accomplishments included:

- Eight new Company-Named Fellowships and the first GRC/John L. Prince Fellowship were awarded through the GRC Graduate Fellowship Program to bring the number of Fellows at the beginning of the 2006 fall term to 38. Ten GRC Fellows graduated in 2006.
- Nine new Company-Named GRC Master's Scholarships were awarded, for a total of 15 at the beginning of the 2006 fall term. 14 Master's Scholars graduated in 2006.
- 141 GRC students presented their research at the SRC Student Symposium 2006 in Cary, North Carolina
- 646 individual resumes were published on the GRC Web site, another 241 on the FCRP Web site.
- The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars. A copy may be obtained by contacting SRC Student Relations at the SRC corporate address.
- The sixth Simon Karecki Award was made from the Simon Karecki Fellowship Fund to Rong Chen, Stanford University. This award recognizes outstanding student performance through the GRC/NSF Center for Environmentally Benign Semiconductor Manufacturing, centered at the University of Arizona.
- FCRP student/industry networking events were held in conjunction with the annual research reviews for the FENA, C2S2, MSD, IFC, and GSRC Focus Centers.
- TechConnects for GRC students, that provide an opportunity for direct student interactions with member companies, were held at the University of Arizona, the University of California/Santa Barbara, and the University at Albany/SUNY.
- Phase 2 of the SRC/SIA SoC Design Challenge culminated at the SRC Student Symposium in the presentation of awards for first, second and third place to research teams from Harvard, the University of Virginia, and Michigan State University, respectively. The first place award was presented by Daryl Hatano, SIA VP for Public Policy, to Mark Hempstead and Professor Gu-Yeon Wei from Harvard University for their entry "Design and Implementation of an Ultra-Low-Power, Event-Driven System Architecture for Sensor Network Applications."



(l-r) Daryl Hatano, Mark Hempstead and Prof. Gu-Yeon Wei

SRC Education Alliance

The Undergraduate Research Assistants Program (URA) is managed through the SRCEA with funding from the Department of Defense, MARCO and SRC. The URA Program targets academically qualified students early in their undergraduate careers and seeks to build their enthusiasm for disciplines of interest to the semiconductor industry.

Thirty-nine students at 20 universities participated in the URA program in 2006. Six students completed the program and all continued to graduate school. Twenty-four students were in the program at the beginning of the Fall 2006 term.

Following the recommendation of the Student Relations-Technical Advisory Board and Value Chain-Technical Advisory Board, an all new student event, SRC Student Symposium 2006, was established. This conference was designed to take place during the year that SRC does not conduct TECHCON. The objective of this conference was to provide a cost-effective student/industry networking event with outstanding technical presentations by students, combined with ample opportunities for research discussions, and interaction between students and industry participants.

Symposium attendees, industry and students alike, agreed that the first SRC Student Symposium was a resounding success. Technical presentations by students and the ample networking opportunities made the Symposium an outstanding event. The Symposium, sponsored by eight SRC member companies, was held in Cary, North Carolina on October 9-10, 2006.

SRC students presented 128 papers in 16 sessions over a two-day period, including four papers from the Focus Center Research Program. In addition, 13 Fellows and Scholars presented posters. Best in Session Awards were presented after the Symposium to winners in each of the 16 sessions. The annual Fellows Award for Outstanding Research Presentation was presented to David Kelly, TI/SRC Fellow at the University of Texas/Austin.

David Benson (right), the current Robert M. Burger Fellow, and Dr. Burger, SRC

A highlight of the Symposium was the keynote speech at the banquet on Monday evening by Dr. Hans Stork, Texas Instruments' Senior Vice President and Chief Technology Officer and Chair of the SRC Board of Directors. The banquet also included presentation of the 2006 Aristotle Award to Professor Mark Law, University of Florida, and presentation of awards to the winners of the SRC/SIA System-on-Chip Design Challenge. The 2006 Mahboob Khan Mentor Awards were also presented to industry liaisons. (See following page for award details).

Symposium Sponsors

AMD

APPLIED MATERIALS

freescale™ semiconductor

IBM

intel

Mentor Graphics

NOVELLUS

Texas Instruments

Prof. Mark Law with SRC students Diane Hickey (l) and Leah Edelman (r)

Aristotle Award

The 2006 Aristotle Award was presented to Professor Mark Law, University of Florida, at the SRC Student Symposium 2006 in October. The Aristotle Award recognizes GRC-supported faculty whose deep commitment to the educational experience of GRC students has had a profound and continuing impact for GRC members over a long period of time. The award acknowledges outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project.

Mahboob Khan Award

The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time GRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as Industrial Liaisons. Recipients represent "ideal mentors" whose commitment more than enhances the GRC research program.

The 2006 award recipients were:

Ken Butler of Texas Instruments has guided an effective research program with Dr. Rob Daasch at Portland State University and Professor Mohammad Tehranipoor at The University of Connecticut. According to Dr. Tehranipoor, Dr. Butler has a special "ability to visualize a problem and derive solutions that are both innovative and practical." Rob Daasch notes that he "knows how to strike the balance between an unfettered pursuit of knowledge and a significant research problem facing the semiconductor industry."

Robert Gauthier of IBM's Semiconductor Research and Development Center in Essex Junction, was nominated by fellow employee Peter Cottrell. Dr. Cottrell indicates that Dr. Gauthier has developed a relationship with Elyse Rosenbaum and her students at the University of Illinois/Urbana-Champaign. Over the past years, several students have interned at IBM under Dr. Gauthier's direction; students note that his encouragement during the internship resulted in successful completion of academic goals.

Larry Gochberg of Novellus has served as an Industrial Liaison to Professor Mark Kushner for his tasks on plasma equipment and process, both at the University of Illinois/Urbana-Champaign and now at Iowa State University. According to the nominator, John Kelly of Novellus, Dr. Gochberg is known for "providing advice and encouragement and freely sharing his perspective on technology development from a diverse career including the semiconductor and aerospace industries."

Zoran Krivokapic of Advanced Micro Devices has worked with Professors T. P. Ma, Charles Ahn, and their student Xia Hong at Yale University. Xia Hong said that Dr. Krivokapic makes visits to Yale once or twice a year and has an "in-depth discussion with each student, reviewing various aspects of his research project." Mr. Hong continues, "his knowledge of the state-of-the-art in semiconductor devices and processing, ... and his inspiring suggestions regarding new materials to study and novel device structures, have led to new research directions."

Jim Libous and Dan O'Connor of IBM initially recruited Principal Investigator Dr. Madhavan Swaminathan of Georgia Institute of Technology in 1999, and have mentored him and his students continuously. They have arranged numerous summer internships and made many visits to Georgia Institute of Technology to meet and consult with the professor and students.

Sani Nassif of IBM was nominated by Professor Malgorzata Marik-Sadowska at the University of California /Santa Barbara for his "vision and genuine talent in selecting research problems that blend practical considerations with theoretical significance." Former student, Dr. Kai Wang, wrote that Dr. Nassif was his manager during a summer internship, and served on his doctoral committee. According to Wang, "Dr. Nassif's vision and industrial perspective provided invaluable suggestions and insightful comments" to the successful completion of his academic program.

(l-r) Dan O'Connor, Jim Libous, Larry Gochberg and Robert Gauthier

Technical Excellence Award

The GRC Technical Excellence Award is given annually to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research. They are groundbreakers and leaders in their fields and are regarded as model collaborators with their colleagues in the GRC member community. The 2006 award was presented at the SRC Board of Director's Meeting in San Jose, California by the Board Chairman, Dr. Hans Stork of Texas Instruments.

Professor Gennady Gildenblat and his student Weimin Wu of Arizona State University received the award for work that some say has revolutionized MOSFET Modeling. The work was recently selected as the next standard compact MOSFET model by the Compact Model Council. According to nominator, Colin McAndrews of Freescale Semiconductor, "Dr. Gildenblat has assiduously leveraged industrial partners to make sure his model solves real problems. Apart from Berkeley Short-channel IGFET Model (BSIM), his model is the most successful work funded by GRC in terms of making its way into simulators and being used by, and having an impact on the industry."

Prof. Gennady Gildenblat

Weimin Wu

Intellectual Property (IP) assets emerging from SRC-sponsored university research programs are provided by SRC to its members to protect and enhance the value of SRC membership. IP assets support SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs by SRC member companies. SRC's significant portfolio of intellectual assets minimizes the risk of infringement and encumbrances as research results are used by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship.

SRC receives non-exclusive, worldwide, royalty free licenses to IP from university research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results may be investigated, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights to provide a level playing field for members by ensuring that those who use SRC-sponsored technologies do so only within the scope of a valid license. SRC seeks to ensure that members receive and benefit from all IP rights from SRC research to which they are entitled.

SRC continually investigates ways in which IP assets can provide new and additional sources of value to the SRC member community. Recently, GRC pioneered an innovative joint licensing and commercialization partnership focused on commercializing selected inventions in specific technology areas, in an effort to build a themed IP portfolio. The Exclusive Licensing Model has received strong support from several universities and member companies. This new program benefits GRC members by increasing their potential competitive advantages, while also providing for a possible new source of royalties. Under this new licensing model, select GRC and university IP rights are combined and licensed to SRC. The formerly separate IP rights have greater value once combined in an escrow managed by SRC. As a result, enhanced commercialization prospects and greater licensing value can be provided as compared with the traditional SRC-university licensing model.

During 2006, 16 GRC-sponsored U.S. and foreign patents issued, bringing the portfolio of SRC and GRC patents to 270. This significant patent portfolio supports both U.S. and international member company operations in numerous countries around the world. GRC's web site permits members to submit real time queries in the IP database to obtain status on pending and issued patents as well as information on GRC sponsored software.

GRC's IP portfolio provides over 518 software programs, software models, and technical databases to member companies. Software and database licenses from GRC-sponsored research programs represent a growing and complementary part of the SRC IP portfolio. SRC members receive non-exclusive, worldwide, royalty-free intellectual property licenses to applicable software programs and technical databases.

GRC United States Patents issued in 2006 include 7,129,734 to Geiger, Chen, Jin, Kuyel, and Parthasarathy, "A Method for Testing Analog and Mixed-Signal Circuits Using Functionally Related Excitations and Functionally Related Measurements" (Iowa State University, Texas Instruments); 7,149,999 to Gupta, Sylvester, Yang, and Kahng, "Method for Correcting a Mask Design Layout" (University of California/San Diego, University of Michigan); 7,096,174 to Pileggi

and Beattie, "System, Methods and Computer Program for Creating Hierarchical Equivalent Circuit Models" (Carnegie Mellon University); 7,151,632 to Brown, Biss, and Youngworth, "Inhomogeneous Polarized Optical Beam for Use in Illumination and a Method Thereof" (University of Rochester); 7,030,997 to Robins, Gennari, Neureuther, and Adam, "Characterizing Aberrations in an Imaging Lens and Applications to Visual Testing and Integrated Circuits Mask Analysis" (University of California/Berkeley); 7,015,546, to Herr and Zhirnov, "Deterministically Doped Field Effect Devices and Methods of Making Same" (SRC, North Carolina State University); 7,075,699 to Chen and Oldham, "Double Hidden Flexure Microactuator for Phase Mirror Array" (University of California/Berkeley); 7,141,858 to Hu, King, and Polishchuk, "Dual Work Function CMOS Gate Technology Based on Metal Interdiffusion" (University of California/Berkeley); 7,092,138 to Solgaard, Jung, and Wang, "Elastomer Spatial Light Modulators for Extreme Ultraviolet Lithography" (Stanford University); 7,110,420 to Cavin, Liu, and Bashirullah, "Integrated Circuits Devices Having On-Chip Adaptive Bandwidth Buses and Related Materials" (SRC, North Carolina State University); 7,144,803 to Junker, Ekerdt, Sun, and Engbrecht, "Method of Forming Boron Carbo-Nitride Layers for Integrated Circuit Devices" (University of Texas/Austin, Motorola); 7,155,698 to Gennari, "Method of Locating Areas in Mask Layout that are Sensitive to Residual Processing Effects" (University of California/Berkeley); 7,078,817 to Ho, Lee, Ogawa, and Matsuhashi, "Multiple Copper Vias for Integrated Circuit Metallization" (University of Texas/Austin); 7,081,674 to Ganapathiraman and Ramanath, "Polyelectrolyte Nanolayers as Diffusion Barriers in Semiconductor Devices" (Rensselaer Polytechnic Institute) 7,026,716 to Ganapathiraman and Ramanath, "Self-Assembled Sub-Nanolayers as Interfacial Adhesion Enhancers and Diffusion Barriers for Integrated Circuits" (Rensselaer Polytechnic Institute); and 7,032,151, to Chatterjee and Halde, "Systems and Methods for Testing Integrated Circuits" (Georgia Institute of Technology).

During 2006, seven FCRP-sponsored U.S. patents were issued, bringing the portfolio of MARCO and FCRP patents to sixteen. FCRP's IP portfolio provides 16 software programs, software models, and technical databases to member companies. FCRP members receive non-exclusive, worldwide, royalty-free intellectual property licenses to applicable software programs and technical databases.

FCRP United States Patents issued in 2006 include 7,132,736 to Bakir, Martin, Meindl, and Patel, "Devices Having Compliant Wafer-Level Packages With Pillars and Methods of Fabrication" (Georgia Institute of Technology); 7,016,569 to Mule, Meindl, and Gaylord, "Back-Side-of-Die, Through-Wafer Guided-Wave Optical Clock Distribution Network, Methods of Fabrication Thereof, and Uses Thereof" (Georgia Institute of Technology); 7,099,525 to Martin, Meindl, and Bakir, "Dual-Mode/Function Optical and Electrical Interconnects, Methods of Fabrication Thereof, and Methods of Use Thereof" (Georgia Institute of Technology); 7,135,777 to Martin, Meindl, and Bakir, "Devices Having Compliant Wafer-Level Input/Output Interconnections and Packages Using Pillars and Methods of Fabrication Thereof" (University of California/San Diego, University of Michigan); 7,062,743 to Kahng, "Floor Plan Evaluation with Timing Driven Global Wire Planning, Pin Assignment, and Buffer/Wire Sizing" (University of California/San Diego); 7,064,055 to Reif, "Method of Forming a Multi-Layer Semiconductor Structure Having a Seam-Less Bonding Interface" (Massachusetts Institute of Technology); and 7,075,648 to Gaylord, Montarou, "Performing Retardation Measurements" (Georgia Institute of Technology).

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