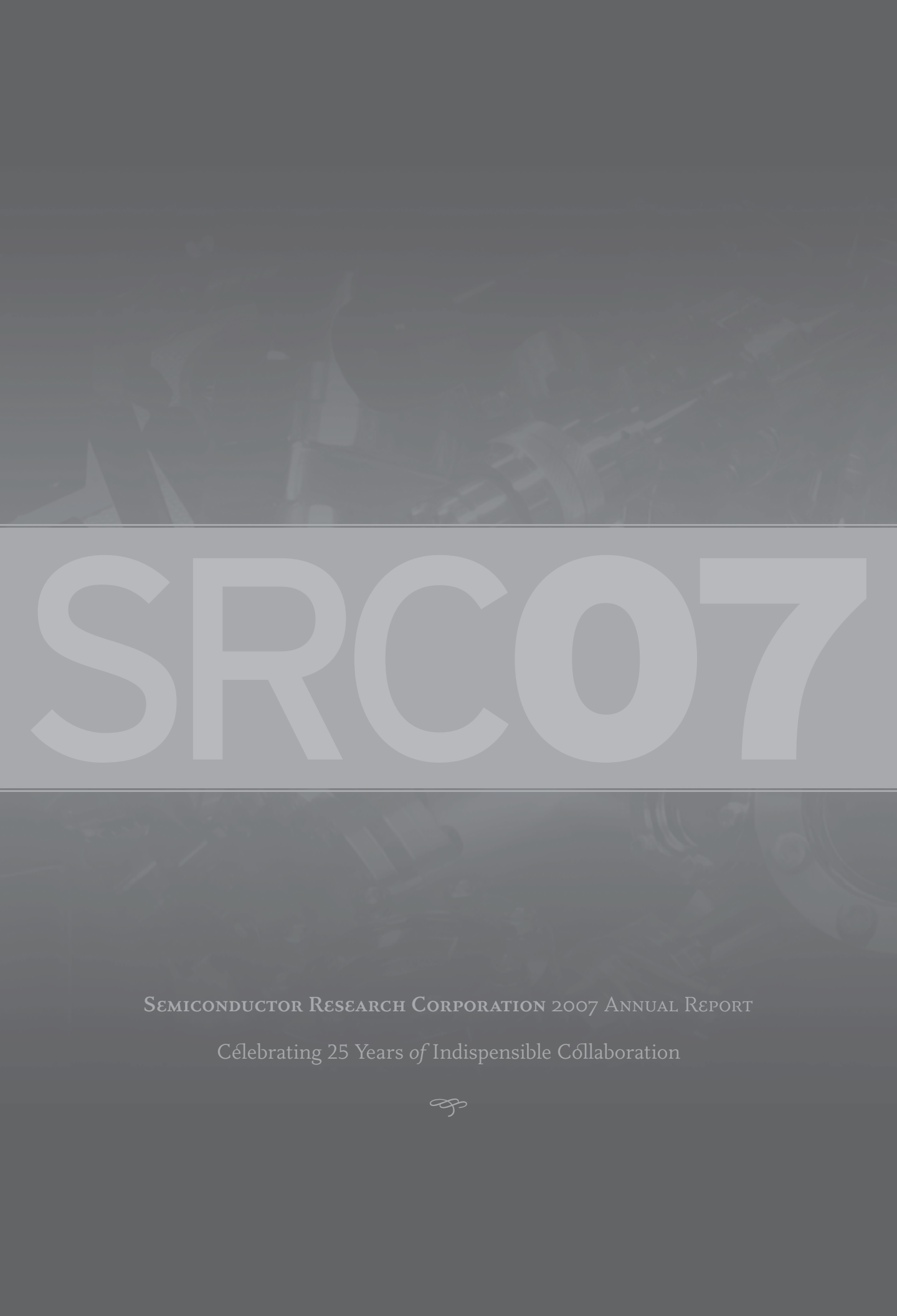
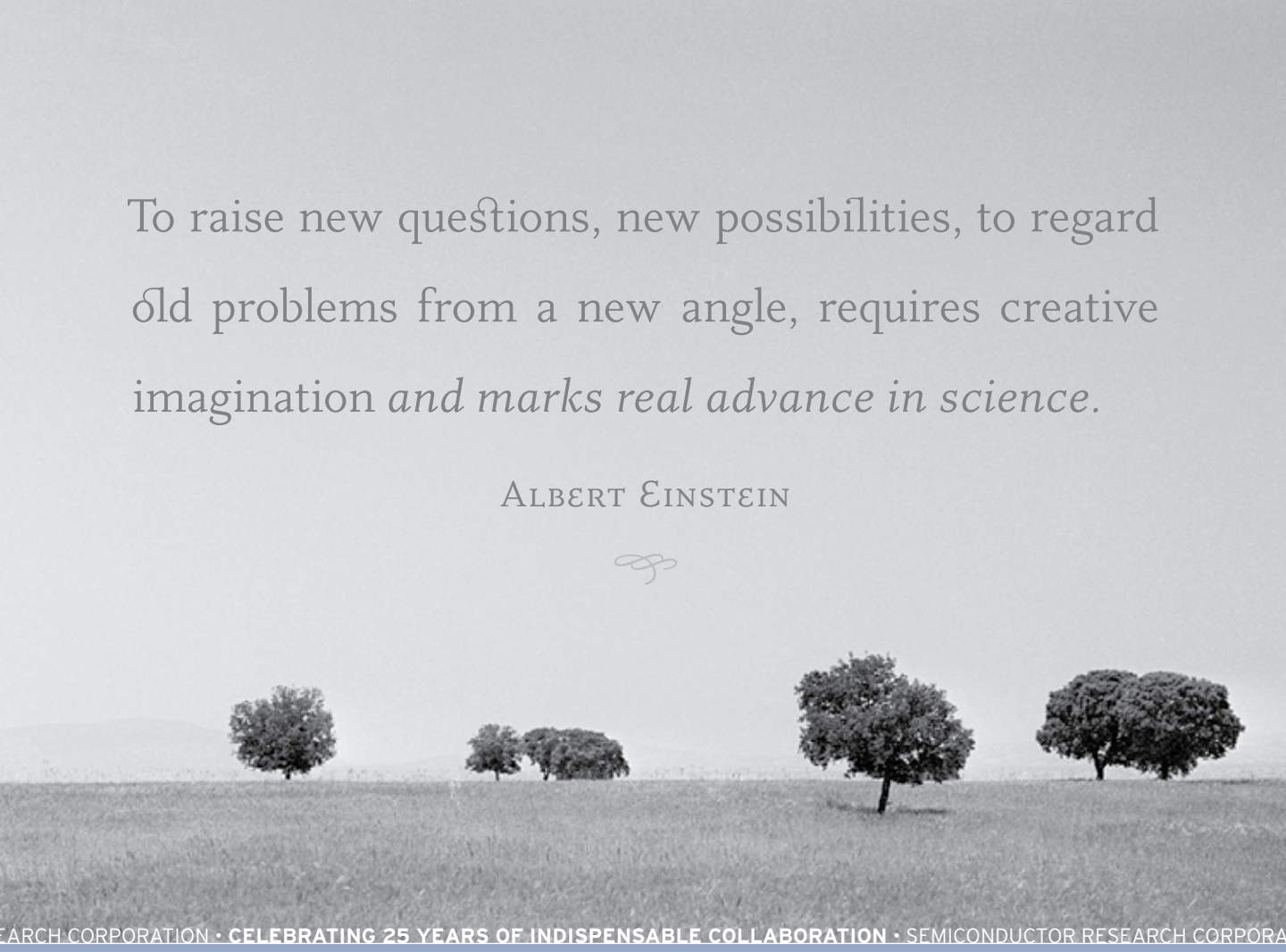


SRC07

Semiconductor Research Corporation 2007 Annual Report

Célebrating 25 Years *of* Indispensible Cóllaboration



EARCH CORPORATION • **CELEBRATING 25 YEARS OF INDISPENSABLE COLLABORATION** • SEMICONDUCTOR RESEARCH CORPORA

Semiconductor Research Corporation **2007 Annual Report**

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THE ANNUAL REPORT OF SEMICONDUCTOR RESEARCH CORPORATION IS published each year to summarize the directions and results of the SRC research program and provide information on activities and events of the SRC community for the previous calendar year.

A copy of this report and additional information about SRC are accessible online at www.src.org.

25 YEARS, **INDELIBLE ACHEIVEMENTS**

RESEARCH:

- $797M invested by SRC Members
- $427M total leveraged funding
  - › $88M directed – flows through SRC
  - › $146M collaborative – flows to SRC contracts
  - › $193M influenced – influences process and shares research results
- 2,786 contracts
- 6,976 students
- 1,598 faculty members
- 237 universities

OUTPUTS:

- 39,536 technical documents
- 302 patents in SRC portfolio
- 717 patent applications
- 597 inventor awards
- 555 software programs
- 2,127 tasks/themes in research catalog

A LETTER FROM **LARRY W. SUMNEY, PRESIDENT & CEO**

IN AN INDUSTRY WHOSE DEFINING CHARACTERISTIC is change, one constant is the need for discovery and innovation. SRC has been at the forefront of pre-competitive research on behalf of the semiconductor industry for over 25 years. Through close interactions with its members, SRC has been able to anticipate trends in generic research needs and implement university programs that have responded in a timely manner. Almost everywhere I go, I am met by a former SRC student – one of over 6500 who have been supported by SRC – who is making a key contribution to the enterprise that employs them.

We were especially gratified in 2007 to learn that SRC was chosen to receive the 2005 U.S. National Technology Medal, and we acknowledge the role of many thousands of outstanding industry, government and university participants who share ownership of this prestigious award with us. The citation reads: "…for building the world's largest and most successful university research force to support the rapid growth and advance of the semiconductor industry; for proving the concept of collaborative research as the first high-tech research consortium; and for creating the concept and methodology that evolved into the International Technology Roadmap for Semiconductors."

During 2007, SRC has steadily sought to comprehend long-term semiconductor industry directions and to create innovative programs whose outputs will contribute to pacing semiconductor industry technologies. In the Global Research Collaboration (GRC) program, SRC, in collaboration with Texas Instruments and the State of Texas, has formed a new research center in analog integrated circuits at the University of Texas, Dallas. This new center is created in recognition of the importance of analog integrated circuits in a broadening array of applications and the need for critical advances in design technology. In other areas, the joint industry-DARPA/DoD Focus Center Research Program (FCRP) has continued to provide advances across a broad array of technologies targeted at the end of ITRS scaling, and I am delighted that the SRC collaboration with its government partners has never been stronger. Moreover, the National Institute of Standards and Technology (NIST) has recently become a partner in the Nanoelectronics Research Initiative (NRI) that is seeking new information processing technologies to complement ultimately-scaled CMOS. NIST participation has enabled SRC to expand the existing NRI program and better address metrology needs in the far-nanometer regime.

The SRC Board of Directors provided decisive leadership in 2007, maintaining the strategic vision of SRC as an indispensable resource for the industry. For example, in order to provide a mechanism for SRC to respond to niche research interests outside the purview of its three primary research programs, the Board has authorized the formation of a new program entity called Topical Research Collaboration (TRC). This new flexibility should enable SRC to explore emerging areas that could become an important component of member company businesses in the future. A key feature is that companies that do not currently belong to GRC, FCRP or NRI can participate in various TRCs to assist in meeting research needs. On an even larger scale, the SRC Board members have continued to provide guidance on the future directions of this dynamic industry that are so critical to the successful execution of SRC research.

Looking ahead, we at SRC are excited about the opportunities that lay before us. We believe that the agility and flexibility that are an integral part of the SRC mindset will ideally position us to support our members' successes for the next 25 years.

Sincerely,

LARRY W. SUMNEY, *President & CEO*

HISTORY

Semiconductor Research Corporation (SRC) is proud to celebrate 25 years of indelible contribution to the semiconductor industry. SRC was founded on the premise that cooperative university research programs, which focus on pre-competitive semiconductor technologies and are sponsored by industry rivals, could raise the competitiveness of all participating companies. This postulate, radical when adopted in the early 1980s, has proven valid for the semiconductor industry, and SRC programs have produced a foundation of ideas and talented professionals throughout its twenty-five year history.

IMPACT

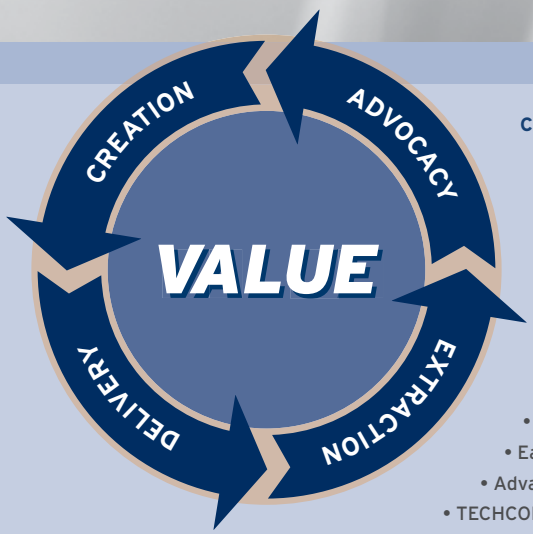
SRC offers a comprehensive value proposition. In addition to creating value, the SRC model and capabilities ensure value delivery through state-of-the-art, streamlined mechanisms. The SRC staff diligently collaborates with each member company to facilitate the maximum value extraction from SRC programs, and regularly engages stakeholders to continuously improve the value to its members. These principal efforts entail mechanisms to monitor and respond to the research needs of each member within the cooperative context; a capability to operate the research programs to be synergistic with a university's educational mission; and a focus on providing rapid access of research results to members.

With a professional staff recognized as leaders in their respective disciplines, SRC conducts three principal research programs on behalf of its member companies: Global Research Collaboration (GRC), which fosters direct member involvement in the research at many levels and emphasizes innovation in the CMOS technologies; Focus Center Research Program (FCRP), which is primarily university-directed and conducts research focused on the transition from Moore's Law scaling of CMOS to emerging technologies beyond CMOS; and Nanoelectronics Research Initiative (NRI), a discovery-research program seeking new information technologies that could sustain historical exponential growth in performance and reductions in cost per function.

THE FUTURE

SRC is poised to build upon its solid foundation and respond to the ever-changing needs within the dynamic semiconductor industry – an industry whose societal impact grows daily. As the industry rapidly expands and semiconductor technologies evolve, we will continue to enable the pace of progress.

As the impact of semiconductor technologies broadens, we are faced with new research opportunities – opportunities driven by imminent information systems requirements in biotechnology, energy, entertainment, transportation and many other areas. SRC stands ready. The agility and adaptability that are hallmarks of the SRC model position us well for the next twenty-five years.



SEMICONDUCTOR RESEARCH CORPORATION'S **VALUE PROPOSITION**

CREATION
- Member funding for full spectrum of semiconductor technologies
- Student programs, fellowships & scholarships
- Intellectual property *(grc.src.org/members/ref/legal/overview.asp)*

DELIVERY
- Delivery of research results to SRC members
- Effective website delivery of research results
- Networking
- e-Workshops
- Early access to publications & presentations
- Advanced awareness of graduating students
- TECHCON
- Forums

ADVOCACY
- Compelling reasons
- Return on investment (ROI)
- Continuous improvement

EXTRACTION
- Liaison program
- Member participation in Industrial Assignee Program
- Annual research reviews for all contracts

GLOBAL RESEARCH COLLABORATION

SRC Global Research Collaboration (GRC) is an indispensable part of the research and development strategies of the world's leading semiconductor companies. The program's unique operational model harnesses research from the world's top universities and converts it into an incomparable competitive advantage for SRC members.

In 2007 GRC continued efforts to expand its research portfolio to reflect the growing needs of the industry, specifically in the areas of technology scaling, novel systems and architectures, and robust design methodologies. Through the research of individual projects and centers involving collaborations of universities around the world, these topics continue to be explored and analyzed.

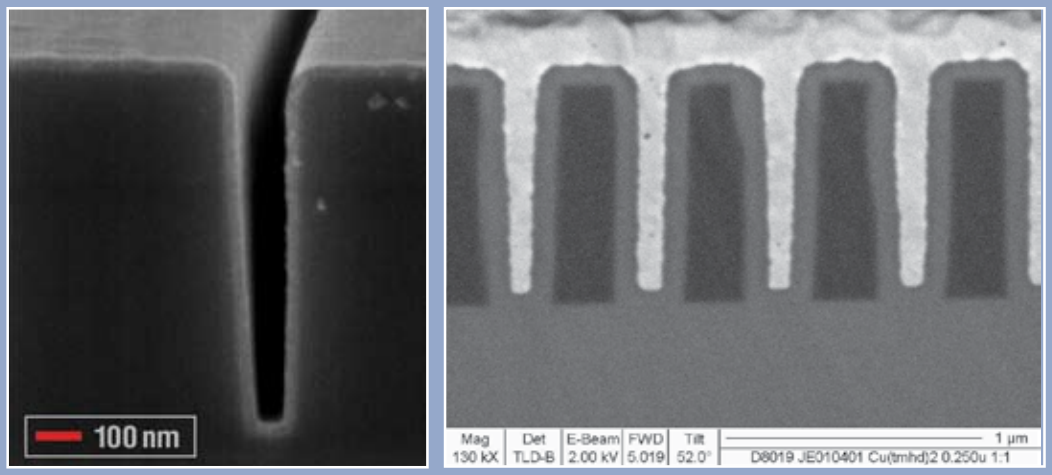
GRC funds projects in over 100 universities globally, with about 25% of these universities outside of the US. This year the Non-Classical Research Center (NCRC, formed in 2006 and led by the University of California-Santa Barbara), added the Glasgow University in Scotland to its research investigators. GRC also acquired a renewal from the State University of New York (SUNY) system, garnering three more years of leveraged support for a major research center.

RESEARCH FOCUS: TECHNOLOGY SCALING

SRC awarded the New York Center for Advanced Interconnect Science and Technology (CAIST) a three-year contract aimed at extending copper and low-k dielectric scaling. This essential center, managed by SUNY at Albany, will subcontract 27 new research projects on this topic with 14 top US universities. Interconnect scaling is one of the most important enablers for the continuation of Moore's Law beyond 2011. By providing chip companies with materials and methods for further extension of interconnect scaling, these projects will help to ensure that semiconductor chips grow smaller, faster and cheaper.

As a new expansion to the NCRC, University of Glasgow researchers will help identify the best p-channel material to scale the MOSFET minimum feature size, including gate length, down to the 8-nanometer technology generation. Exploiting compound semiconductor materials, progress expected from the Glasgow research will enable scaling of faster silicon chips for an additional four to six years beyond previous projections.

At the heart of this challenge is the MOSFET, the basic unit or switch in a silicon CMOS gate which is the basis for all silicon digital circuits. The industry has relied on reducing the MOSFET



Hafnia (left) and Cu (right) films deposited by SFD.

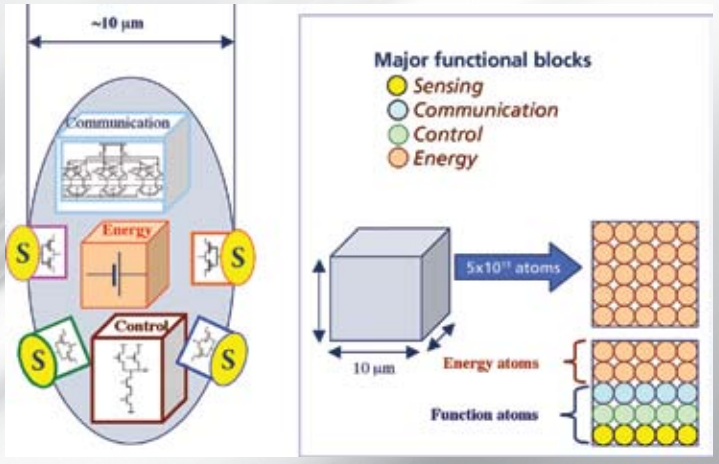
minimum feature size to support continued miniaturization of integrated circuits for many generations. To sustain progress, switching speed on the chips must continue to increase. The International Technology Roadmap for Semiconductors (ITRS) requires a solution that will provide more rapid switching for turning various transistors on and off as they send signals throughout the chip.

A critical challenge facing semiconductor nanofabrication technology is the ability to deposit conformal, defect-free metal and metal oxide films over complex 3D nanoarchitectures. Conformal depositions on high aspect ratio features are required to enable scaled nanodevices for advanced computing and memory, and for realizing new capabilities in supercapacitors, sensors and other applications. The National Science Foundation-sponsored Nanoscale Science and Engineering Center for Hierarchical Manufacturing, in synergistic partnership with SRC, is developing enabling strategies for the deposition of metals and metal oxides on or within complex device structures using supercritical fluid deposition (SFD). This technique offers conformal deposition of metals, including Cu, Pt, Pd, Ni, Au, Co and their alloys; metal oxides, including hafnia, titania and zirconia; and mixed metal oxides, within high aspect ratio and sub-100 nm features. Excellent step coverage at high deposition rates are possible due to very high fluid-phase precursor concentrations, which lead to surface reaction rate-limited kinetics over broad ranges of precursor concentrations. The Cu deposition technology offers potentially viable solutions for future generations of interconnect technology. Additionally, the ability to sequentially deposit metals and high k oxides within high aspect ratio features provides a promising pathway for scaling capacitor structures in 3-D.

RESEARCH FOCUS:
NOVEL SYSTEMS & ARCHITECTURE

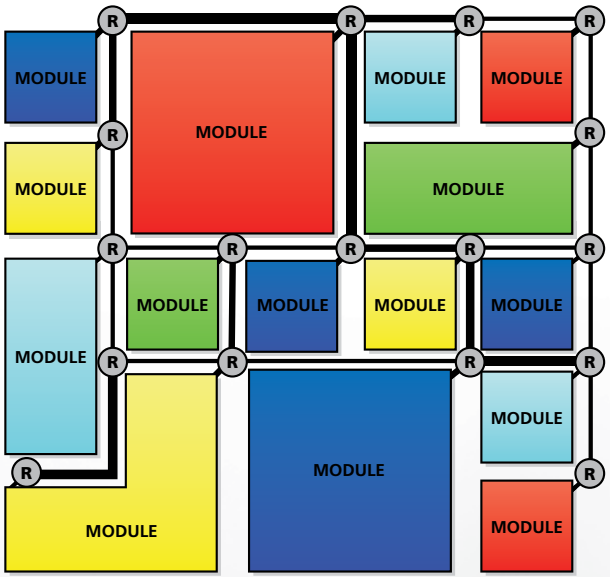
The new horizon of systems research became the theme of a significant SRC forum held this year. The challenges that lay ahead were posed as two primary questions: What is the smallest functional autonomous system that integrated circuit technology might ultimately enable? And could we someday build a cube that is 10 microns per side that would exploit end-of-scaling CMOS technology to determine the health of living cells?

The 2007 SRC Forum on Nanomorphic Microsystems held at Stanford University addressed these provocative queries. Such a cell would need its own energy sources, sensors, computers and communication devices, integrated into a complete system. In addition to the awesome challenges of designing and fabricating at the level of atoms, the artificial cell would need to be extremely energy efficient in its operations since only infinitesimal amounts of energy would be available to it. Clearly, such a microcell is not feasible today; however, the studies on limits for all of the required technologies at the forum indicate that a functional micron-scaled cell cannot be ruled out as a possibility.



A Nanomorphic Cell: *Generic architecture, constraints and trade-offs. Very limited space needs to be divided between sensors, power supply and electronic components (a). At this scale, every atom must play a role (b).*

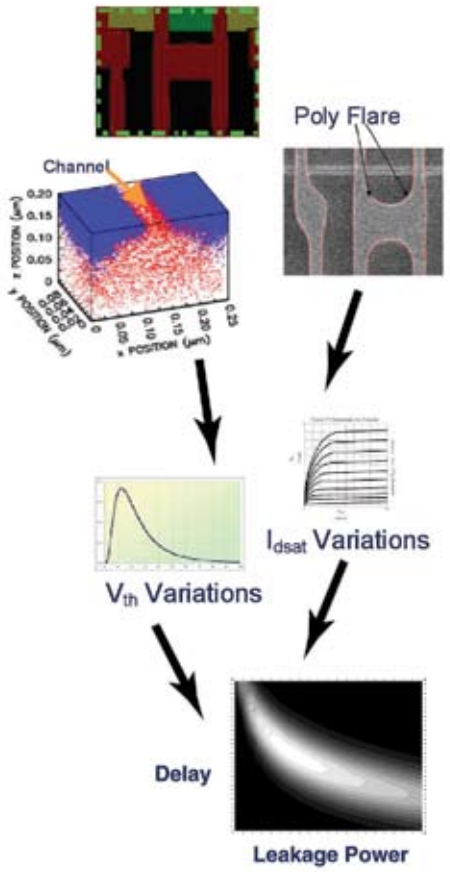
On the opposite end of the systems research spectrum is the need to design large, complex integrated circuits. These are often comprised of many individual blocks with an interconnection scheme based on electrical buses or dedicated point-to-point structures. Network on Chip (NoC) designs, however, use shared links and routers to provide a block interconnection scheme that could require less chip area and use less overall power, while providing the same ability to transfer information. A GRC research group at the Technion-Israel Institute of Technology was able to add a quality metric into a NoC link optimization flow that uses non-uniform link capacities to decrease the needed link capacity by 30% over a conventional approach.



Non-uniform link capacities in NoC design.

RESEARCH FOCUS:
ROBUST DESIGN METHODOLOGIES

Robust design issues are driven by the fact that as feature sizes decrease (smaller devices, wires and spacing), the production of chip designs that work at these reduced dimensions becomes increasingly difficult. As widths approach atomic dimensions, it becomes impossible to control the characteristics of the wires and devices needed for chip correctness. This variability produces chips that are too slow, leak too much power, or do not work at all. Techniques and computer-aided tools produce designs which are robust to this variability and are a key ingredient in advancing semiconductor technology into the future.



Leakage power increases due to process variations.

Researchers at the University of Michigan are addressing aspects of robust design in their work on computer-aided design solutions for parametric yield optimization. Process controllability is not scaling together with devices. These device parameter variations cause large spreads in circuit performance metrics that need to be understood, analyzed and compensated for in the design. Otherwise, the designs will not be robust. Yields will drop and more chips will have to be discarded because they do not meet their performance specifications.

The Michigan researchers developed a design technique called "soft-edge flip-flops" to make such designs more robust. These flip-flops (simple storage elements) have a transparent window rather than a hard edge, allowing signals slowed down by variability to arrive on time. By enabling time borrowing or cycle stealing, the logic paths between flip-flops work properly in the presence of these delay variations, creating chips that can perform faster while still giving acceptable yield. This successful technique has improved mean delay by as much as 22%, while simultaneously reducing the standard deviation of delay by as much as 24% and increasing power by less than 3%.

The College of Nanoscale Science & Engineering's Albany NanoTech Complex

CAIST CENTER

SRC awarded the State University of New York (SUNY) at Albany a three-year, $1.5 million contract aimed at extending copper and low-k dielectric scaling. The New York Center for Advanced Interconnect Science and Technology (CAIST), managed by SUNY, has subcontracted 27 new research projects with 14 top universities throughout the United States. Moreover, the state of New York will match the funding at a level of $1 million per year.

Interconnect scaling is one of the most important enablers for the continuation of Moore's Law beyond 2011. By providing chip companies with materials and methods for further extension of interconnect scaling, these projects will help to ensure that semiconductor chips grow smaller, faster and cheaper. Research areas of focus include methods to reduce the resistance of Cu in narrow dimensions; formation of Cu diffusion barriers just a few atoms thick; processes for depositing very strong insulators which are mostly air; fundamental understanding and improvement of interconnect reliability; and techniques for seeing buried interfaces with resolution on the scale of a single atom.

NON-CLASSICAL RESEARCH CENTER

The University of Glasgow has joined the Non-Classical Research Center (NCRC), led by the University of California-Santa Barbara, in researching high-k dielectric and p-channel material development. The Center has studied realistic non-parabolic band structure, which is expected to yield higher channel carriers and current. It has proposed a structure design predicting a high current of 4 mA/mm. Other achievements include a process for planarized, self-aligned, selective epitaxy for InGaAs source/drain, and contact resistance on InGaAs less than 10^{-8} ohm-cm^2.

TECHCON, sponsored by the SRC community, is the eminent semiconductor industry technical conference. This annual event showcases the quality of the SRC research portfolio, the excellence of SRC students and faculty, and the magnitude of the collaborative research investment made by the semiconductor industry through SRC.

TECHCON 2007, SRC's ninth technical conference, was held September 10-12 in Austin, Texas – a great venue, as several member companies are located there. Attendees included 184 industry participants, 17 faculty, 177 students, and 34 others (staff, etc.), for a total of 412 diverse participants. One hundred seventy students presented technical papers and posters representing a broad cross-section of SRC-funded research.

Dr. John Cohn, IBM Fellow and Chief Scientist of Design Automation, delivered the keynote address at the Conference Banquet on Tuesday evening, and Dr. Nerissa Draeger, Novellus Technologist/Patent Executive, spoke at the Awards Luncheon on Wednesday. Dr. Cohn completed his PhD as an SRC student at Carnegie Mellon in 1991; Dr. Draeger was an SRC Fellow and completed her PhD at the University of Illinois/Urbana Champaign in 2000.

Professor Wojciech Maly, recipient of the 2007 Aristotle Award, surrounded by current and former students and SRC staff.

2007 Technical Excellence Award Winner Professor Madhavan Swaminathan, Georgia Tech.

OTHER CONFERENCE SPEAKERS INCLUDED:

Sumit Sadana, Freescale Senior Vice President, Strategy and Business Development, addressing the GRC Fellows and Scholars and others attending the Graduate Fellowship Program Banquet.

Speakers from academia included **Professors Michelle Simmons,** University of New South Wales, and **Paul Nealey,** University of Wisconsin, in a special session on "Novel Nano Assembly" on Monday afternoon. UC/Berkeley CITRIS Center Director **Professor Shankar Sastry's** presentation entitled "Information Technology for the Benefit of Society" was the basis of a special session on Tuesday afternoon.

The TECHCON students get better with every event and industry support continues to be outstanding. As one industry evaluator said, "I think you have it perfected!" And so the ninth iteration of TECHCON is declared a success.

AWARDS

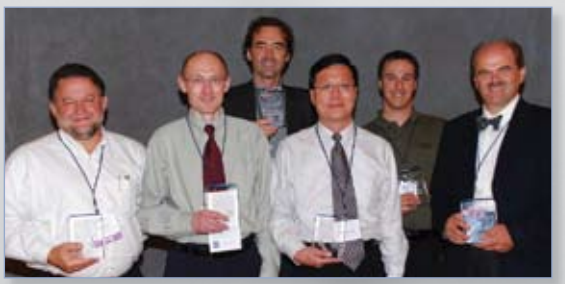
Aristotle Award | For excellence in teaching through the research process.

• **Professor Wojciech Maly** was a task leader on SRC's first contract at Carnegie Mellon University in 1982 and is still active on 3 SRC contracts.

Technical Excellence Award | For research that is a key contributor to technology significantly enhancing the productivity of the semiconductor industry.

• **Professor Madhavan Swaminathan** and his team from Georgia Tech
• **Jinwoo Choi,** former student, now at IBM
• **Krishna Srinivasan,** current student at Georgia Tech
• **Rohan Mandrekar,** former student, now at IBM

Inventor Recognition Awards were given to a number of faculty and students for their research leading to patentable inventions.



Winners of the 2007 Mahboob Khan Outstanding Mentor Awards: *Rick Wise, TI; Jon Reid, Novellus; Martin Gall and Hsi-An Kwong, Freescale; Charles Alpert, IBM, and Radu Secareanu, Freescale. Colin McAndrew, Freescale, was not present for this photo.*

Mahboob Khan Outstanding Mentor Awards

The Mahboob Khan Outstanding Mentor Award recognizes GRC Industrial Liaisons who have made a significant impact on the technical contributions of the research, been instrumental in transferring the research results to industry, and are deeply committed to graduate student education. Nominations for this award are accepted from GRC members, including GRC-sponsored university researchers and graduate students.

STUDENT **PROGRAMS**

SRC research supports over 1500 advanced degree students each year on contracts guided by the program memberships —more than 6500 since 1982. These students are academically outstanding and have demonstrated research capability in disciplines critical to the semiconductor industry. Student contributions to the various SRC research programs are significant, as evidenced by their participation in national conferences, invention disclosures, technical awards and publications.

SRC also offers a number of resources to help member companies obtain access to relevantly educated technical talent. Recruiters can search a database of supported students on the secure website for each research program to find students whose backgrounds meet their interests. Through sponsored events, industry representatives have many opportunities to meet and interact with students. These resources assist members in filling internship and employment needs.

THE VALUE OF **SRC STUDENTS**

- Since 1982, over 60% of former SRC students (more than 3600) have joined sponsoring organizations or university faculties, or have continued to a higher degree.
- Over 100 alumni currently represent their companies as members of various SRC technical advisory boards and as mentors to SRC research projects.
- Over 200 former SRC students are on faculties at leading universities around the world, including 48 who have current research funding with one or more SRC entities.
- At the beginning of the 2007 fall term, 35 GRC Fellowships, 1 NRI Fellowship, and 14 SRCEA Master's Scholarships were in place. These programs are designed to attract students with US citizenship or permanent resident status to semiconductor industry research.

2007 **STUDENT HIGHLIGHTS**

- Student/industry networking events were held at the University of Arizona, Carnegie Mellon University, UCLA, MIT, UC/Berkeley, and Georgia Tech.
- The first CareerConnections Online was held in October.
- NRI student information became available via the website.
- The 2007 Simon Karecki Award was presented to Nelson Felix, Cornell, at the University of Arizona CEBSM Review.
- SRC's fourth design contest, SRC/SIA IC Design Challenge: Performance at the Limits, was initiated with 47 participating university teams.

For further information on SRC Student Programs, *please refer to the Student Programs Brochure online at* www.src.org/member/students/about.asp.

***Best in Session Awards at TECHCON 2007** were presented by SRC Board Chair Craig Sander, AMD (center). Awards were made based on judging by a panel of industry experts in each of 19 paper sessions.*

FOCUS CENTER RESEARCH PROGRAM

Focus Center Research Program (FCRP) is an initiative for pre-competitive, cooperative, long-range, applied microelectronics research sponsored by members of the Semiconductor Industry Association (SIA), members of the US semiconductor equipment, materials, software and services industry, and the US Department of Defense (DoD). The Microelectronics Advanced Research Corporation (MARCO), a SRC subsidiary, was established in 1997 to support the work of FCRP.

The intent of FCRP is to concentrate resources on those areas of microelectronics research that must be addressed to maintain the historic productivity growth curve of the industry; strengthen the university research infrastructure and expand its capabilities in silicon related research; achieve critical mass through relatively large blocks of funding; and provide the optimal balance of creative freedom and targeted objectives. FCRP has been an extremely successful program for industry, government and academia.

Focus Centers are "virtual" in that they consist of multiple universities, allowing for the best expertise at a number of institutions to be tapped, and the greatest overall capability in a particular technology area to be built. Each center is managed by a full-time university center director and addresses one of the major technology focus areas of the International Technology Roadmap for Semiconductors (ITRS). In order to provide the contributions necessary to keep the semiconductor industry on its technological growth track, heavy emphasis is placed on achieving key long-term research results. Although the needs identified by the ITRS provide a meaningful guideline for the research objectives, a measurable percentage of the effort also encompasses activities not envisioned by the Roadmap.

EACH FOCUS CENTER IS EXPECTED TO HAVE OR DEVELOP THE FOLLOWING KEY ATTRIBUTES:

A compelling and well-articulated vision for long-term, exploratory research important for US semiconductor industry competitiveness; a vision that is both embraced and enthusiastically deployed; a vision that leads to the conception, demonstration and evaluation of revolutionary options;

An interactive, cross-disciplinary, multi-institutional environment, where the implications of all research plans and results are adequately comprehended by a team of center investigators;

Acknowledged global leadership in the technical field based on pioneering contributions;

A crisp, motivating and empowering message that can be remembered and used by all center participants as a guiding principle to make decisions;

An up-to-date understanding of all significant technology barriers within a center's area of focus, and an understanding of the larger context in which the center's work is performed;

A dynamic process for program evolution, including adding, subtracting and modifying theme areas.

Mission

The mission of FCRP is to provide long-term breakthrough research resulting in paradigm shifts and multiple technology options. The program provides a US-based university research program that is guided strategically by industry and the US government, but managed by the US university community. It provides a multi-university, multi-disciplinary, collaborative research environment that is highly leveraged by both industry and US DoD funding. The FCRP program provides for research focused on carrying CMOS to its ultimate limits while developing "hooks" to solutions beyond CMOS. The program also provides access to highly trained university graduate students.

Advantage

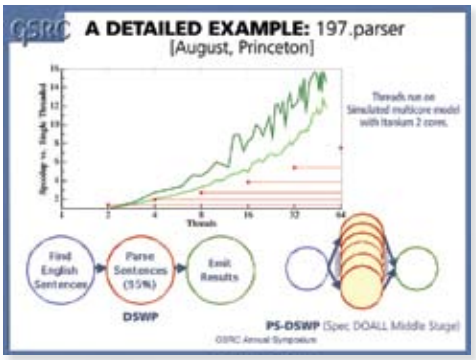
FCRP research creates the breakthroughs that are critical to the US security and economic competitiveness goals, giving US companies a tremendous competitive advantage in the race to lead the technological revolution. FCRP offers mutual leverage to industry and government sponsors. Moreover, this incomparable program is the only university research program that gives the DoD one-to-one leverage for its money, delivering an unmistakably high payoff.

EXAMPLES OF ACADEMIC YEAR 2007 **ACCOMPLISHMENTS IN THE FCRP CENTERS:**

1 GIGASCALE SYSTEMS RESEARCH CENTER (GSRC)

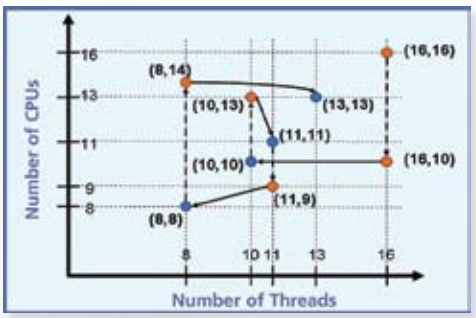
Design Technologies *for* Concurrent Systems Theme

The Implicitly Parallel Programming Flow made significant progress in discovering and exploiting concurrency in sequential programs. The SPECint 197.parser benchmark has been traditionally considered a program with very little hope for parallel execution in multiprocessor systems. David August and his team at Princeton showed that by isolating the core sequential recurrence from the bulk of the work in large loops, one can create a code arrangement that has more than 32 simultaneous threads and achieves up to 16 times of speedup on a simulated multicore system. This shows that with appropriate parallelism detection and code transformation, one can achieve a much higher level of speedup for legacy code base than what most people anticipated in the past.



Design Technologies *for* Concurrent Systems Theme

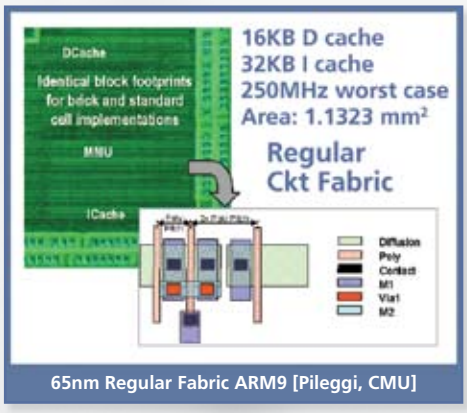
Irwin, et. al., at Penn State are studying helper thread-based schemes to adapt application execution to CPU availability changes with the goal of minimizing the energy-delay product (EDP). The dotted lines represent a specific CPU availability change pattern along program execution (16 -› 10 -› 13 -› 9 -› 14). The solid lines point to better configuration points selected by the helper thread. With the ideal number of CPUs and threads selected dynamically, the EDP savings can be up to 50% for the FFT codes in NAS NPB benchmark suite.



2 CENTER FOR CIRCUITS & SYSTEMS RESEARCH CENTER (C2S2)

Silicon Infrastructure Theme

Regular Circuit Fabrics impose strict uniformity requirements at geometry level for all devices, and then restructure the entire RTL flow, from library up to synthesis, to ensure that there is no loss of silicon efficiency. Prior solutions, such as so-called Restricted Design Rules (RDRs) had imposed penalties as high as 15% on silicon area. In 2007 C2S2 demonstrated a fully functioning ARM9 CPU core in 65nm CMOS, with both footprint and speed identical to that of a standard cell-based approach *(right)*. This showed conclusively that we can gain the benefits of more predictable circuits without unacceptable penalties in speed or area.

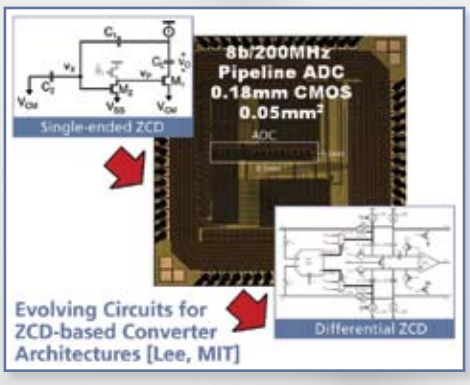


65nm Regular Fabric ARM9 [Pileggi, CMU]

Analog Circuits and Interfaces Theme

The principal challenge for non-digital circuits, in the face of nanometer scaling, is the ongoing degradation of essential analog device behaviors: less gain, more variability, less matching, etc. C2S2 researchers are working on novel "mostly digital" architectures for analog building blocks (i.e., analog functions rendered with high-volume scaled digital transistors). They are working across the full spectrum of analog building blocks: converters, communication circuits, phase lock loops, wireless, wireline, etc.

An excellent example of this *(right)* is their work on switched-comparator (SC) circuits at MIT. This work is whole scale reinvention of essential switched-capacitor architecture, but replaces opamps (and attendant gain/stability issues) with comparators. The work was awarded a Best Paper honor this year at ISSCC. This research also generated a DARPA-funded seedling, under the TEAM project, to work on a variant of these ideas: zero-crossing detector (ZCD), based comparator circuits, for switched comparator architectures.



EXAMPLES OF ACADEMIC YEAR 2007 **ACCOMPLISHMENTS IN THE FCRP CENTERS:**

3 INTERCONNECT FOCUS CENTER (IFC)

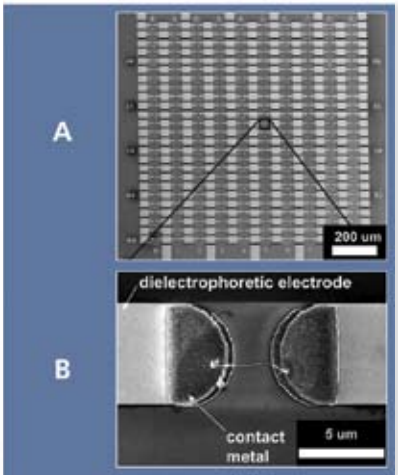
Electrical Interconnects Theme

Carbon Nanotube (CNT) manipulation is important for testing individual structures and potentially assembling more complex networks. Electrophoresis has been used to move and place individual CNTs, enabling IFC researchers, for the first time, to conduct a comprehensive statistical characterization of multi-wall metallic carbon nanotube interconnects. They used an array of CNTs to quantify the impact of diameter, number of shells, tube quality and contact metal (Au, Al, Ti and Pd) on conductivity.

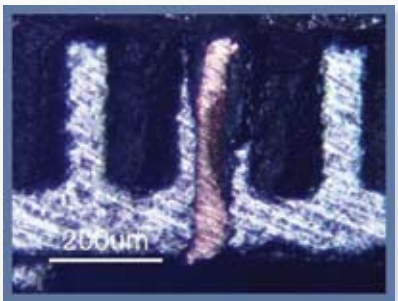
Thermal Dissipation *and* Power Management Theme

New concepts in electrical/optical/thermal I/O have been created. During 2007 IFC researchers fabricated, for the first time, a prototype having electrical through-wafer interconnects, fluidic through-wafer interconnects, micro-channel heat sink, heaters/thermometers, and solder bumps.

In particular, the cooling of 3-D stacks of chips has been achieved by constructing fluidic channels within each chip in the stack. High speed, chip-to-chip communications are being pursued through the use of shielded, coaxial I/O and air-cladded signal paths on organic substrates. The evaluation of the off-chip approaches are being pursued along with the development of a high-speed research test vehicle.



Array of CNT connections manufactured to enable study (H.-S.P. Wong, Stanford)

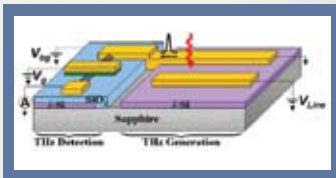


Cross-section of a wafer with electrical (copper) and fluidic through-wafer interconnects (M. Bakir et al, Ga Tech)

4 MATERIALS, STRUCTURES AND DEVICES RESEARCH CENTER (MSD)

CMOS Extension: Si-Ge Channel Materials *and* Devices Theme

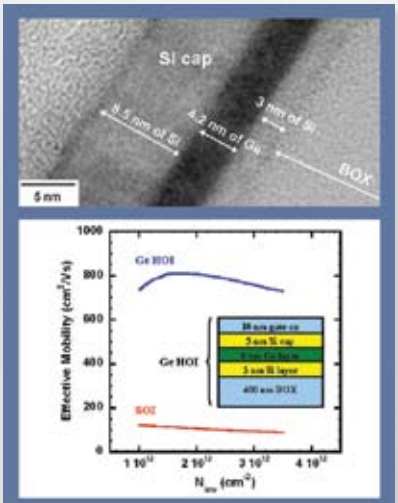
Strained Si/strained Ge heterostructures on insulator p-FETs with 9x hole mobility enhancement over Si were demonstrated in Professor Saraswat's and Professor Hoyt's groups. This technology, combining the advantages of strain, confinement, and low parasitic resistance, is an attractive candidate for scaling P-FETs into the sub-20-nm regime.



Device geometry and measurement setup for terahertz electrical transport study of single-walled carbon nanotube. The metal electrodes are shown in gold colour, SiO top-gate dielectric in green, SiO_2 in blue, silicon layer in pink, and the sapphire layer in grey. Femtosecond laser excitation (red arrow) generates picosecond voltage pulses, which are then transmitted to the nanotube transistor. (McEuen, Cornell)

CMOS Extension/CMOS Plus: Nanowires *and* Nanotubes Theme

Professor McEuen's group has made a breakthrough in measuring transport in carbon nanotubes (CNTs) at THz frequencies. These results probe the physics of high-speed transport and provide important knowledge that will be useful for developing new predictive models for performance of high-speed CNT devices.



Measured effective hole mobility versus inversion charge density for Ge/40 HOI and SOI. The buried Ge channel is nominally 6nm thick. The SOI thickness is 27nm. (Hoyt, MIT)

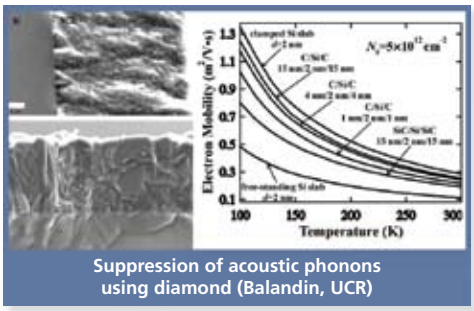
EXAMPLES OF ACADEMIC YEAR 2007 **ACCOMPLISHMENTS IN THE FCRP CENTERS:**

5 FUNCTIONAL ENGINEERED NANO ARCHITECTONICS CENTER (FENA)

Simulation and Computation of Novel Engineered Nanomaterials & Devices Theme

FENA researchers have shown that the mobility enhancement achievable through the suppression of electron-phonon scattering in diamond/Si nanowires can also be achieved in planar structures. Diamond is the best heat conductor and has demonstrated potential for electronic applications. This is an important finding, since thin film planar structures can be more easily incorporated into a CMOS process.

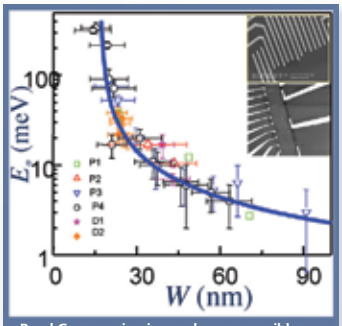
Figure top right shows the results of the modelling of electron mobility in thin Si films embedded within the acoustically hard barrier layers made of nano-crystalline diamond (n-D) and SiC. Inset shows micrographs of n-D films on Si samples used for experimental study and comparison with the modelling results.



Suppression of acoustic phonons using diamond (Balandin, UCR)

Novel Integrated Devices Theme

In the area of graphene-based nanoscale electronics, FENA researchers, for the first time, measured quantum coherent transport in graphene-based field effect transistors. They have developed a method to synthesize graphene by reducing graphite oxide and also manipulating graphene nanoribbons via quantum confinement effects to increase the bandgap, for which this year they have achieved up to 0.3 eV by patterning 20 nm ribbons.



Band Gap opening in graphene nano ribbons: Energy Gap ~ 300 meV for ~20 nm ribbon width (P. Kim, Columbia)

2007 FCRP **TRANSFERRED PROJECTS**

FROM GRC TO FCRP

Fast Stimulation of Data and Coupling Noise in Oscillators and PLLs via Automatic Nonlinear Macromodeling and Multi-Time Numerical Methods: SPICE++analog/RF system prototyping and simulation environment incorporated into Metropolis II hybrid simulation environment.
***Professor Jaijeet Roychowdhury**, University of Minnesota*

FROM FCRP TO GRC

Robustness of Deeply Scaled CMOS Logic Circuits: Design methodology for developing robust circuits in deeply scaled CMOS.
***Professor Borivoje Nikolic**, University of California-Berkeley*

Predictive Modeling and Simulation of Reliability Degradation in Nanoscale Circuits: Predictive models for various reliability mechanisms, compatible with standard models and open source, extraction method of model parameters, circuit-level simulation methods for both short-term and long-term reliability prediction, and in-situ diagnosis techniques for circuit aging.
***Professor Kevin Cao**, Arizona State University*

On-Chip Arrays for Quasi-Static Transistor Variability Characterization: Develop and fabricate integrated, on-chip measurement test structures for measuring current-voltage, capacitance-voltage, and 1/f noise characteristics of large numbers of devices in highly multiplexed arrays.
***Professor Ken Shepard**, Columbia University*

Variation Insensitive Low-Power SRAM Design Using Circuit Adaptation and Tuning: A set of design topologies and methods that desensitize SRAMs to process variation and environmental conditions in the 45nm and 32nm nodes, while minimizing disruption to existing circuit topologies and design methodologies.
***Professors Ken Mai**, Carnegie Mellon University **& Ben Calhoun**, University of Virginia*

FCRP RESEARCH PROGRAMS

- $137M invested by FCRP Members
- $69M total leverage funding
- $65M directed
- $4M collaborative
- 9 contracts
- 1,215 students
- 333 faculty members
- 41 universities

DELIVERABLES

- 5,482 technical documents
- 22 patents in FCRP portfolio
- 153 patent applications
- 126 inventor awards
- 17 software programs
- 87 themes in research catalog

NANOELECTRONICS RESEARCH INITIATIVE

As the ultimate limits to the scaling of CMOS (Complementary Metal Oxide Semiconductor) technology continue to get closer, new approaches to emerging areas in nanoscale electronics need to constantly be explored. For this purpose, the Semiconductor Industry Association (SIA) requested that SRC establish the Nanoelectronics Research Corporation (NERC), a wholly owned SRC subsidiary, to develop and administer a university-based program. In 2005 Nanoelectronics Research Initiative (NRI) was successfully instituted.

The goal of NRI is to demonstrate novel computing devices capable of replacing the CMOS transistor as a logic switch in the 2020 timeframe. These devices should show significant advantage over ultimate CMOS transistors in power, performance, density, and/or cost, and enable the semiconductor industry to extend the historical cost and performance trends for information technology.

To meet these goals, NRI is primarily focused on researching devices that utilize new computational state variables beyond electronic charge. In addition, NRI is interested in new interconnect technologies and novel circuits and architectures – including non-equilibrium systems – for exploiting these devices, as well as improved nanoscale thermal management, novel materials and fabrication methods for these structures and circuits. Finally, it is NRI's aim that these technologies be capable of integrating with CMOS to allow exploitation of their potentially complementary functionality in heterogeneous systems, and to enable a smooth transition to a new scaling path.

NRI RESEARCH CENTERS

Throughout 2006, NRI established research programs at over 20 universities across the country, organized into virtual centers. The key objectives for 2007 were to complete the organization of these centers, launch clear research programs on vital NRI topics, and to create a clear framework for delivering those results back to the member companies. With participating universities grouped largely by geography, three main NRI centers have been established. While all of the centers are working on research aimed at finding a new logic switch, the focus of the programs at each center has its own specific character.

The Western Institute of Nanoelectronics

The Western Institute of Nanoelectronics (WIN), headed by Professor Kang Wang, was the first research center to be established in 2006. Headquartered at the UCLA Henry Samueli School of Engineering and Applied Science, WIN participants come from three University of California campuses (Los Angeles, Berkeley, and Santa Barbara), as well as Stanford University. WIN focuses solely on spintronics and related phenomena, extending from material, devices, and device-device interaction, all the way to circuits and architectures. In addition to its NRI funding, this center receives additional direct support from Intel and the UC Discovery program.

The Institute for Nanoelectronics Discovery and Exploration

The Institute for Nanoelectronics Discovery and Exploration (INDEX) was established in the second quarter of 2006 and is headed by Professor Alain Kaloyeros. Headquartered at the College of Nanoscale Science and Engineering of the State University of New York-Albany (SUNY-Albany), it also includes the Georgia Institute of Technology, Harvard University, the Massachusetts Institute of Technology, Purdue University, Rensselaer Polytechnic Institute and Yale University. INDEX focuses on the development of nanomaterial systems; atomic-scale fabrication technologies; predictive modeling protocols for devices, subsystems and systems; power dissipation management designs; and realistic architectural integration schemes for realizing novel magnetic and molecular quantum devices. INDEX also receives additional direct support from IBM and New York State.

The South West Academy for Nanoelectronics

The South West Academy for Nanoelectronics (SWAN), headed by Professor Sanjay Banerjee, is the newest of the centers, established in the third quarter of 2006. Headquartered at the Microelectronics Research Center at the University of Texas-Austin, it includes a collective team from UT-Dallas, Texas A&M, Rice, Notre Dame, Arizona State and the University of Maryland. SWAN focuses on a variety of new devices, including spin-based switches, nanowires, nano-magnets, and devices that use electron wave or phase interference. Additional work is being done on modeling, novel interconnects, such as plasmonics, and nano-metrology techniques. In combination with its NRI funding, SWAN receives support from TI and the Texas Emerging Technology Fund.

Given the exploratory nature of much of the NRI research as it seeks out entirely new device and computation technologies, it is particularly important that industry and academia work closely as research paths develop. Each NRI center has an Executive Committee, comprised of the center lead professors and representatives from the member companies, which meets regularly to discuss the center's technical progress and logistical issues.

At the end of 2007, the second Annual NRI review was held in Santa Clara, CA and was attended by almost 100 individuals coming from all of the NRI centers, member companies and government agencies. This was the first opportunity to see an overview of all of the NRI research projects—from the NRI Centers and from NSF-NRI projects—after their first full year of operation. The attendees gave overwhelmingly positive feedback on the review, and were particularly impressed with how quickly the projects had ramped up, especially with relatively modest initial resources. Highlights included new results in understanding the unique properties of graphene for potential device usage, including pseudospintronics; new results on magnetic and spin-wave logic; and exciting insights into the new class of multi-ferroic materials for devices. The diversity and quality of NRI projects were seen as creating a robust research portfolio, well positioned to achieve the NRI goals in the coming years.

Leveraged Research

In 2006 NRI joined forces with the National Science Foundation (NSF) Nanoscience Centers to acquire supplemental funding of NRI-related activities at these centers, funding work at six NSF centers. In 2007 this work was expanded and six additional projects at NSF centers have become jointly funded by NSF and NRI, and all 12 projects were highlighted at the annual review. This joint venture has shown to be a true synergistic partnership, with the NRI program gaining from knowledge created through the NSF centers, and the NSF centers benefiting from industry involvement through NRI.

Fall of 2007 also brought a new research partnership between NRI and the Commerce Department's National Institute of Standards and Technology (NIST). This partnership will enable expansion of the NRI core center programs, and will allow joint work with the NIST labs. This is a unique model which we think will accelerate the NRI research going forward.

Industry Assignee Program

NRI has recently established an industrial assignee program, where employees of the member companies are able to work directly at one of the NRI university centers. These assignees, present on behalf of NRI, assist the center directors in the technical integration of the research programs and serve as active participants in specific research projects at the center. The program grew rapidly this year, and at the end of 2007 there were seven full-time and three part-time assignees at the centers, with each center having at least three assignees on sight. This high level of industry-university interaction is expected to efficiently guide the research in the most promising directions, while simultaneously maximizing the ability of the member companies to harvest early research results as they are produced.

NRI **E-WORKSHOPS**

The NRI Technology Transfer e-Workshops are webcasts delivered by researchers from within the NRI community. The series is aimed at educating both our industry sponsors and other university participants (both students and PIs) on specific research topics being done at NRI centers.

The e-Workshops, presented by phone and web, serve a dual purpose for NRI. First the workshops allow for the latest research results to be transferred from the universities back to the sponsor companies. They are also used to disseminate the newest work-in-progress between all of the NRI participants (university and industry). Since much of this work is in brand new fields, the e-Workshops incorporate both a tutorial aspect, as well as "latest breakthroughs" information. This unique NRI offering has proven very popular, with an attendance average of 50 and some having over 100 participants.

The National Medal of Technology *(now known as the National Medal of Technology and Innovation) is the highest honor for technological achievement bestowed by the President of the United States on America's leading innovators. According to the United States Department of Commerce, the Medal "recognizes those who have made lasting contributions to America's competitiveness, standard of living, and quality of life through technological innovation, and recognizes those who have made substantial contributions to strengthening the Nation's technological workforce."*

As an Award recipient, SRC was recognized for building the world's largest and most successful university research force to support the rapid growth and advance of the semiconductor industry; for proving the concept of collaborative research as the first high-tech research consortium; and for creating the concept and methodology that evolved into the International Technology Roadmap for Semiconductors.

SRC is a research community of talented and dedicated people working together to enable progress in the semiconductor sciences and technologies that empower humankind. And it is this very community – you, our membership, university researchers and students – on which this prestigious award has been bestowed.

Thank you.

"I appreciate you encouraging the next generation **to follow in your footsteps**."

President **George W. Bush**, *upon SRC's acceptance of the award*

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SIA *(FCRP, GRC, NRI)*

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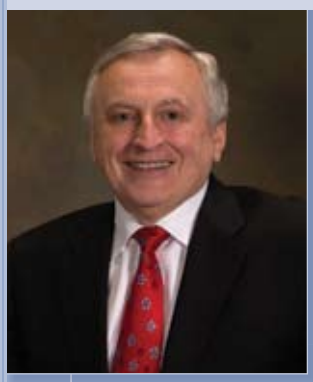

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