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The Story of SRC | Annual Report 2008

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STORY. There is one behind every individual and every company. A good story engages, persuades, even calls to action. It is a powerful force.

FOR SEMICONDUCTOR RESEARCH CORPORATION (SRC), stories abound. They can be heard from industry greats, university leaders and individual students — all of whom describe the profound impact made because of their association with SRC. Moreover, the research results and their subsequent application also create indelible impact — impact whose source largely goes unrecognized by the very public it benefits.

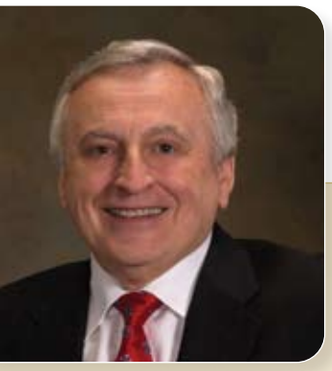
When it comes to semiconductor technology and nanoelectronics, only a relative few can understand the intricacies of a white paper written by an SRC-sponsored student. But everyone can get the fact that by doing this research, the student's life was forever changed — through paid tuition, a job with an industry leader, a bright future. And although the topic of semiconductors doesn't usually come up in the daily conversation of most people, all are aware of the technologies that drive modern life. Even many in the technology industry itself use patented discoveries resulting from SRC collaboration… yet they don't know SRC.

SRC's distinctive model of collaboration has been creating profound impact over the past quarter-century. It has brought together industry competitors to support cooperative research as a means to greater ends. It has taught universities that a joint effort with industry benefits not only their brightest students, but also their proud academic name. SRC has changed technology — and continues to do so. It has improved the U.S. economy and defense, and it has truly changed the world. SRC engages, persuades and calls to action.

And it's a really good story.

A Letter from **Larry W. Sumney**, President & CEO

OVER TWENTY-FIVE YEARS AGO, THE U.S. semiconductor industry companies formed SRC on the premise that, even though they compete in the marketplace, each could benefit by supporting cooperative, pre-competitive university research programs. I am pleased to report that in 2008 SRC, begun by these visionary industry leaders, continues to prove the validity of their hypothesis by providing university research programs responsive to the long-term needs of industry. The characteristic dynamism of the semiconductor industry has continued unabated in 2008, as it has sustained its tradition of offering more functionality per unit cost. Simultaneously, the industry has begun to explore new application areas for semiconductor products.



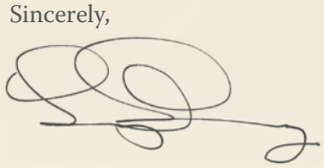
SRC is structured to rapidly adapt to the changing needs of its member companies, and several initiatives were launched in 2008 that reflect this flexibility. For example, SRC has begun to actively engage in the application of the Topical Research Collaborations (TRC) model that was established by the SRC Board of Directors. A TRC enables SRC to form and operate targeted research programs of interest to a set of companies, none of whom need be SRC members, although SRC's current members are eligible to participate and are encouraged to do so. As a general rule, a TRC research program is designed to complement the mainstream SRC semiconductor technology research programs. In 2008 SRC formed two TRC legal entities to administer and manage two distinct research efforts. One is centered around Sandia National Laboratory and focuses on nano-engineering research. The second is focused on energy research. Additionally, SRC, together with the National Institute of Standards and Technology (NIST), has engaged in the development of a research plan in bioelectronics that could serve as a basis for a third TRC. In each of these cases, SRC is offering opportunities for research programs in areas that leverage the core expertise of SRC in developing and managing university research programs in the semiconductor sciences and technologies.

The three primary existing SRC research programs, Global Research Collaboration (GRC), Focus Center Research Program (FCRP), and Nanoelectronics Research Initiative (NRI), have continued to make important research contributions in response to their individual missions. Two new university-based research centers were launched in 2008: GRC's Texas Analog Center of Excellence (TxACE) and NRI's Midwest Institute for Nanoelectronics Discovery (MIND). Headquartered at the University of Texas at Dallas, TxACE research will focus on analog integrated circuits with an application space defined by low power, public safety and security, and medical applications. It is particularly notable that Texas Instruments and the state of Texas, through its Emerging Technology Fund for Research Superiority, are funding partners for TxACE. SRC has partnered with the state of Indiana and NIST to create NRI's newest center, MIND, headquartered at Notre Dame.

The focus of MIND research is on low energy devices and systems within the context of NRI's mission of sustaining the benefits of scaling through device and system innovation. FCRP operates under a three-year renewal cycle for its five centers, and SRC began preparations in 2008 to develop the 2009 solicitation for FCRP centers.

In a difficult economic environment, scientific and engineering innovation is key to providing pathways to products and services for the recovery and/or growth of SRC member companies. SRC is well positioned to respond to this challenge and pledges to strive for excellence in response to the research and human resource needs of our member companies.

Sincerely,



Larry W. Sumney, President & CEO

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The annual report of Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program and provide information on activities and events of the SRC community for the previous calendar year.

A digital PDF version of the 2008 SRC financials are available for members online at www.src.org. A copy of this report and additional information about SRC are also accessible at www.src.org.

2008 IMPACT **BY THE NUMBERS**

SRC Research Programs

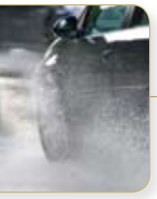
$1.335 Billion total investment

- $803M invested by SRC members
- $532M total leveraged funding
  - $92M directed
  - $179M collaborative
  - $261M influenced
- 2906 contracts
- 7455 students
- 1707 faculty members
- 241 universities

Research Programs Deliverables

- 43,419 technical documents
- 326 patents granted
- 777 patent applications
- 695 inventor awards
- 579 software tools
- 2315 research task/themes

04



SRC Collaborative Research Offers Lifesaving Technology and Economic Growth Opportunity

A fog has settled on the road you're traveling. You're driving carefully, but the dense mist has reduced your visibility to mere inches beyond your car's hood. Your car, however, knows what's ahead and alerts you to a vehicle stopped before you in the darkness. You take action accordingly, thanks to your car's warning, and prevent the impending accident.

A RADAR SYSTEM LIKE THAT DESCRIBED ABOVE is not science fiction. It does exist, but has been limited to luxury vehicles few can afford. SRC is developing the fundamental technology to enable implementation of this life-saving radar using a silicon chip platform at a cost affordable to everyone. This lower-cost automotive radar, key to features such as adaptive cruise control and collision avoidance, relies on inexpensive, widely accepted CMOS technology, with the new silicon-based radar chip costing just a few dollars to produce.

According to Professor Ken O, lead researcher at the University of Florida, whose collaborative team developed the innovative technology breakthrough, "Our dream is that the radar chip will be available for every person who can afford an automobile." Moreover, the market for the radar technology is expected to quickly grow to $2 billion by 2010, enhancing the overall economy and engaging technology and automotive industries around the world.

06

Acknowledging Past Successes, **Anticipating Tomorrow's Victories**

IN THE AUTUMN OF 1981, the U.S. semiconductor industry recognized that it was rapidly losing market share to formidable competitors. The response of the U.S. companies was novel and unexpected: *they formed SRC in the Spring of 1982 to organize and manage a cooperative university research program to address the technical challenges faced by the industry.* The immediacy of the problem of market share loss was addressed by funding the long-range solution of university research — a visionary and radical idea. Since its inception, SRC research and graduates have played an important role in stemming and reversing the loss of market share by SRC member companies, and SRC has been a key enabler for their remarkable resiliency in the global marketplace.

The semiconductor enterprise landscape is different today than in 1982, but it remains very dynamic. Some companies worldwide have moved away from the Integrated Device Manufacturing (IDM) business model and are niche players in the semiconductor markets, while others provide fabrication of integrated circuits as a service. The forces driving these industry changes are many, but include the high cost of integrated manufacturing facilities and operations, as well as the strategy of some companies to focus on specific markets in a growing integrated circuit application space. Overall, semiconductor companies are taking a two-faceted approach to provide their customers with increased functionality while reducing cost: scaling of feature sizes in accordance with Moore's law, and diversification in the application space for integrated circuits to stimulate the growth of new products. Many societal benefits in biomedicine, energy and consumer electronics will result.

COOPERATIVE RESEARCH: INCOMPARABLE VALUE

Cooperative university-based research programs offer the optimum approach to addressing current technology challenges. Today SRC research — an ongoing collaboration among industry, universities and government entities — is addressing the very questions that will impact tomorrow's world.

- What can be done to provide information technologies that offer orders of magnitude improvements in performance per unit of power consumed?
- How can the cost of integrated circuits manufacturing be reduced by orders of magnitude?
- Are there design techniques that can reduce non-recurring engineering costs for integrated circuits containing billions of transistors by orders of magnitude?
- How can reliable, self-organizing systems be designed and fabricated that reconfigure themselves in response to defects and/or component failures?
- Can the traditional benefits of continuous semiconductor technology cost reductions be extended to medical diagnosis and treatment through the convergence of biology and nanoelectronics?

It is the SRC experience that collaborative university, industry and government research programs can be expected to make essential contributions to the daunting technical challenges the industry now faces. Over the past 25 years, the synergy resulting from SRC's unique structure has always stimulated remarkable and unexpected solutions to the ever-shifting issues facing the semiconductor industry. Today's — and tomorrow's — challenges are no different. The SRC model remains strong, relevant and proven… ready to usher in innovative answers and new victories.

"Our motivation is to fund the most relevant and critical research for international companies, so we go where the best university talent is — around the globe."

Steven Hillenius, Executive Director GRC

GLOBAL RESEARCH COLLABORATION

Advancing the Next Big Thing

GLOBAL RESEARCH COLLABORATION (GRC) harnesses research from the world's top universities and transforms it into incomparable competitive advantage for SRC member companies. Industry-driven and pre-competitive, this research focuses on the next breakthrough in semiconductor technology. GRC has invested more than one billion dollars and worked with over 7400 students in hundreds of universities worldwide, not only advancing essential technology that drives the global economy, but creating the future leaders and innovators in the industry.

GRC programs address the critical challenges on the International Technology Roadmap for Semiconductors (ITRS), delivering the solutions that sustain Moore's Law. Synergy among researchers and the industry members is the cornerstone of GRC. Within all GRC programs, the operational model involves intense industry engagement in formulating, shaping and executing the research agenda. This fact, coupled with unique features such as the Industrial Liaison Program, ensures that member company needs are met with high-leverage, compelling return-on-investment research.

The emphasis in 2008 has been in the areas of technology scaling, applications research and the robust design of circuits, systems and architectures.

RESEARCH FOCUS: TECHNOLOGY SCALING

The semiconductor industry's growth rate relies on continuously enhanced functional density to provide increasing value through new materials and assembly options. Additionally, new characterization, materials and assembly methods are needed that enhance functional scaling and diversification. The ultimate objective is to develop novel, sustainable, high performance and low variability processes, materials and nanocharacterization methods that enable affordable nanofabrication.

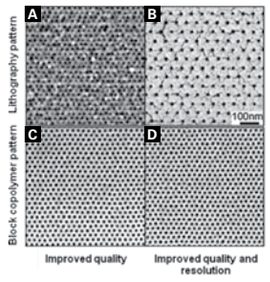


FIGURE 1 Comparison of the quality and resolution of patterns created by lithographic tools using current materials and processes (A, B) versus patterns created using the same tools but with self-assembling block copolymer materials (C, D).

Two recent advances have been in the directed self-assembly and nano-metrology research areas. A directed self-assembly technique of pattern density multiplication is an approach demonstrated by the University of Wisconsin/Madison researchers. They have achieved a pattern density multiplication of 4X, with 27nm features (Figure 1). A project seeking to extend the spatial, temporal and spectral resolution of low energy electron microscopy (LEEM) has made substantial progress in realizing instrumentation capable of imaging at one millisecond temporal resolution and two nanometers of spatial resolution. This enhanced spatial resolution and improved temporal resolution has been used to improve understanding of the growth of germanium (silicon) quantum dot nanostructures (Figure 2).

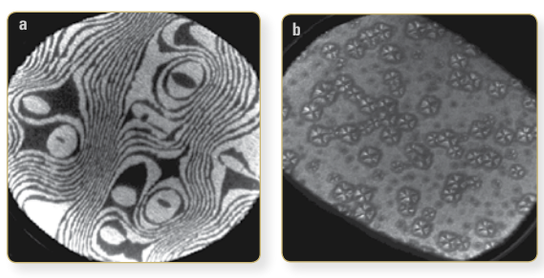


FIGURE 2 a) Si (100) 2x1 surface, dark field image, 5 µm field of view; b) Ge wetting layer and quantum dots grown on Si (100) 2x1 surface, dark field image, 10 µm field of view.

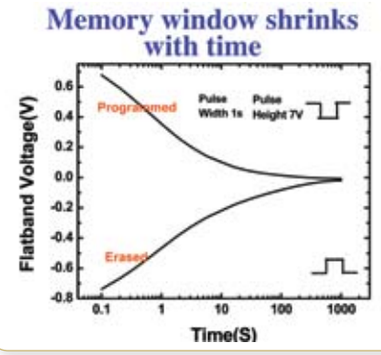


FIGURE 3 Retention time of MOSFET with ferroelectric gate dielectric after program and erase demonstrates potential for DRAM application.

Significant research progress was made in 2008 in device structures. In the Non-Classical CMOS Research Center (NCRC), researchers demonstrated III-V channel materials using the targeted process flow.

Research on using MOSFETs with ferroelectric gate dielectric has promising results and potential. An application for this structure for a DRAM element has shown that the retention is more than 3 orders of magnitude better than current DRAM technologies (Figure 3).

As feature dimensions continue to scale, the fundamental details of both the etch and deposition processes become increasingly important to reduce variability, roughness, dielectric damage and undesired chemical reactions. For example, the development of robust etching and cleaning processes that can control dielectric trench widths and roughness to within a few atomic layers without degrading the etched low-k dielectric constant have been particularly challenging. Researchers at the University of Michigan are developing a full set of plasma modeling platforms to both fundamentally understand and optimize plasma tools and processes. The researchers at Michigan are collaborating closely with researchers at The Pennsylvania State University, as well as benefiting from a coordinated activity with several other universities. This broad-based effort to both model and experimentally verify the impacts of a wide range of plasma conditions should provide fundamental understanding to improve the plasma processes. It should also spawn revolutionary changes to plasma processing tools that advance plasma processing control to meet the increasingly aggressive needs of the industry (Figure 4).

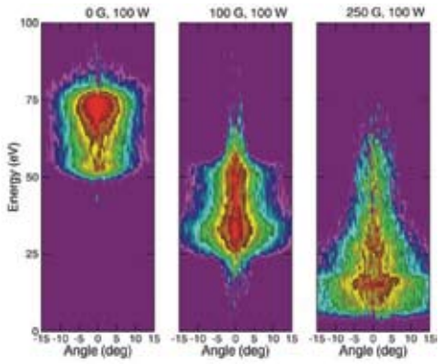


FIGURE 4 University of Michigan researchers model the impact of a transverse magnetic field on the energy and angular distribution of argon ions in an magnetically enhanced reactive ion etching source. The magnetic field both dramatically lowers the ion energy and broadens the distribution.

The SRC/Sematech Engineering Research Center for Environmentally Benign Semiconductor Manufacturing is dedicated to researching the environmental issues of the materials and processes. Beginning in 2008 an open solicitation was undertaken to renew the entire research portfolio. The new research tasks, which are planned to begin in early 2009, include an increased emphasis on nanomaterials and the issues of concern to the semiconductor industry. Funding of the center continues to be shared between SRC and Sematech.

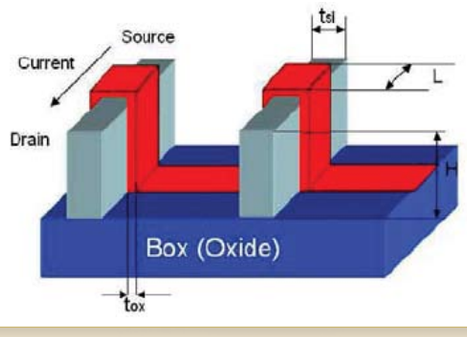


FIGURE 5 FinFET structure that may lead to lower power circuits

RESEARCH FOCUS: APPLICATIONS RESEARCH

A key challenge facing designers of large complex SoCs is finding and fixing all of the flaws in the design, some of which are only apparent after fabrication. Research at Stanford University will make it easier to locate bugs during this post-silicon validation process. Instruction Footprint Recording and Analysis (IFRA) helps bridge the gap between circuit-level and system-level debugging by the insertion of small-area hardware recorders. Algorithms to analyze the recorded information on a super-scalar processor are applied to accurately localize the error with minimal impact on chip area.

As new device structures such as FinFETs become available, fundamental circuit structures can change, giving designers additional opportunities to optimize logical building blocks. Research at Princeton University is re-architecting basic digital cell libraries to take advantage of the FinFET structure to decrease predicted power consumption. Early results show that the use of the redesigned cell library can decrease power by 67%, compared to a conventional library (Figure 5).

One important component of emerging computational paradigms is morphic computation. In the context of chip architectures, this refers to architectures adapted to effectively address a particular problem set, often gaining inspiration from biological or scientific computational paradigms. It appears that this class of structures is a particularly fertile area for the application of novel devices, and even for the extended application of CMOS technologies. One example of a morphic chip architecture is the work at the University of Tokyo. Some of the circuits that support the operation of the associative system yield fully parallel implementations (Figure 6).

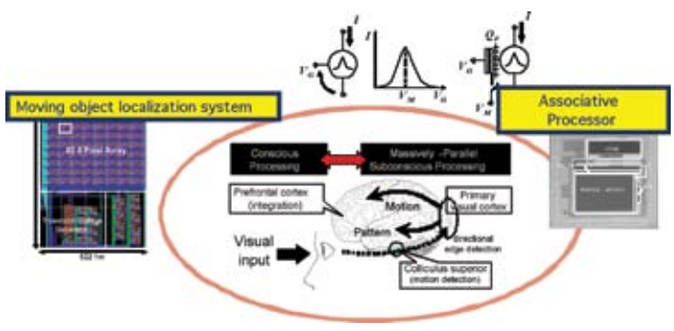


FIGURE 6 A psychologically-inspired brain model architecture for nano-functional-device-based intelligent systems (University of Tokyo)

Texas Analog Center of Excellence (TxACE)

SRC JOINS THE UNIVERSITY OF TEXAS (UT), DALLAS, in forming the newest Global Research Collaboration (GRC) center, the Texas Analog Center of Excellence (TxACE). This center will help shape the landscape for research in analog electronics, a fundamental technology that touches everyone's daily life. TxACE is a $16M collaborative center, funded by the Emerging Technology Fund of the State of Texas, SRC, Texas Instruments, and the University of Texas system.

This center will focus on research in analog, mixed-signal and radio frequency technologies to help address some of the world's biggest challenges in areas such as energy efficiency, healthcare and public safety. The results, expected to be ready for use in devices within five to eight years, should enable integrated circuits for state-of-the-art applications in a wide range of wired and wireless electronics, benefiting markets and people worldwide.

"Analog technology is critically important for connecting digital electronics with the real world," said Dr. David Yeh, SRC's Director for Integrated Circuits and Systems Research, on assignment from Texas Instruments. "Ironically, as almost every electronic device increasingly relies on digital technology advances for improved performance and cost, the need for advances in analog technology also increases."

RESEARCH FOCUS:
ROBUST DESIGN OF CIRCUITS AND SYSTEMS

Manufacturing test has often been considered the unsung workhorse of the design automation area. Yet this area is increasingly important. The ITRS states that "test is not just screening, but a significant value of test is realized in reducing time-to-volume by improving yield learning curves." GRC researchers continue to make progress against these challenges. Significant promise has been shown in research at Portland State University on augmenting test flows with statistical techniques to address increases in systematic and parametric variation of semiconductor designs. Adaptive test strategies to dynamically adjust test flows for yield and test time improvements have shown reductions in test times of up to 60%.

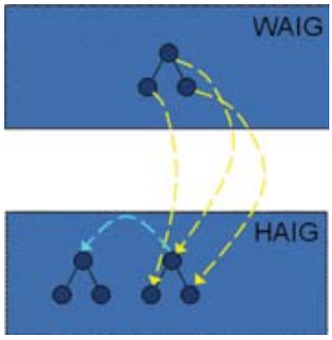


FIGURE 7 Correspondences between a working and-inverter graph (WAIG) and a history graph (HAIG) are recorded during synthesis and used to aid verification.

Verifying hardware designs (and, increasingly, accompanying software) using formal methods has long been a foundational contribution of GRC researchers. With large fractions of the design cycle time devoted to verification, improvements in its speed and its accuracy at detecting bugs is critical to reducing both time-to-market and field failures. While logic synthesis and verification employ similar techniques, they are often pursued separately by different engineering teams. But by performing synthesis and verification in isolation, verification runs the risk of becoming intractable, and synthesis optimizations are avoided because they are hard to verify. Researchers at the University of California/Berkeley have been investigating how to exploit the links between synthesis and verification to improve both processes. They record the synthesis history of a design and use this as input to sequential equivalence checking, resulting in a 4X speedup in runtime and an increase in the reliability of verification. Their model checker, based on the synthesis and verification methods they developed, won the 2008 model checking competition at CAV '08, the 20th International Conference on Computer Aided Verification (Figure 7).

"We go after high-level, complex problems that can only be solved with a multi-disciplinary and highly collaborative approach."

Betsy Weitzman, Executive Director FCRP

FOCUS CENTER RESEARCH PROGRAM

Finding the Ultimate Limits

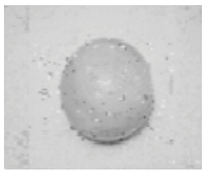
FOUNDED IN 1998, Focus Center Research Program (FCRP) is a cooperative multi-university program sponsored by U.S. industry and the federal government in order to maintain the historic productivity growth curve of semiconductor technology. Each center is managed by a full-time university center director and addresses one of the major areas of technology challenges of the International Technology Roadmap for Semiconductors (ITRS). Currently, this collaborative endeavor to extend CMOS technologies to the end of the transistor roadmap involves 44 universities, 220 faculty and over 550 graduate students. All FCRP research, guided by the university center directors, forges a nationwide effort to keep the United States and its technology firms at the front of the global microelectronics revolution.

FCRP research creates the breakthroughs that are critical to U. S. security and economic competitiveness goals, giving member companies a tremendous advantage in the race to lead the technological revolution. Always long-term and big-picture, FCRP research programs offer mutual leverage to industry and government sponsors. FCRP is also the only university research program that gives the U.S. Department of Defense one-to-one leverage with significant payoff for its investment.

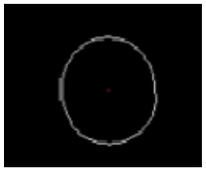
The focus centers themselves are not physical locations, but rather virtual centers, each consisting of multiple universities that engage the leading experts at the participating institutions.

FCRP CENTER HIGHLIGHTS FROM THE 2008 ACADEMIC YEAR

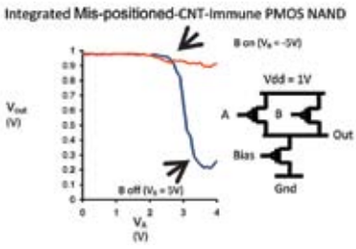
GIGASCALE SYSTEMS RESEARCH CENTER (GSRC)



Received image degraded by poor RF + baseband quality to save power.



Edge detection performed successfully on degraded image.



RESILIENT SYSTEMS DESIGN THEME

GSRC efforts are demonstrating that introspective capabilities integrated into wireless transmission could reduce power requirements and improve transmission performance. Georgia Tech researchers have developed an adaptive wireless system, VIZOR, which adjusts key parameters based on channel conditions, variation and application constraints. This novel approach can take advantage of end application knowledge to which the transmitted or received data is applied to reduce power, reduce error rates and maximize bandwidth. If the wireless system adapts to transmitted image and channel quality, up to 10X power savings is possible over non-adaptive designs for applications, such as edge detection on the received image.

ALTERNATIVE COMPUTATIONAL MODELS THEME

Investigating promising post-Si devices is an ongoing activity in a number of research centers and communities. GSRC researchers have taken a significant step by demonstrating for the first time complete PMOS static logic circuits, such as NAND and inverters, using carbon nanotube field effect transistors (CNFETs).

The measured DC voltage transfer curve of a PMOS NAND gate, shown at left, indicates that the static logic circuits can be designed using CNFETs. This result opens up the possibility of designing more complex circuits and systems using CNFETs and studying power, delay and reliability issues. This work was done jointly with C2S2 and FENA research centers.

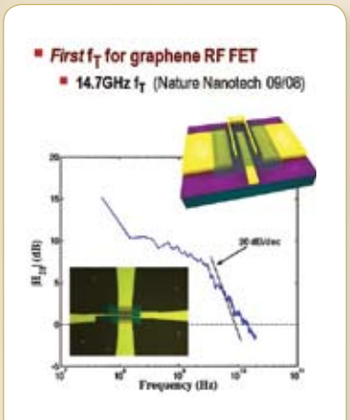
CENTER FOR CIRCUITS & SYSTEMS RESEARCH (C2S2)

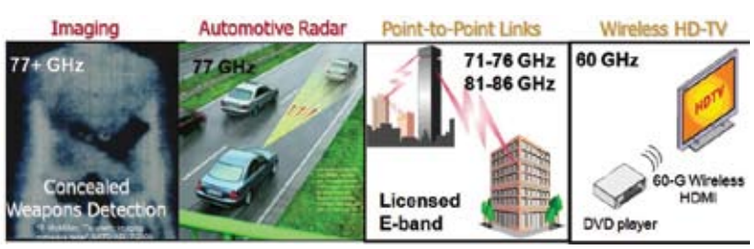
ANALOG CIRCUITS AND INTERFACES THEME

Given recent speed gains in SiGe and CMOS technologies, researchers are beginning to look at mm-wave, extremely high-frequency applications that can leverage these technologies. C2S2 researchers are working on a range of projects in antenna circuits, integrated front-end receivers, DSP at very high (GHz) IF, and mostly digital beamforming. A particularly exciting achievement is the first-ever fully integrated 60GHz transceiver including RF, local oscillator, phase lock loop and baseband integrated into a single chip. Data transmission up to 5 Gbps on each of I and Q channels has been measured, as has data reception over a 1 m wireless link at 4 Gbps QPSK with less than 10-11 bit error rate. This is the largest mm-wave integrated design ever reported.

EMERGING CIRCUITS AND APPLICATIONS THEME

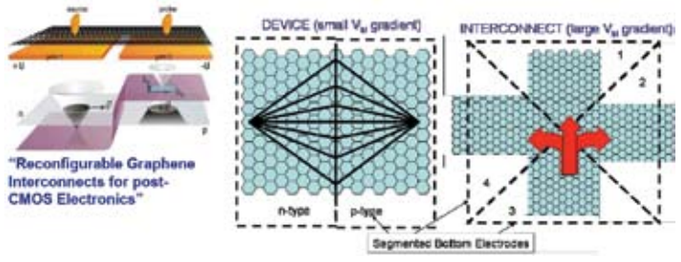
Graphene has recently emerged as a promising material for post-silicon devices. Although it has a challenging on/off current ratio for switching, it may be useful in RF applications. C2S2 researchers were able to complete the first-ever measurement of the f_T (unity gain frequency) for a top-gated graphene FET used in an analog circuit context. This result appeared in *Nature Nanotech* in September 2008.





Applications areas for mm-wave CMOS

INTERCONNECT FOCUS CENTER (IFC)

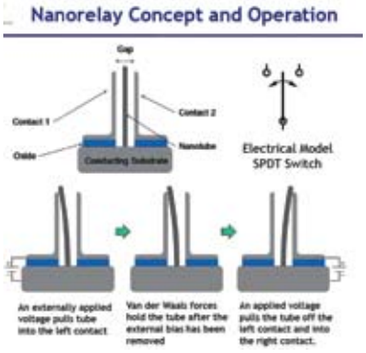


ELECTRICAL INTERCONNECTS THEME

IFC researchers are currently fabricating reconfigurable graphene structures for interconnect applications that exploit the optics-like manipulation of electrons in graphene. These structures are based on electrostatically defined p-n interfaces for total reflection, focusing, or transmission of carriers, depending on the abruptness of the p-n interface. Using electrostatic gating, this approach has the potential to demonstrate p-n interfaces that can direct (reconfigure) the flow of carriers. This approach does not require fine-line patterning of graphene and is expected to be less sensitive to band-gap opening.

THERMAL MANAGEMENT, POWER DELIVERY, & NEW MATERIALS INTEGRATION THEME

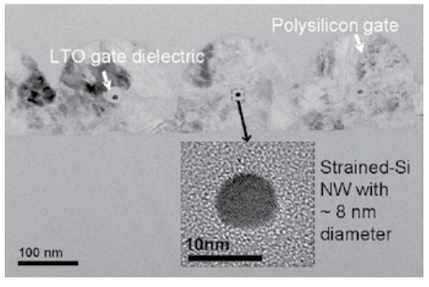
Power consumption is one of the most important problems facing the electronics industry, and with continued transistor scaling, leakage currents continue to be a major contributor to the power drain. A vertical carbon nanotube-based (CNT-based) NEMS switch with virtually no off current is being developed as a potential solution for low leakage applications. Switching of the nanorelay is accomplished by applying an appropriate voltage to the CNT; after the voltage is removed, Van der Waals forces maintain contact between the CNT and metal electrodes.



MATERIALS, STRUCTURES AND DEVICES RESEARCH CENTER (MSD)

CMOS EXTENSION: SI:GE CHANNEL MATERIALS AND DEVICES THEME

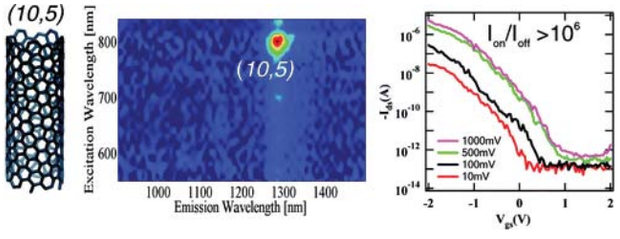
The MSD Center recently demonstrated significant progress in channel engineering, fabricating and characterizing the performance of the first uniaxial tensile-strained Si nanowire gate-all-around (GAA) n-MOSFETs, with nanowire dimensions down to 8 nm. These devices combine the performance enhancement of uniaxial strained Si with the potential for superior MOSFET scalability associated with the GAA architecture. Details were presented at the 2008 IEDM Conference.



Cross-section TEM image of a GAA strained-Si n-MOSFET, looking down the axis of the nanowires in the device channel, showing parallel nanowires with diameter ~ 8 nm, and LTO gate dielectric.

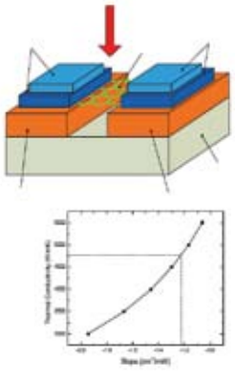
CMOS EXTENSION/CMOS PLUS: NANOWIRES AND NANOTUBES THEME

An elusive goal for the carbon nanotube electronic device research community has been to achieve high performance single-walled carbon nanotubes (SWNTs) field effect transistors (FETs) comprised of only single chirality SWNTs. This is believed to be essential to obtain high on/off current ratio and minimize device variations. The MSD Center has demonstrated separation of single chirality (10,5) SWNTs from high-pressure carbon monoxide process tubes with ion exchange chromatography enhanced by a new DNA sequence, which can recognize SWNTs with the specific chirality (10,5). FETs comprising separated SWNTs in parallel gave I_{on}/I_{off} ratio up to 106 owing to the single chirality enriched (10,5) tubes. This is the first time that SWNT FETs with single chirality SWNTs were achieved.



Emission spectra and FET I_{on}/I_{off} ratio for single chirality enriched (10,5) SWNTs

FUNCTIONAL ENGINEERED NANO ARCHITECTURES CENTER (FENA)



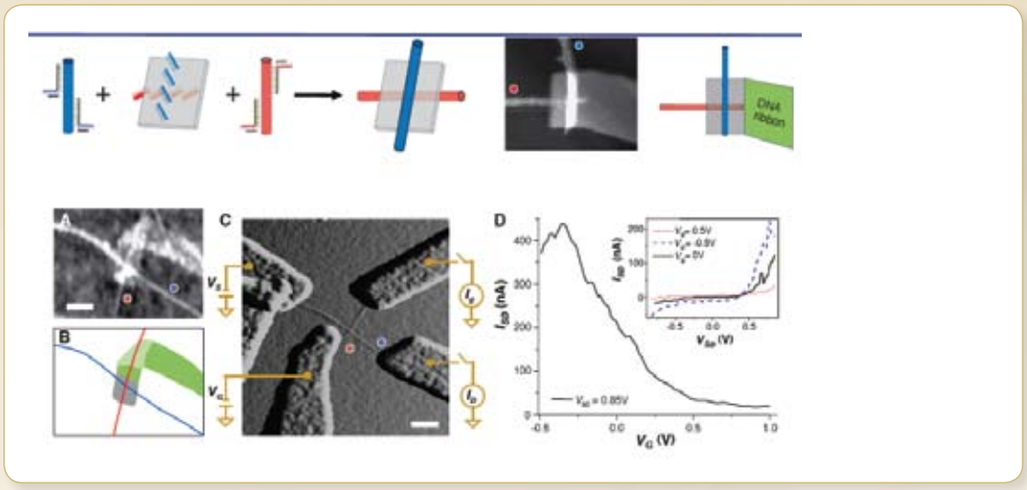
Schematic of the experiment used in the simulation (top); calculation of the thermal conductivity of graphene from the slope $\theta^{1}=(\delta P/\delta\omega)$. The numeric value (upper limit) is close to the one obtained in the experiment (bottom).

NANODEVICES THEME

FENA researchers have recently discovered that graphene has very high thermal conductivity, exceeding that for carbon nanotubes. They have made measurements of the thermal conductivity of the few-layer graphene flakes suspended across trenches in silicon wafers. Preliminary results obtained for graphene flakes with n=2, 3 and 4 atomic layers suggest that the thermal conductivity reduces with the increasing number of layers, approaching that of graphite basal planes. They also found using theoretical analysis that the near room-temperature thermal conductivity of single layer graphene can vary over a wide range, depending on the defect concentration and roughness of the edges.

NANO STRUCTURES AND PATTERNS THEME

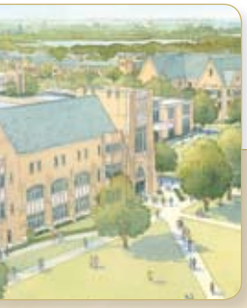
FENA researchers demonstrate unprecedented control over the nucleation of ribbons of DNA tiles, controlling their width, pattern or a computation embedded within them. The capstone achievement, the nucleation of a binary counter, is shown in figure below. They also did exciting research on the organization of carbon nanotubes with DNA "origami", as well as the placement of "origami" on silicon surfaces.



Two dimensional organization of carbon nanotubes on DNA "origami"

"NRI is looking for the next switch to propel technology beyond its current limits."

Jeffrey J. Welser, Director, NRI



NANOELECTRONICS RESEARCH INITIATIVE

Discovering Beyond the Known

NANOELECTRONICS RESEARCH INITIATIVE (NRI) is a consortium of companies in the Semiconductor Industry Association seeking to find a device that can scale computer technology beyond the ultimate limits of current CMOS transistors. This university-based research, cooperatively funded by industry and federal and state governments, is looking toward nanoelectronics in the year 2020 — further out than anyone else. With a goal of discovering the next switch — a new mechanism for computing that goes beyond simply improving today's transistor — NRI engages the most talented students to become the innovators and leaders of tomorrow's technology industry.

Groundbreaking NRI research is currently being conducted at over 30 universities. The projects are organized into multi-university centers (WIN, INDEX, SWAN and MIND) and at NSF nanoscience centers (NSF-NRI joint projects). And given the exploratory nature of the research, which seeks out entirely new device and computation technologies, it is particularly important that industry and academia work together closely to rapidly identify and develop emerging research paths that show potential to extend the historical cost and performance trends for information technology.

NRI-NIST RESEARCH CENTERS

With the addition in late 2007 of NRI's newest partner, National Institute of Standards and Technology (NIST), NRI was positioned to greatly expand its core research program at its multi-university centers. NIST serves as a full partner on the NRI technical and governing boards, not only contributing funding to NRI centers, but also being integrally involved in the proposal review process to choose new projects during the expansion.

The most notable expansion result during 2008 was the launch of a new center, the Midwest Institute for Nanoelectronics Discovery (MIND), headquartered at the University of Notre Dame. This center brings in a new group of professors and students and expands the technical scope of the program, as NRI continues to look for the "next switch". The member universities, the state of Indiana and — for the first time in SRC's history — the city of South Bend all contributed leverage funding to help make the center a reality.

Midwest Institute for Nanoelectronics Discovery (MIND)

2008 MARKED THE LAUNCH OF THE NEWEST Nanoelectronics Research Initiative (NRI) Center —the Midwest Institute for Nanoelectronics Discovery (MIND). The $61 million research center, headquartered on the prestigious campus of the University of Notre Dame, is the latest collaboration among academia, technology industry members and government, including the NRI's newest federal partner, the National Institute of Standards and Technology (NIST). As with all innovative NRI research, the focus of MIND is the development of alternatives to today's semiconductor technology, opening new doors toward the next nanoscale logic device.

"Thanks to efforts by NRI, the State of Indiana, the City of South Bend and IBM, MIND researchers will work in collaboration to enable future breakthroughs in nanoelectronics," explains Dr. Jeff Welser, NRI Director. "Semiconductor technology is the underpinning to everything from the cell phones in our pockets to the supercomputers in our research labs, so nanoelectronics progress is crucial to innovation —not only in all areas of science and technology, but to our nation's continued economic growth."

The MIND center will be led by Notre Dame and include a network of universities, including Purdue University, University of Illinois, The Pennsylvania State University, University of Texas/Dallas and University of Michigan. The university researchers will also be engaging with NIST, the Argonne National Laboratory and the National High Magnetic Field Laboratory in this pioneering research effort.

WIN: Western Institute of Nanoelectronics, UCLA (Kang Wang, Director): Focuses solely on spintronics and related phenomena for logic applications, including materials, device structures and interconnects. In addition to its NRI funding, this center receives additional direct support from Intel and the UC Discovery program.

INDEX: Institute for Nanoelectronics Discovery and Exploration, SUNY-Albany (Alain Kaloyeros, Director): Focuses on a broad range of phenomena for logic devices, organized in centers of competency around excitronic, quantum-dot spin, magnetic, and graphene devices, with emphasis on fabrication and characterization. INDEX also receives additional direct support from IBM and New York State.

SWAN: SouthWest Academy for Nanoelectronics, UT-Austin (Sanjay Banerjee, Director): Focuses on a large graphene program, which integrates projects on theory, material fabrication, device structures and metrology, as well as work on magnetic materials, pseudospintronics, magnetic and multi-ferroic materials, and plasmonics. In combination with its NRI funding, SWAN receives support from TI and the Texas Emerging Technology Fund.

MIND: Midwest Institute for Nanoelectronics Discovery, Notre Dame (Alan Seabaugh, Director): Focuses on tunneling and non-equilibrium phenomena for energy efficient devices and architectures, as well as thermal phonon management. In addition to NRI funding, MIND receives additional support from IBM, Indiana and the City of South Bend.

With the newest center (MIND), the NRI-NIST program now has research projects at over 30 universities in 20 states across the country. While all of the centers are working on research aimed at finding a new logic switch, the focus of the programs at each center has its own specific character.

Highlights of the work in 2008 from the three original centers are shown in Figures 1 through 3.

In addition to being a substantial funding partner, NIST brings a deep technological expertise to NRI's research. Six joint projects were identified during 2008 alone — some new and some existing collaborations now being leveraged to extend NRI research. Nanometrology and characterization are keys to any advances in nanoelectronics — particularly in trying to link experimental work to theory. The expanding NIST-NRI partnership will help guide the continued work on new characterization tools to those most vital for developing and characterizing the next generation of nanoelectronic devices. By working closely with NRI university and industry researchers, the results of any new capability will have much more rapid impact on future device and product innovations.

NRI-NSF PROJECTS

During 2008 NRI continued — and expanded — its partnership with the National Science Foundation (NSF). NRI-related projects were jointly funded at the existing NSF nanoscience centers across the country, including the Nanoscale Science and Engineering Centers (NSECs), Materials Research Science and Engineering Centers (MRSECs), and the Network for Computational Nanotechnology (NCN). NRI currently supports 18 projects at 12 NSF centers, which range from advanced computer simulation of spin-based devices, to measurements of non-equilibrium coherent transport in single-layer graphene sheets, to directed self-assembly of quantum dot and wire structures for novel devices. (See Figure 4 for a 2008 program highlight.)

This joint investment with NSF is mutually beneficial, with NRI gaining from NSF center knowledge, and the NSF centers benefiting from NRI's industry involvement.

YEAR-END RESULTS

At the end of 2008, the third Annual NRI Review was held at NSF in Arlington, VA. In order to further NRI's interaction with the NSF nanoscience centers, as well as other government agencies in the Washington, DC area, the review was combined with the NSF Annual Grantees' Conference. The event was attended by over 100 individuals, coming from all of the NRI centers, member companies and government agencies, and the feedback was overwhelmingly positive.

In particular, the sponsors were impressed with the strong focus of the basic science work in all centers around specific device ideas across universities. One industry member summed it up by saying, "The NRI experiment is working. For understanding graphene, for example, the NRI [academic team] is probably the best in the world. We learned more about graphene for applications in the last two years than we would normally learn in five or more years due to the NRI focus on science for devices." This is precisely the intended purpose of forming NRI as a goal-oriented, basic-science research program, and indicates NRI is well positioned to achieve its goals in the coming year.

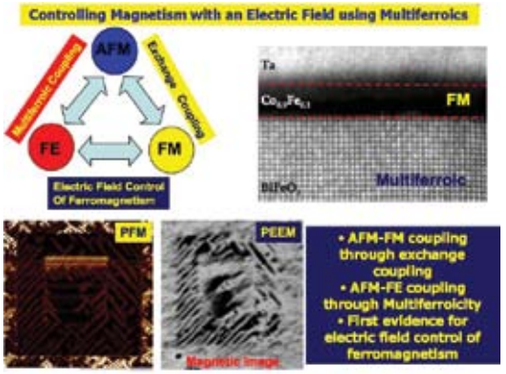


FIGURE 1: Multiferroic Materials
First demonstration of control of ferromagnetism with an electric field applied to a multiferroic material. Indicates the possibility of using simple electric field to control spin or other correlated properties. (University of California/Berkeley)

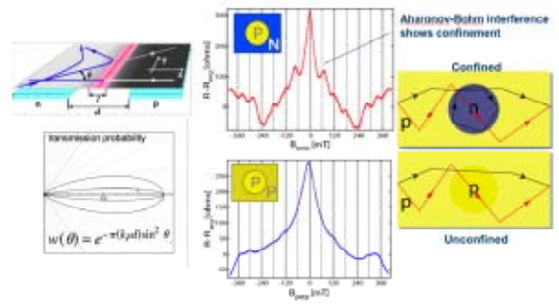


FIGURE 2: P-N Junctions in Graphene
Experimentally characterized transport across graphene p-n junctions, as well as trapping due to total internal reflection in n-p-n island structures, consistent with theory. Crucial to understanding of the p-n "puddles" that dominate current graphene structures, and for future Veselago Lens devices. (Harvard University)

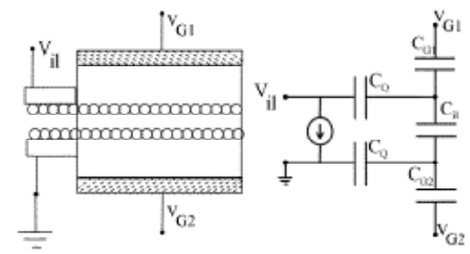


FIGURE 3: Bi-layer pseudoSpin FieldEffect Transistor (BiSFET)
Proposed a new device based on Pseudospintronics: Bi-layer pseudoSpin Field Effect Transistor (BiSFET). Utilizes the correlation between electrons and holes in a coupled bi-layer graphene structure to move large charge "pulses" between layers with mV potentials. (University of Texas/Austin)

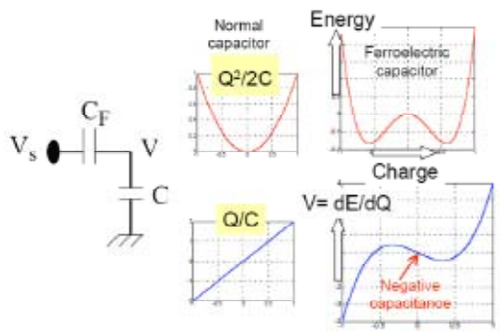


FIGURE 4: Negative Capacitance Voltage Transformation
Introduction of the negative capacitance concept, which identifies the theoretical possibility of using a ferroelectric capacitor to obtain sub-Vt swings of less than 60 mV/dec at room temperature. Possibility for lower voltage / lower power dissipation in devices, as well as non-equilibrium carrier behavior. (Purdue University)

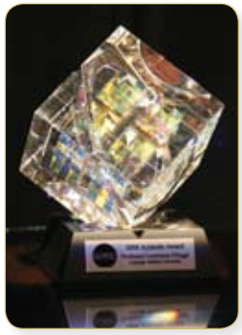
TECHCON 2008

EACH YEAR SRC sponsors TECHCON, a premier technical conference focusing on the semiconductor industry. This event showcases the quality of the SRC research portfolio, the excellence of SRC students and faculty, and the magnitude of the collaborative research investment made by the semiconductor industry through SRC. TECHCON 2008, hosted at the Renaissance Hotel in Austin, Texas on November 3 and 4, marked the tenth anniversary of the conference and proved to be one of the most successful events to date. Sessions reflected all SRC entities, with 144 student-presented technical papers and posters representing a broad cross-section of SRC-funded research. Eighteen students won Best-in-Session Awards, with industry judging based on technical content, perceived value, technology/information transfer and presentation.

Total attendance reached 346, including 138 industry participants, 18 faculty, 158 students and 30 others (staff, etc.), making for outstanding networking and technical exchange. Among the attendees were 40 alumni of SRC student programs who are now maintaining connection with SRC for their current organizations.

The keynote address was given by former SRC student, Dr. Lisa Su, currently Freescale Senior Vice-President and General Manager of the Networking and Multimedia Group. Professor Allan MacDonald, NRI researcher at University of Texas/Austin, presented the Special Session, "New Frontiers in Device Research and Application." Both speakers provided glimpses into the very exciting future of the semiconductor industry.

A new event for TECHCON this year was a faculty lunch, hosted by SRC's Dr. David Seeger, Vice President of Strategic Planning and Business Development. Dr. Seeger presented an overview of the future directions for SRC-sponsored projects. Dr. Steven Hillenius, Executive Vice-President, SRC and Executive Director, GRC, as well as Ms. Betsy Weitzman, Executive Vice President, SRC and Executive Director FCRP, were also in attendance and gave overviews of their respective programs. A lively discussion and information exchange followed as the faculty asked questions of the SRC team.



Inventor Recognition Awards recognize those university researchers whose creativity and innovations lead to patentable inventions, thereby increasing the competitiveness of SRC member companies. This year 47 innovative research faculty and students were recognized for this prestigious award during TECHCON 2008 in November.

The Aristotle Award recognizes excellence in teaching through the research process, as well as an exceptional commitment to students. Professor Lawrence Pileggi was a student on SRC's first contract at Carnegie Mellon University (CMU), and has continued to be an integral part of SRC-sponsored research in his role as CMU faculty. Dr. Pileggi currently holds research contracts with both GRC and FCRP.

2008 TECHNICAL EXCELLENCE AWARD

The Technical Excellence Award is an incentive and recognition program for research of exceptional value to GRC members. The award is shared among key contributors for innovative technology that significantly enhances the productivity and competitiveness of the semiconductor industry.

W. Robert Daasch

The 2008 Technical Excellence Award was presented to a team of researchers from Portland State University, led by Professor W. Robert Daasch and supported by students Liwei Ning (PhD, 2009) and Amit Nahar (MS, 2006, now with Texas Instruments), for their research, "Burn-in Reduction: Improving Outlier Screening". The team is a pioneer in the area of statistical analysis for outlier identification and their work has made a significant impact on testing and test data analysis within a member company. A $5000 cash award was presented to the team of research contributors.

Student Programs

SINCE 1982 SRC has supported over 7,000 students as part of its unique collaborative research model. Of the SRC-supported students, nearly 60% of graduates have joined sponsoring organizations or university faculties, or have continued on to pursue a higher degree. These students provide a path for technology transfer and an invaluable source of relevantly educated technical talent for the industry.

Member companies benefit greatly from SRC-sponsored student programs, as these organizations gain valuable access to this pool of talented, experienced student researchers. Member company personnel can search a database of supported students on SRC's secure website to find students whose backgrounds meet their interests. And many sponsored events around the country also allow industry recruiters the opportunity to meet and interact with students.

2008 HIGHLIGHTS

- 39 SRC student alumni represented their companies as members of various SRC technical advisory boards, and another 187 acted as mentors to SRC research projects.
- 81 former SRC students had active research funding with one or more SRC entity.
- Over 1,500 students participated in SRC research across GRC, FCRP and NRI, with 204 completing MS or PhD degrees.
- At the beginning of the 2008 fall term, 33 GRC Fellowships, 1 NRI Fellowship, and 11 SRCEA Master's Scholarships were in place. These programs are designed to attract academically qualified students with US citizenship or permanent resident status to relevant semiconductor research.
- Student/industry networking events were held at Southern Methodist University, University of Albany/SUNY, University of Florida, Carnegie Mellon University, UCLA, MIT, University of California/Berkeley and Georgia Tech.
- The 2008 Simon Karecki Award was presented to Yasa Sampurno, University of Arizona, at the Center for Environmentally Benign Semiconductor Manufacturing Review.
- Phase 1 of the SRC/SIA IC Design Challenge: *Performance at the Limits* was completed with winners announced at TECHCON 2008. First place went to the team from Purdue led by Professor Byunghoo Jung.

Eighteen students won Best in Session Awards at TECHCON 2008, presented by Dr. David Seeger, Conference General Chair (standing left).

For further information on SRC Student Programs, please refer to About SRC Student Programs online at www.src.org/member/students/about.asp.

Back Row Henning Braunisch, *Intel;* Kemal Aygun, *Intel;* Stefan Zollner, *Freescale;* Magdy S. Abadir, *Freescale.* **Front Row** Anne E. Gattiker, *IBM;* Friedrich J. Taenzler, *Texas Instruments;* Taras A. Kirichenko, *Freescale.* **Not pictured** Ruchir Puri and Robert Rosenberg, *IBM.*

2008 MAHBOOB KHAN OUTSTANDING MENTOR AWARD WINNERS

The GRC Industrial Liaison Program is a powerful partnership that brings together university researchers, graduate students and semiconductor industry experts. The program allows member companies to effectively extract value from GRC, and it gives students an increased breadth of academic experience through real-world industry research. As an integral part of the research team, Liaisons are actively involved in task planning and guidance throughout the process, and the long-term relationships formed in the program impact and enrich the lives of both mentor and student.

The Mahboob Khan Outstanding Mentor Award, named in memory of longtime program advocate from AMD, is presented to those individuals who have made significant contributions in their roles as Industrial Liaisons. These recipients represent "ideal mentors" whose commitment meaningfully enhances the GRC research program.

SRC Impacts Students…
And SRC Students Create Impact.

COMBINING ACADEMIA AND INDUSTRY, THE SRC student fellowship programs engage the brightest students of technology and science in use-inspired research that makes a real difference. Students are able to attend the best universities for their particular focus, universities get to accept the most talented technology students, and industry members have access to the research integral to their success. There is no other organization that provides the synergy of SRC student programs.

And although most students will never forget their SRC experience upon completing their studies, sometimes the impact is so profound that these same students give back to SRC in a new capacity: *as advocate, teacher, mentor.*

Lisa Su and Larry Pileggi are two shining examples of former SRC students who have not only gone on to enjoy impressive semiconductor careers in industry and academia, respectively, but they have also chosen to maintain a relationship with SRC for future generations of students and technology innovation.

LISA SU

Then: SRC-sponsored student at Massachusetts Institute of Technology (MIT) from February 1991 to September 1994

Now: Senior V.P. and General Manager of Networking and Multimedia Chief Technology Officer, Freescale Semiconductor

Impact: Dr. Su has been an outspoken advocate for SRC within two member companies — first with IBM and now with Freescale. Her ongoing participation with SRC keeps her organization engaged in the SRC model, maintaining a mutually successful partnership.

LARRY PILEGGI

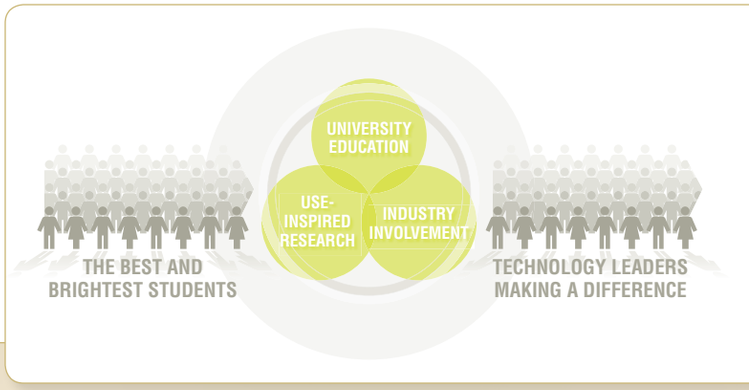
Then: SRC-sponsored student at Carnegie Mellon University (CMU), graduating in April 1989

Now: Tanoto Professor of Electrical and Computer Engineering at CMU

Impact: Professor Pileggi currently holds research contracts with both GRC and FCRP and is dedicated to preparing students for a career in the sciences, as well as inspiring them to use their skills for the betterment of humanity.

"SRC supports the university research that establishes the foundation for the industry, and provides the next generation of engineers and scientists. It is through these two actions that SRC helps the industry be competitive around the world."

Craig Barrett, Chairman of the Board, Intel Corporation



SRC EDUCATION ALLIANCE

Producing Leaders. Making a Difference.

INSPIRING THE FUTURE OF TECHNOLOGY

For over 25 years SRC student programs have been changing lives. Bringing together universities and industry, these programs engage the brightest students of science and technology in research that makes a significant difference. Students work with faculty who are recognized experts in their respective fields. The industry-driven, high-impact research with which they are involved gives them the relevant experience necessary to establish a rewarding career after graduation.

During 2008 SRC set into motion plans for expanding the Education Alliance to leverage past successes and broaden its impact. As a private foundation, the Education Alliance will develop sources of funding beyond its industry members, increasing the ability to attract and support a wide diversity of students at various levels of education.

TODAY'S STUDENTS, TOMORROW'S LEADERS

Now, more than ever, opportunities abound for technologically educated individuals to make a difference in areas that are important to the economy and industry, as well as to national security and quality of life. Many of these opportunities are with high-tech industries that need bright and passionate talent to effectively innovate and compete.

Through fellowships and scholarships, the Education Alliance will connect students with the science- and technology-based industries, and show them how to transform research results into useful products that create change.

EXPANDING PARTNERSHIPS, INCREASING IMPACT

The Education Alliance is poised to amplify its impact through increased student support and the development of new programs for science teachers and younger students. From tackling energy challenges and improving healthcare delivery, to strengthening security around the world, these students will become tomorrow's innovators and leaders.

The SRC model of connecting students, faculty researchers and industry experts has been consistently proven over the past quarter-century. The prospect of effective growth will not only attract more quality students and improve student retention, it will ultimately increase the benefit to innovation-based companies and university partners.

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APPLIED MATERIALS, INC. | FCRP, GRC

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HEWLETT-PACKARD COMPANY | GRC

IBM CORPORATION | FCRP, GRC, NRI

INTEL CORPORATION | FCRP, GRC, NRI

LSI CORPORATION | FCRP, GRC

MENTOR GRAPHICS CORPORATION | GRC

MICRON TECHNOLOGY, INC. | FCRP, NRI

NOVELLUS SYSTEMS, INC. | FCRP, GRC

ROHM AND HAAS ELECTRONIC MATERIALS | GRC

TEXAS INSTRUMENTS INC. | FCRP, GRC, NRI

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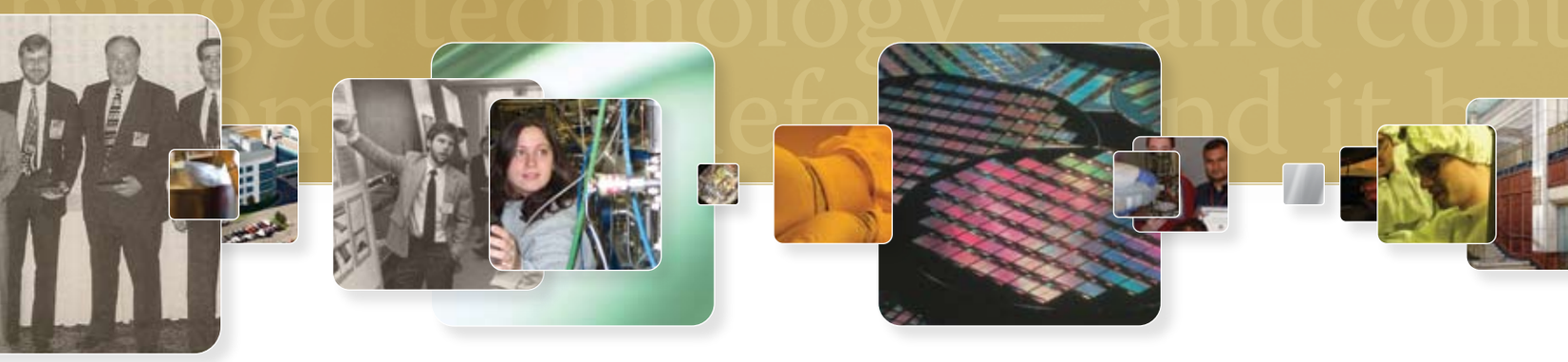

1101 Slater Road
Brighton Hall, Suite 120
Durham, North Carolina 27703

P.O. Box 12053
RTP, North Carolina 27709-2053
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