THE **VALUE** OF **members**

SRC® Semiconductor Research Corporation

2009 **Annual Report**


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VALUE. The word carries a connotation of worth and significance, of a good return for something exchanged. Semiconductor Research Corporation is always striving to create value — to society, academics, industry and the global economy. SRC also understands that its programs must contribute to the value creation enterprises of its Members and thereby provide value to them. But it is also the commitment and dedication of our Members that create the significance behind all we accomplish. This is the value of Membership. ***And it's the very foundation upon which SRC is built.***

In the early 1980s, the U.S. semiconductor industry found itself facing intensifying international competition. Without an adequate inflow of research ideas addressing industry technology needs, or access to university graduates who were knowledgeable about semiconductor sciences and technologies, something had to be done. Led by the Semiconductor Industry Association (SIA), the industry adopted the radical idea of jointly funding pre-competitive university research programs whose results would be shared by all sponsoring (and fiercely competitive) companies… creating incredible, immense value for all entities involved.

The result of this unique industry inspiration was the creation of Semiconductor Research Corporation. From its inception, SRC has been charged with determining industry needs in order to continuously increase integrated circuit functionality at lower cost, and funding the exceptional university research required to accomplish this. The global impact of SRC over the past three decades is immeasurable. But equally profound is the resulting value to our Members. Not only are research results delivered quickly and efficiently, but Member companies also gain access to the most talented, relevantly educated graduates the world has to offer.

And we greatly value our Members… in fact, SRC defines itself in terms of its ability to meet and exceed Member expectations.

A Letter from Larry W. Sumney,
President & Chief Executive Officer

THE LIFEBLOOD OF ANY CONSORTIUM is the ongoing commitment it must earn from its Members as they continuously assess the value that the consortium provides in return for their investment of resources. Since its foundation, SRC has held the guiding principle of making every effort to maximize value for our Members. Our operations are designed to be responsive to Members in every facet of our activities—from the creation of excellent, relevant university research programs and the support of outstanding graduate students and faculty, to the rapid dissemination of research results to our Members and the implementation of an intellectual property policy designed to maximize freedom of action by Members in applying research results. The results from our annual Member satisfaction surveys are gratifying to us because they consistently reflect a high degree of Member satisfaction regarding the value of SRC research to them.

Nevertheless, we must strive to identify additional venues to increase the value perceived by our loyal Member companies, as well as offer attractive value-incentives to non-members that would entice them to participate in SRC programs—a true challenge in today's dynamic environment where companies rapidly respond to new business opportunities while eschewing other business lines that have been historically important to them.

When 2009 began, no one knew what to expect. Market conditions were seemingly worsening by the minute, and visibility was extremely poor. This made an already dynamic industry very challenging to determine what course to take. Understandably, this also made it more difficult for many to commit to research and development that offers a future. However, SRC and its Members knew that even in the midst of one of the most extreme economic cycles, research is the key to innovation and growth of our industry; so continued investing through this major economic downturn was the best approach.

Our strategy for increasing Member satisfaction in this environment of change has several facets:

- *SRC will continue its historical focus on all aspects of silicon technology, while providing as much latitude as possible for Members to focus on those aspects of silicon technology important to their specific business focus.*
- *The expanding application space for semiconductor-based systems offers new opportunities to serve companies within the SRC family and engage non-member companies as well. SRC has developed new participation mechanisms for initiatives in emerging areas such as nanoelectronics, energy, bioelectronics, secure information systems, etc. We believe that as new participants in these initiatives comprehend the value of pre-competitive research in response to industry needs, they may wish to expand their participation in SRC to other core programs. In order to increase participant value, SRC will undertake development of government support for these initiatives.*
- *SRC continues to maximize value to our Members and sustain a clear focus on excellence in everything we do by maintaining a staff of the highest quality and selecting the very best university researchers.*

As we move forward, SRC shall not deviate from the proven worth of providing high value to our Members, and promise to consistently sustain a "Members-first" attitude throughout the organization.

Sincerely,

Larry W. Sumney, President & CEO

About SRC

A PROVEN PAST

When the U.S. semiconductor industry recognized that it was rapidly losing market share to formidable competitors, their response was novel and unexpected. Led by the Semiconductor Industry Association (SIA), the industry adopted the radical idea of jointly funding generic pre-competitive university research programs whose results would be shared by all sponsoring (and fiercely competitive) companies. This was the genesis of Semiconductor Research Corporation.

Formed in 1982, SRC was given the mandate to rapidly create and operate a U.S. university research program to address the long-term needs of the industry. In response, SRC has created a unique industry consortium that not only has built a significant research infrastructure for rapid delivery of research results, but also provides Members with capable and relevantly educated talent.

PARTNERING FOR SUCCESS

The operational models established in the early days of SRC have gradually been refined over time to emphasize Member satisfaction and continuous process improvement. One unique attribute of SRC's research program is that it strives to create partnerships between university researchers and the industry Sponsors. With each project assigned at least one industry liaison, the researchers receive the vital consultation and support they need to maximize their research. And through SRC's web-accessible and interactive database housing thousands of technical research results documents, industry Sponsors receive timely delivery of research results.

freescale™ semiconductor

FREESCALE SEMICONDUCTOR, INC. is a global leader in the design and manufacture of embedded semiconductors for the automotive, consumer, industrial and networking markets. The privately held company is based in Austin, Texas, and has design, research and development, manufacturing or sales operations in more than 20 countries.

The company's rich history of embedded solutions goes back more than 50 years to when it was a subsidiary of Motorola. Freescale's portfolio of power management solutions, microprocessors, microcontrollers, sensors, radio frequency semiconductors, analog and mixed signal circuits and software technologies are embedded in products used throughout the world.

Please visit www.freescale.com for more information about Freescale Semiconductor.

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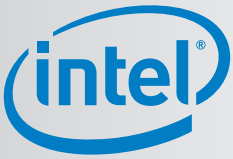
"SRC's Global Research Collaboration provides a unique framework, along with the management skill, to develop and facilitate high quality research projects on topics of importance to Freescale."

KEN HANSEN | Sr. Fellow, Vice President and Chief Technology Officer | Freescale



INTEL CORPORATION (NASDAQ: INTC), the world leader in silicon innovation, develops technologies, products and initiatives to continually advance how people work and live. Intel pushes the boundaries of innovation so its work can make people's lives more exciting, fulfilling and manageable. Originally founded as a memory company, microprocessors for client and server computers have come to be its most important product. Intel's history of developing groundbreaking technology continues today. From 2001 through 2008, Intel invested more than $80 billion on R&D and new capital expenditures.

Owning, investing and expanding its in-house manufacturing network has proven to be Intel's greatest advantage and remains a top priority. Innovations such as high-k metal gate transistors are bringing performance and energy efficiency increases to established processor markets—and creating entirely new industry opportunities through mobile internet devices, netbooks (low-cost notebook PCs), connected CE equipment and other embedded computers.

Please visit www.intel.com for more information about Intel.

Over its 27-year history, SRC has supported 8287 students—a large percentage of whom obtained a Ph.D. And because SRC is able to anticipate long-term technical needs and create highly innovative programs that respond to those needs, the research emerging from SRC programs has had a significant impact on the operations of Member companies.

GLOBAL IMPACT

As SRC has maintained a steady focus on its mission of university research in support of the semiconductor industry, the global nature of the industry – and the economy – has greatly broadened the original SRC vision. Driven by this recognition that today's research needs and expertise are global, as well as the fact that sustaining progress in the far nanometer regime will require the world's best collective efforts, SRC expanded its original "core" research program to accept sponsorship by international companies and participation by non-U.S. universities. To date, projects have been undertaken at over 50 universities outside the United States and are producing excellent research results and graduates.

Looking ahead, SRC is well positioned to address the technology challenges faced by the semiconductor industry and to apply its management methodologies to the resolution of societal needs for clean energy, improved technologies for healthcare, and many other areas. The semiconductor enterprise landscape is different today than in 1982, but it remains very dynamic. SRC looks forward to making a continued valuable impact… on our Members, our researchers and the world.

"Intel has been a supporter of SRC since its founding. SRC provides a unique opportunity for the electronics industry to engage collaborative, pre-competitive research at the world's leading universities. This not only provides seed ideas which can blossom into tomorrow's technologies, it also serves to educate the researchers of the future who will help implement those ideas."

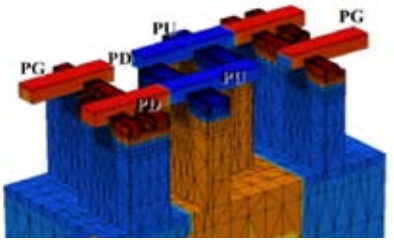
MICHAEL MAYBERRY | Vice President, Technology; Manufacturing Group Director, Components Research | Intel

Global Research Collaboration
Advancing the Next Big Thing

Research sponsored by Global Research Collaboration (GRC) emphasizes the key critical challenges defined in the International Technology Roadmap for Semiconductors (ITRS). The research achievements for 2009 are focused on the continued scaling of large systems and the associated manufacturing and design challenges that emerge. The common themes that have surfaced in the research results are the progress in developing three-dimensional (3D) structures at the device, interconnect and package levels. The manufacturing challenges that result from the smaller dimensions and the 3D integration have required more accuracy in the simulation tools, the feature size control and the ability to verify and test the resulting products. System architectures and circuit design methodologies must now comprehend the use of multicore technologies. These circuits and systems need to be robust to manufacturing variations and uncertainties in the circuit configurations. In addition to these challenges, the need for low-cost, environmentally benign manufacturing techniques has inspired tremendous progress in the area of self-assembly and low material use processes.

DEVICE STRUCTURES

Researchers at UC/Berkeley are exploring an evolutionary pathway for scaling bulk-Si CMOS technology to the end of the roadmap. The segmented transistor structure can be fabricated using a standard bulk-Si CMOS process flow, starting with corrugated Si wafers comprising Si stripes of uniform width (and low aspect ratio, ~1) isolated by very shallow trench isolation oxide, so the transistor width is divided into multiple equal stripes. The advantages of such design include improved control in process variability and short-channel effects. These advantages have been modeled by simulations and demonstrated experimentally by fabricated devices. Furthermore, the segmented transistor design for improving SRAM performance and yield has been assessed via atomistic device simulations and compact analytical modeling. Initial SRAM experimental results confirm that this tri-gate bulk MOSFET technology reduces the impact of process-induced variations to facilitate supply-voltage scaling.

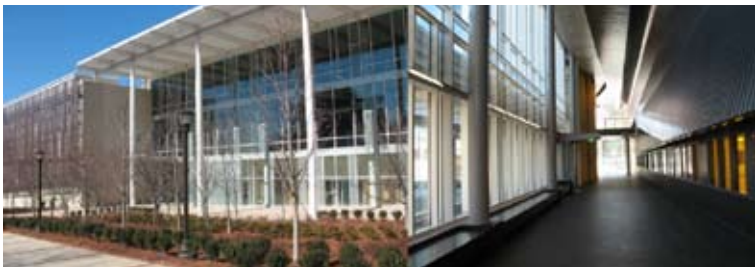


In the field of device compact modeling, the surface-potential-based models for bulk MOSFETs have become the industry standard. Researchers at Arizona State continue to extend the capabilities of these models, including features such as SOI partially depleted and dynamically depleted MOSFETs.

INTERCONNECT & PACKAGING

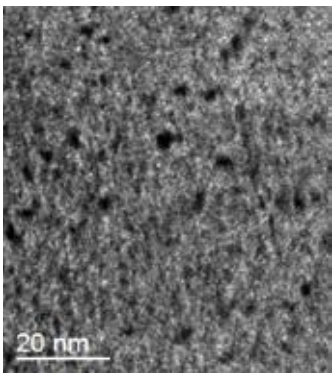
In response to the industry's focus on greater integrated functionality in smaller form factors, GRC launched a new Interconnect and Packaging Center (IPC) at Georgia Tech in February of 2009, which has a 3D technology focus. Researchers from five different universities, including Georgia Tech, Harvard, Nanyang Technical University (Singapore), Iowa State and UT/Austin, work together to help solve some of the most challenging problems in implementing 3D technology. Research topics include low temperature bonding processes, thermal modeling, thru silicon via fabrication and reliability assessment, MEMs integration, interfacial delamination and system modeling.

To enable continued scaling of interconnect performance, it is essential to introduce porosity into the low k dielectric materials to further reduce their k value. The detailed structure of



The Interconnect and Packaging Center is located in the Marcus Nanotechnology Building at Georgia Institute of Technology. The Center funds $870K/year of research with $320K/year coming from the state of Georgia.

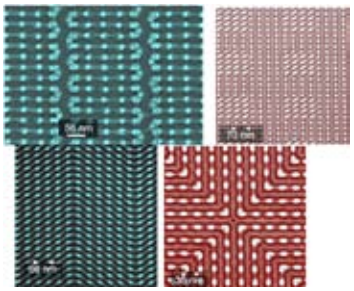
this porosity will determine the mechanical strength of the dielectrics, with uniformly distributed, small pores being the most mechanically robust distribution. While ellipsometric porosimetry, small angle x-ray scattering and positron annihilation spectroscopy can all give indirect measurements of the pore structure within porous low k materials, only electron tomography can give direct imaging of the pore structure. Researchers from Cornell have applied electron tomography to generate full 3D images of the low k pore structure. In general, the pores imaged by electron tomography have a predominantly ellipsoidal shape with relatively little multi-pore connectivity. These measurements strongly complement ellipsometric porosimetry measurements with full 3D images.



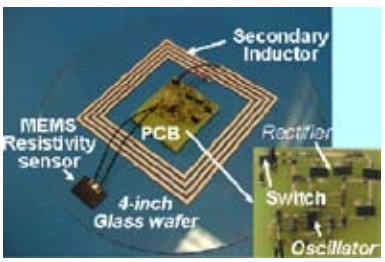
NANOMANUFACTURING

The semiconductor industry's growth rate continues to be driven by decreasing cost per function. However, it is becoming increasingly difficult to manage variability, cost, reliability, yield, sustainability and factory operations with conventional scaled subtractive processing alone. This trend implies an increasing number of potential insertion opportunities for breakthrough innovations in materials and nanofabrication technologies that address these challenges.

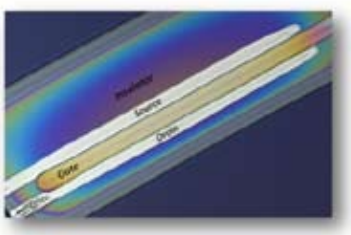
Researchers at MIT have developed a 'sparse templating' technology for self-assembling complex features, under the guidance of a minimum density of written features. They have demonstrated ring shaped and square symmetry arrays. Additionally, they have developed and validated models for designing more complex structures.



Water conservation in semiconductor facilities is becoming a major concern for integrated device manufacturers, as the costs, availability and sustainability of water resources can greatly affect manufacturing facilities. The use of water resources is getting increasingly more critical, especially as the industry moves to smaller features and approaches nano-scale manufacturing technologies. Arizona State University researchers have shown a new, exclusive way to dramatically conserve the amount of water needed to manufacture semiconductors. A unique device called an Electro-Chemical Residue Sensor allows for clean, rinse and dry process optimization that helps make semiconductor facilities more efficient, sustainable and cost-effective.



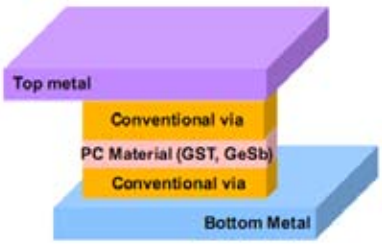
A team of researchers at UC/Berkeley has demonstrated the novel self-alignment scheme for near-micron inkjet printing technology. They report substantial achievements in use of surface flow during inkjet printing to achieve layer-to-layer registration. By exploiting liquid properties, they are able to solve a major problem with printed electronics, i.e., self-alignment. Using this approach, a minimum overlap of 0.78μm was achieved, contrasted to the >10μm typically acheived in conventional printed transistors. This enabled an order of magnitude reduction in parasitic capacitance. The process is very robust, and it has been extended to realize



fully integrated simple circuits (inverters, etc.), all formed using self-alignment. This technology should enable scalability to high-resolution inkjet heads.

NEW MODELS FOR NEW MATERIALS

Phase-change materials appear to have high potential for application in integrated circuits. This type of material switches between a crystalline and amphorphous state, each with different physical properties such as resistance. Thus, it can be used to make a programmable switch using less area than a transistor switch. Once the physics of the transformation is characterized, using the new material requires simple models that accurately describe the required properties within an electronic circuit.



Researchers at Carnegie Mellon University have developed a model for phase-change vias, coded in a standard language of Verilog-A, which includes electrical, temperature, crystallization and conductivity effects. They have done so to model the change of a chalcogenide made with germanium and antimony (GeSb) that has high impedance in the amorphous state and low impedance in the crystalline state. Furthermore, the material is compatible with current semiconductor processing flows. The model helps circuit designers determine the optimal way to take advantage of the new material and begin constructing basic circuit building blocks.

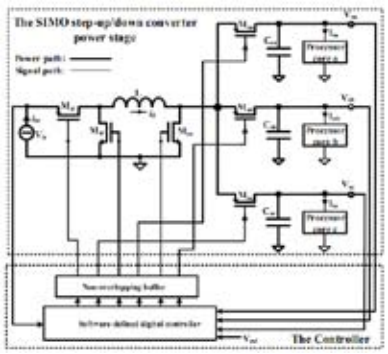
"The SRC model brings together the best minds for our industry to improve our competitiveness. And the people that come out of their programs are highly educated, highly trained, very, very relevant to our industry—and they can hit the ground running from Day One."

JOHN E. KELLY III | Senior Vice President & Director of Research | IBM

DC/DC VOLTAGE CONVERSION

As the world of digital integrated circuits gets more complex with the introduction of multi-core chip architectures, the world of analog circuit design also becomes more complex. Managing the power needs of these large systems-on-chip often requires multiple power domains with each being dynamically controlled based on the local thermal profile.

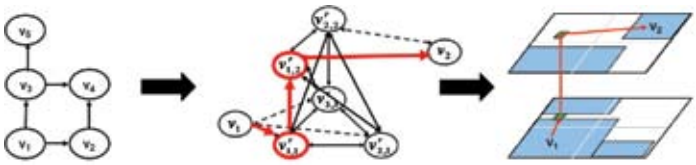
Researchers within the Texas Analog Center of Excellence (TxACE) developed a single-inductor multiple-output DC/DC voltage converter that operates between 2.0 and 3.3 volts while delivering power levels from 33 to 900mW. This type of converter provides a cost-effective approach to robust, fast-transient, on-chip power domains that are compatible with dynamic voltage scaling techniques.



MULTICORE SYSTEMS

Satisfying the continuing demand for increased performance — along with the difficulties of continued scaling, power and thermal challenges — has brought a renewed focus on systems that integrate multiple, heterogeneous processor cores on a single chip. But there are many barriers to achieving this multicore success. GRC and the National Science Foundation have begun a three-year, $10 million joint program to address these challenges, focusing on hardware and software design, tools for design, test and verification, architectures, and interconnect. It is essential to design the cores, the interconnection network and the memory system to optimize system-level performance. The tight design constraints of multicore systems are best managed through closely coordinated optimizations that bridge the gap between architecture and layout.

A floorplanner and simulation infrastructure developed by GRC researchers at the University of Minnesota provide the ingredients needed to perform layout-aware multicore design. Their work combines floorplanning and interconnect synthesis, optimizing the network topology for a particular application and workload. This implementation handles 3D and 2D technologies, and has shown a 35% reduction in power dissipation, 20% reduction in chip temperature, and 25% reduction in network latency over previous results.

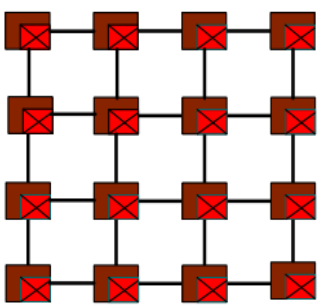


Five Cores | Routing Graph | Floorplan

MULTICORE NETWORK-ON-CHIP

As multicore chip architectures become more common and the number of processing units grows, there is an increasing requirement to move data across the chip as computation is done in multiple locations. There may also be instructions that try to use and modify the same data that may be stored in different locations, leading to data corruption issues, especially in CPU cache memories.

Researchers at Princeton are investigating techniques to trap and filter redundant requests for the same data and show how their techniques reduce the total network traffic by 25% on a 16-core chip multiprocessor system. Results for a 64-core architecture show a traffic reduction by 27%, demonstrating that the technique is scalable to larger multicore systems.



POST-SILICON VALIDATION

After a chip is fabricated, even if it has been extensively simulated and "verified" before manufacturing, it must go through "silicon bring-up" to be sure it works as intended. Unlike older practices of bringing up a board, however, integrated circuits have much more limited observability and accessibility. And while a processor chip may work in isolation—and may even be able to boot up an operating system—it may not work when integrated into a customer's system, or may fail in the field long after release. Various post-silicon validation techniques are being investigated to address this problem.

Researchers at the University of British Columbia have developed a new program, BackSpace, using formal analysis augmented with some on-chip hardware to support post-silicon debugging. They have demonstrated this on an OpenRISC 1200 processor implemented with FPGAs and show that it can run software at full speed, stop the chip at arbitrary states, and back up for hundreds of cycles from a crash or observed bug, computing a trace of exactly what led up to the problem.

FUNDAMENTAL LIMITS

GRC also evaluated some of the fundamental questions behind the technology limits by setting specific challenges to drive the discussions with the semiconductor community. One major topic for 2009 was on the limits of memory technology. What will semiconductor memory look like in 2020? What can be done to provide memory technologies that offer one to two orders of magnitude improvements in performance per unit of power consumed? In 1957, Richard Feynman asked in a lecture at Caltech if it might be possible to write the entire twenty-four volumes of the Encyclopedia Britannica on the head of a pin, which he argued has the area of about 2.5 mm2. Modern semiconductor technology is within an order of magnitude of affirmatively answering Feynman's question. Looking ahead to 2020, is it reasonable to consider the possibility of storing the U.S. Library of Congress (about ten Terabytes) in a one cm3 volume while maintaining reasonable access time, retention times and durability? A metric was proposed for use in evaluating various memory technologies based on the "Least Action Principle" of classical physics. Physical systems frequently evolve so that "action"—the product of energy consumed and transition time—is minimized. For new memory technologies, minimization of time and energy per access is highly desirable, as is the physical size of the memory device. Thus the space-action metric (e.g., the product of energy, time and volume) was proposed as a uniform metric for memory technologies. Results of optimization studies of candidate memories are given in the table below.

	$N_{carriers}$	$V_{storage}$, nm^3	E_{write}, J	t_{write}, ns	Space-Action, $J \cdot ns \cdot nm^3$
DRAM	10^5	10^5	10^{-14}	1	$\sim 10^{-8}$–10^{-9}
Flash	10	10^3	10^{-16}	10^3	10^{-9}
STT-MRAM	10^5	10^3	10^{-14}	1	10^{-13}
ReRAM	100	1	10^{-17}	1	10^{-14}

The estimated minimum space-action metric for various memory technologies

Focus Center Research Program

Solving Challenges at the Integrated Circuit Level & Beyond

Established in 1998 to conduct innovative, multi-university research in semiconductor technology with an eight+ year horizon, the Focus Center Research Program (FCRP) targets the intractable challenges in semiconductor-based technology on behalf of its Sponsors, including the Department of Defense (DARPA), the microelectronics industry and, starting this year, new companies from the defense industry. FCRP research employs a hierarchy of approaches for integrated electronics, ranging from nanomaterials, novel devices and circuit techniques, to system level design methodology and new "chip" architectures. Research in such technology enablers generates crucial results for both micro- and macro-electronic systems of the future, maintains a world-leading university-based semiconductor research engine, and is aimed at providing leading edge solutions to the U.S Department of Defense, while addressing the technology needs of the semiconductor and defense systems industries.

The Focus Centers represent virtual Centers, each consisting of multiple universities that engage the leading experts at the participating institutions. Each Center is managed by a full-time university Center Director and addresses one of the major technology challenges of the International Technology Roadmap for Semiconductors (ITRS).

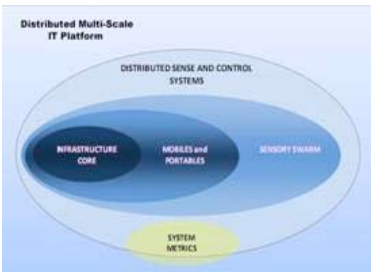
This year brought a major re-competition for all five Focus Centers and added an entirely new Center that will conduct research beyond the integrated circuit realm. Currently, this collaborative endeavor to extend the end of the CMOS transistor roadmap involves 41 universities, 201 faculty and over 382 graduate students. All FCRP research, guided by the lead university Center Directors, forges a nationwide effort to keep the United States and its technology firms at the front of the global nanoelectronics revolution.

FCRP research is creating the breakthroughs that are critical to U. S. security and economic competitiveness goals and giving participating companies a tremendous advantage in the race to lead the technological revolution. Always long-term and big-picture, FCRP research programs offer mutual leverage to industry and government Sponsors.

FCRP CENTER HIGHLIGHTS FROM THE 2009 ACADEMIC YEAR

MULTI-PLATFORM SYSTEMS RESEARCH CENTER (MUSYC)

Distributed Sense and Control System Methodology Theme



This is the overarching theme for the newly formed MuSyC Center: addressing challenges in complex distributed control systems by employing structured and formal design methodologies that seamlessly and coherently combine various dimensions of multi-scale design space, and that provide appropriate abstractions to manage inherent complexity. This theme's initial focus will involve research on an avionics case study, looking at such things as reliable and robust distributed systems architectures, distributed control algorithms, verification and modeling, and trust and security.

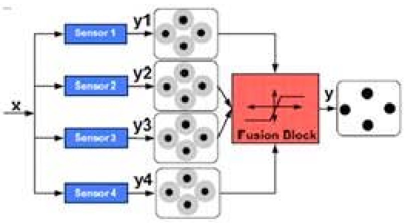
Small-Scale (human-centric) and Large-Scale Systems (data centers) Themes

In the area of Large-Scale Systems, the MuSyC Center will research distributed closed-loop power-management strategies that result in "energy-intensive" large-scale systems to be orders of magnitude more energy-efficient, while ensuring that mission-critical goals are met. This is accomplished by employing a holistic multi-scale solution including all components of the system at multiple hierarchy levels. The initial focus for this area will be on Data Center Efficiency.

The Small-Scale Systems research will be exploring the absolute bounds of energy efficiency and miniaturization in “energy-frugal” human-centric distributed IT systems through a distributed management strategy that dynamically and adaptively selects the correct operational point corresponding to the varying application needs in terms of accuracy or resolution. The initial research focus for this area will be on Human-Centric Distributed IC Systems.

GIGASCALE SYSTEMS RESEARCH CENTER (GSRC)

Alternative Computation Models for Late- and Post-Silicon Technologies Theme



Stochastic sensor NOC (Illinois)

The Alternative Theme is chartered to explore models of computation for the ultra-scaled CMOS and post-Si era, where device and circuit fabrics are expected to exhibit extreme levels of variability. Its challenge is to enable energy efficiency and robustness enhancements at trajectories traditionally promised by Moore’s law. Its research is communications-, network- and neuro-inspired. There were several notable highlights of its research this year, including Stochastic Sensor Network-on-a-Chip (SSNOC): This project (above figure) demonstrated the use of statistical techniques in the design of robust computational systems, demonstrating up to three orders-of-magnitude improvement in robustness, with 2X (energy efficiency) enhancement in the presence of high error-rates (20%-30%), for many media kernels. The practicality of these techniques was demonstrated through: 1) FPGA prototypes and 2) an SSNOC chip implementation in 180nm CMOS. Another project in this theme was Wireless Brain-Machine Interface.

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United Technologies

UNITED TECHNOLOGIES CORPORATION (UTC), based in Hartford, Connecticut, is a diversified company providing high technology products and services to the global aerospace and building industries. Its products include Carrier heating and air conditioning, Hamilton Sundstrand aerospace systems and industrial products, Otis elevators and escalators, Pratt & Whitney aircraft engines, Sikorsky helicopters, UTC Fire & Security systems and UTC Power fuel cells.

With more than 4000 locations in approximately 71 countries, UTC currently employs 206,700 individuals globally (2009). Recently, the organization was named the Number One “Most Admired” aerospace and defense company (*Fortune*, March 2009), as well as listed among Corporate Knights, Inc. “Global 100”—the most sustainable corporations in the world (2005-2009 lists).

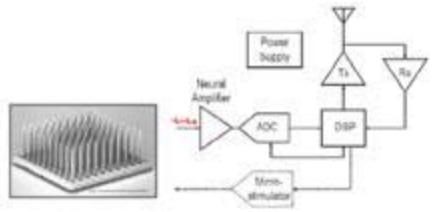
Please visit www.utc.com for more information about United Technologies.

XILINX, INC. is the world's leading provider of programmable platforms, with $1.7B in revenues in 2009 and more than 50% market share in the programmable logic device (PLD) segment of the semiconductor industry. Xilinx programmable chips are the innovation platform of choice for today's leading companies for the design of tens of thousands of products that improve the quality of our everyday lives.

With inherent flexibility, Xilinx award-winning programmable solutions—silicon, software, IP, evaluation kits and reference designs—are used to deliver innovative new products to market in a matter of weeks, drastically reduce research and development costs, and change or upgrade end product features and functions "on the fly" to meet new market demands and adapt to changing industry standards.

Founded in 1984, Xilinx today employs about 3000 people worldwide, serves 20,000 global customers and holds over 2000 patents.

Please visit www.xilinx.com for more information about Xilinx.

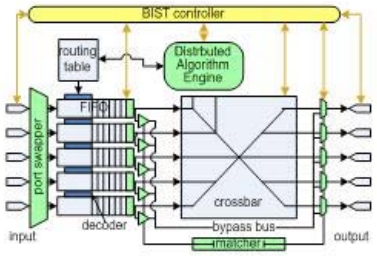


Wireless Brain-Machine Interface (UCB)

This research task experimentally demonstrated reliable recording of neural signals in rats.

Resilient System Design Theme

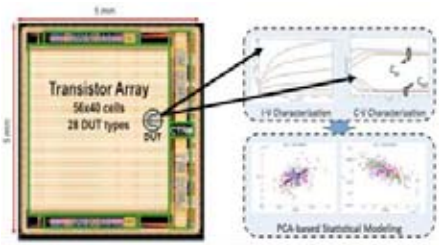
In the VICIS project at University of Michigan, the VICIS reliable chip-multiprocessor routers implement continuous monitoring capabilities that allow soft and hard faults to be detected and recovered. Additional supporting results came from the UC/Santa Barbara team, where they demonstrated that frugal sparing of interconnect wires and simple cores can provide a chip-multiprocessor with significant improvements in yield and lifetime.



CENTER FOR CIRCUITS & SYSTEMS RESEARCH (C2S2)

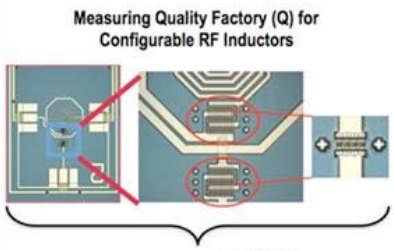
Silicon Infrastructure Theme

In the area of measurement and test, the team developed and taped out new parameter extraction circuits, which are intended to automatically extract deeply scaled parameters and statistical correlation data. For example, a new design in 45 nm CMOS process was taped out in the fall of 2009. This measurement circuit supports sub-fF capacitance resolution extraction of I-V and C-V curves and correlation-aware statistical modeling of critical device parameters, e.g., for industry-standard BSIM models.



Emerging Circuits Theme

Phase Change (PC) materials are being actively investigated as the basis for a variety of new memory applications. These materials change from high-resistance ("off") to low-resistance



("on") states via electrical configuration, allowing them to serve as reversible nanoscale switches. Although most current research is exploring digital applications, work in C2S2 in 2009 demonstrated how these materials may be used for reconfigurable RF circuits. The team builds essential passive components, such as inductors with "extra" features, and uses PC-based vias to configurably add/exclude these extra features. Recent experiments have already suggested necessary changes to the material structure to make the concept practical for RF circuits.

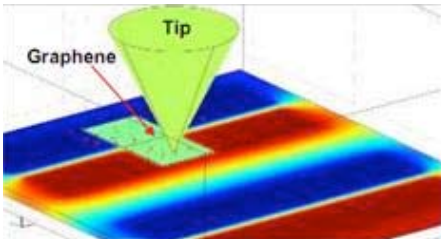
INTERCONNECT FOCUS CENTER (IFC)

Electrical Interconnects Theme

Researchers in this theme made significant advances throughout 2009 in characterization and component testing techniques. They focused on developing a unique set of tools to evaluate the quantitative structural and electrical transport properties of quantum molecular interconnects, and have demonstrated the measurement of the electrostatic doping profile in a graphene p-n junction. Finite element modeling (FEM) has been developed to simulate the electromagnetic force expected for a Kelvin probe force microscopy (KPFM) tip. The tip, graphene, and charged gates are shown (above right). Data shows that the tip should experience a measurable KPFM force due to a single graphene monolayer on the split gate test structure.

Optical Interconnects Theme

Researchers in this theme are exploiting nanophotonics and silicon-compatible materials (e.g., Ge) to make very high performance active devices (e.g., emitters, modulators) integrable with silicon. Using this technology, they have fabricated the first photonic crystal modulator.



Silicon photonic structures designed and fabricated for on-chip routing demonstrated ring-based switches that could be tuned by more than one free-spectral range, thus allowing arbitrary tuning of such switches to any wavelength in devices with 38.5 GHz of bandwidth and with greater than 17 dB of extinction. A complete on-chip optical link using a silicon ring electro-optic modulator, a silicon waveguide, and a germanium detector, was shown to operate at 3 Gb/s with only a 0.5 V swing driving the modulator.

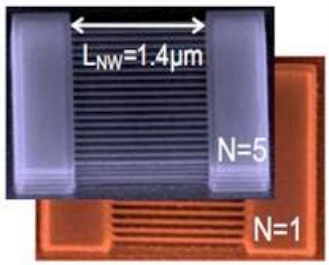
First photonic crystal modulator

Waveguide resonator structures for very low active volume–low energy ~ (1 fJ/bit) optical modulators were designed and fabricated. A compact modulator, based on a photonic crystal nanocavity whose resonance is electrically controlled through an integrated vertical p-i-n junction, was demonstrated and may ultimately allow optical modulators with extremely small volumes and capacitances.

MATERIALS, STRUCTURES AND DEVICES RESEARCH CENTER (MSD)

CMOS Extension: Si-Ge Channel Materials and Devices Theme

The ability to stack multiple levels of tensile strained-Si nanowires has been demonstrated for the first time. Recent measurements show that the strain in such structures is maintained for five levels of stacked nanowires (below). Strained-Si nanowire gate-all-around n-MOSFETs are of interest due to their potential for scalability to short channel lengths and the performance enhancement associated with the uniaxial tensile strain. Stacking strained-Si nanowires offers the potential to increase the current drive in a given chip area.



CMOS Extension: III-V Channel Materials & Devices Theme

On the device front, MIT researchers fabricated deep-submicron Al_2O_3/InGaAs MOSFETs with excellent characteristics (160 nm gate length devices have shown a maximum current of 400 μA/μm, S=141 mV/dec, DIBL=116 mV/V and I_{on}-I_{off} ratio in excess of 10^3). For shorter gate lengths, the short-channel figures of merit degrade very quickly, presumably due to the relatively deep source and drain implanted junctions.

MIT researchers also demonstrated 30-nm enhancement-mode InAlAs/InGaAs HEMTs by Pt gate sinking. These devices show a maximum transconductance of 1.8 mS/μm, S=73 mV/dec and DIBL=85 mV/V. The devices also exhibit f_t=601 GHz and f_{max}=609 GHz at V_{DD}=0.5 V. This is the first transistor of any kind on any material system that exhibits both f_t and f_{max} in excess of 600 GHz.

Separately, researchers at MIT have produced the first functioning p-type AlGaAs/InGaAs FET. This is a high-mobility modulation-doping design. With a gate length of 2 μm and at 2 V, this device exhibits a modest performance given by a drain current of 18 mA/mm and a transconductance of 16 mS/mm. Nevertheless, this device allows the study of the role of uniaxial stress on hole transport, which is the main goal of this project.

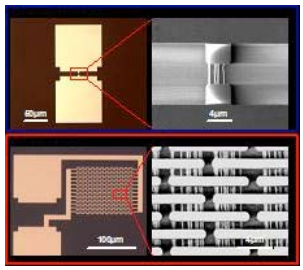
CMOS Extension/CMOS Plus: Nanowires and Nanotubes Theme

Researchers at Stanford made several breakthroughs this year in both CNT and graphene nano-ribbon (GNR) device research. Chemical enrichment of CNTs to a single chirality was achieved with high selectivity (99%). CNT FETs fabricated using this material with ~15 tubes in parallel showed an on/off ratio over 10^6. This group also demonstrated a novel method for fabricating GNRs by "unzipping" CNTs. In this case, the nanotubes were embedded in PMMA with only a narrow strip of each tube exposed. A gentle exposure to argon plasma was used to open these tubes and thereby convert them to GNRs. Ribbons with widths as small as 6 nm have been demonstrated so far. Researchers also developed a method for p-doping of GNRs by bonding N atoms to the ribbon edges using a novel reaction of Joule-heated GNRs in ammonia.

FUNCTIONAL ENGINEERED NANO ARCHITECTURES CENTER (FENA)

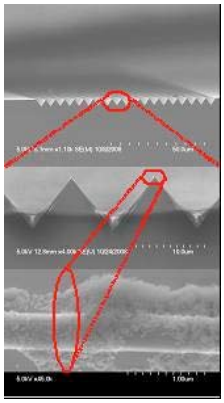
Novel Integrated Devices Theme

FENA researchers achieved breakthroughs in the area of Carbon Nanotube Electronics, with particular emphasis on CNT doping, contact engineering, and understanding CNT variability and designing around this challenge. They have devised a methodology for overcoming the metallic CNT design problem. While other groups are trying to solve the problem by removing metallic CNTs, the FENA researchers took a completely new perspective/approach. They created CNFET designs that are tolerant to metallic CNTs. That is, instead of removing or breaking metallic CNTs, the CNFET was designed to withstand them. Hence the researchers were able to achieve near-100% yield in creating devices that have high on-off ratios, despite the presence of a small number of metallic CNTs. In addition, this process is completely VLSI compatible and uses only standard optical photolithography.



Nanoscale Architectures and Information Processing Paradigms Theme

An important 2009 FENA effort was to explore fault-tolerant circuits and suitable architectures for general-purpose microprocessors on FET-based nanowire fabrics. Researchers made progress in nanowire placement, patterning and devices. Notable accomplishments in this area included achieving self-assembly of SiO_2 nanoparticles onto the ridges of a crystallographically etched Si line array, and demonstrating nanowire selective self-assembly by controlling the surface chemistry of the Si nanowires and Si ridges. The team was also able to engineer a 2nm nanogap that created a heterojunction. In addition, they fabricated a 3D nanoscale crossbar circuit using nanotransfer printing. This process paves the way toward fabricating 3D circuits with ultra-high device density and neuromorphic architectures.



Nanoelectronics Research Initiative

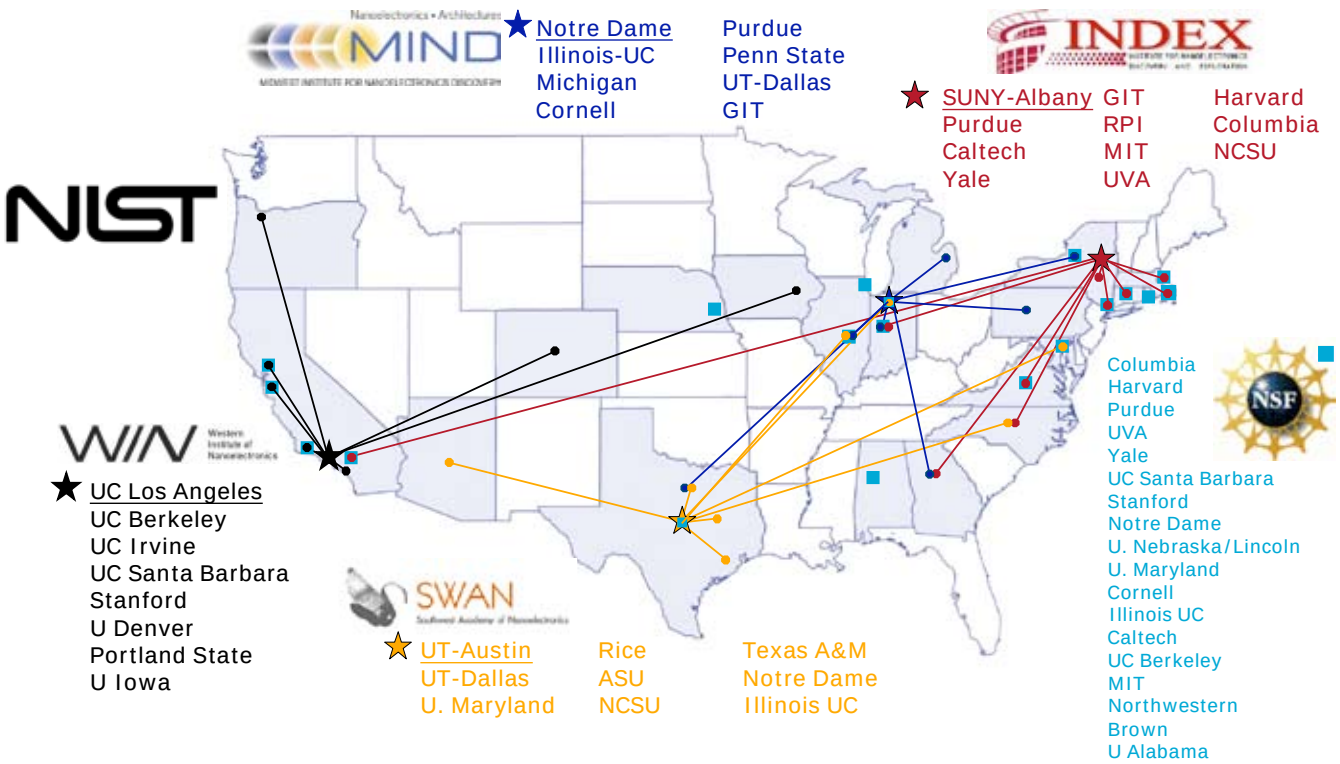
Discovering Beyond the Known

The Nanoelectronics Research Initiative (NRI) is a consortium of companies in the Semiconductor Industry Association seeking to find a device that can scale semiconductor technology beyond the ultimate limits of current CMOS transistors. This university-based research, cooperatively funded by industry and federal and state governments, is looking toward nanoelectronics in the year 2020—further out than anyone else. With a goal of discovering the next switch—a new mechanism for computing that goes beyond simply improving today's transistor, NRI engages the most talented students to become the innovators and leaders of tomorrow's technology industry.

Groundbreaking NRI research is currently being conducted at over 30 universities. The projects are organized into multi-university centers (WIN, INDEX, SWAN and MIND), which are jointly funded with the National Institute of Standards and Technology (NIST), and at National Science Foundation (NSF) nanoscience centers (NSF-NRI joint projects). And given the exploratory nature of the research, which seeks out entirely new device and computation technologies, it is particularly important that industry and academia work together closely to rapidly identify and develop emerging research paths that show potential to extend the historical cost and performance trends for information technology.

NRI Research Highlights

One of the primary challenges for NRI is to foster strong connections between the physicists and chemists doing the basic science work—often in emerging fields where new discoveries come at a rapid pace—and the engineering researchers who



ADVANCED MICRO DEVICES, INC. (AMD) is an innovative technology company dedicated to collaborating with customers and technology partners to ignite the next generation of computing and graphics solutions at work, home and play.

Formed by Jerry Sanders and seven co-founders in 1969, AMD takes great pride in igniting next-generation technology solutions. The company has a unique ability to see where customer and end-user needs are headed next, and then collaborate with the industry accordingly. As it has been for over four decades, AMD is committed to innovation that's truly useful for customers—putting the real needs of people ahead of technical one-upmanship.

Headquartered in Sunnyvale, California, AMD employs 14,700 worldwide (as of 12/27/2008) and operates manufacturing facilities in Germany, Malaysia, People's Republic of China, Singapore and the United States, with sales offices in major cities around the globe. Deriving approximately 88 percent of its revenue from international markets in 2008, AMD is truly a company of the world.

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must utilize how these phenomena could enable a new device. This year saw a huge increase in this kind of collaboration, with each of the NRI Centers starting to coalesce their work around a few key science areas and corresponding device concepts—exactly the kind of goal-oriented, basic-science research program we wanted to create. Moreover, the individual researchers working on the NRI-NSF projects have also started to interact directly with the NRI Centers, linking their individual projects to support the larger efforts there. Finally, our partnership with NIST continues to grow beyond just the funding that NIST provides. The end of 2009 saw over a dozen NRI-related projects being performed at the NIST labs in direct collaboration with NRI university researchers, taking advantage of the unique tools and capabilities of those facilities. There is even a specific NRI post-doc now at NIST, working on tunneling devices with the MIND Center at Notre Dame.

To encourage even more interaction between the NRI universities and NIST researchers, the fourth NRI Annual Review was held in Gaithersburg, Maryland, near the NIST labs. Many NIST personnel, as well as numerous invited visitors from other federal agencies in the DC-area, attended. As NRI expands, it is hoped that the formation of this informal NRI "Observer's Committee" will help foster new partnerships with other agencies in the future.

At the Annual Review it was also noted that all of the projects are focusing on ways to address the key problem: finding a new device that can operate at room temperature but at much lower power than existing technology. While many exciting breakthroughs were produced by these collaborations in 2009, two areas serve as good examples of the kind of results that are emerging.

Spintronics has been a central research topic since the beginning of NRI, due to the potential power savings from manipulating and moving spin instead of charge. The challenge has

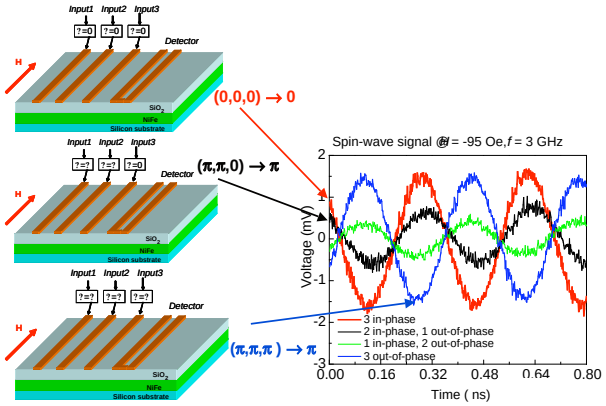

Fig. 01 **Spin Wave Majority Gate**
(WIN – A. Khitun, UCLA)

been to realize a spin device at room temperature and find a way to de-couple the charge and spin behavior. The WIN Center demonstrated the first room-temperature device this year that uses "spin waves" — the movement of the spin state of the electron without the movement of the electrons themselves — to perform a majority logic function (Fig. 01). Another approach is to utilize a collection of spins in a nanomagnetic structure to represent information, and the MIND Center demonstrated several important NanoMagnetic Logic (NML) circuit elements this year (Fig. 02), including a method of clocking the circuits — a key challenge for the technology. While all of the demonstrations so far continue to require higher power than desired, a recent proposal from one of the NRI-NSF joint projects at the Network for Computational Nanotechnology

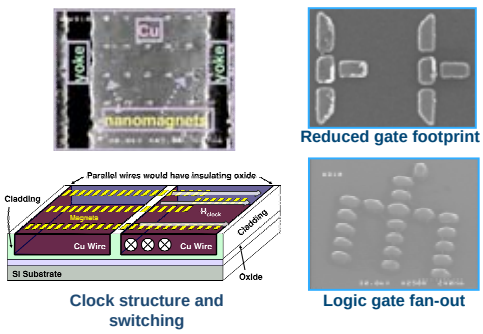

Fig. 02 **NanoMagnetic Logic**
(MIND — Niemier, Bernstein, Hu & Porod, Notre Dame)

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MASAYUKI TOMOYASU | Senior Vice President at TEL Technology Center, America | Tokyo Electron

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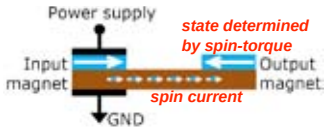
(NCN) showed an all-spin logic concept that combines spin diffusion currents with magnetic inputs and outputs (Fig. 03). Simulations indicate this could be a very low-energy switch, and experimental work is on-going to demonstrate the concept.



Estimated performance parameters (_E~40kT)			
Inverter (FO4)	Energy	Area	Delay
ASL	_E ~ 0.0002 fJ	0.008um^2	3 ps
CMOS^{15nm}	N _E ~ 0.08 fJ	0.03 um^2	4 ps
32 bit adder	Energy	Area	Delay
ASL	_E ~0.4 fJ	0.5 um^2	500 ps
CMOS^{15nm}	N _E ~13 fJ	24um^2	200 ps

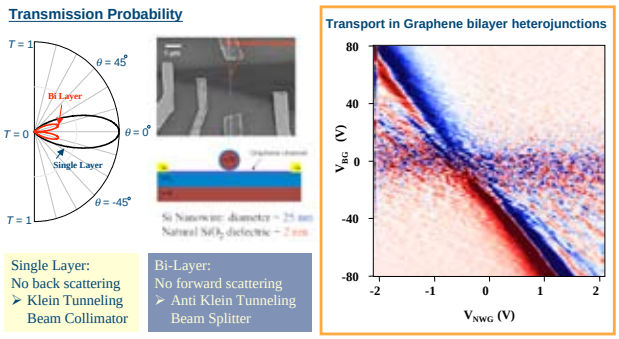
Fig. 03 **All-Spin Logic Device**
(NSF–NCN–B. Behin-Aein, D. Datta, S.Salahuddin & S. Datta, Perdue)

Graphene, a material consisting of a single monolayer of carbon atoms, is a hot area of research right now across SRC programs and at our Member companies. NRI focuses specifically on exploiting the emerging novel transport physics of the material with the goal of finding a low energy switch. The INDEX Center demonstrated how combining monolayer and bilayer graphene could create heterostructures for guiding current flow like a beam of light—enabling one to build beam collimators or splitters, for example (Fig. 04). This technology is the building block of the Veselago lens devices, as well as the programmable interconnect structures that INDEX is investigating. A major hurdle for these structures continues to be the relatively poor quality of the graphene itself, since the

"SRC is an integral part of our company's longer range research program, providing a wealth of innovative ideas from the brightest minds at top universities. Key elements of our leading-edge technologies are enhanced based on learning obtained through our SRC research interactions and student hires."

GREGG BARTLETT | Senior Vice President, Technology and R&D | GLOBALFOUNDRIES

Fig. 04 **Graphene Bilayer Heterojunction Devices–Beam Splitter** (INDEX – P.Kim, Columbia)



fabrication of the material is still in its infancy. The work of the NRI-NSF project at the University of Maryland studying the effect of disorder on transport (Fig. 05) is particularly crucial, as it helps experimentalists deconvolve the true physics from artifacts in their measurements. And progress continues to be made in making higher quality graphene structures, such as the graphene bilayer sandwiching a thin dielectric produced by SWAN. While the structure has not yet shown an excitonic condensate — the ultimate goal — it did exhibit clear Coulumb

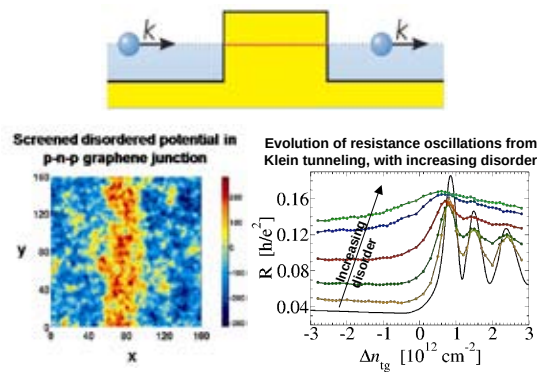


Fig. 05 **Transport in Dis-ordered Grapher** (NSF – CMTC – DasSarma, Hwang, Rossi, U. of Maryland)

drag effects at room temperature (Fig. 06). This structure is at the heart of the proposed Bilayer pseudoSpintronic FET (BiSFET), which SWAN has shown through simulation could achieve ultra low-energy performance, close to the limit of what is possible at room temperature.

Western Institute of Nanoelectronics, UCLA (Kang Wang, Director): Focuses solely on spintronics and related phenomena for logic applications, including materials, device structures and interconnects. In addition to its NRI funding, this Center receives additional direct support from Intel and the UC Discovery program.

Institute for Nanoelectronics Discovery and Exploration, SUNY/Albany (Alain Kaloyeros, Director): Focuses on a broad range of phenomena for logic devices, organized in centers of competency around excitronic, quantum-dot spin, magnetic, and graphene devices, with emphasis on fabrication and characterization. INDEX also receives additional direct support from IBM and New York State.

SouthWest Academy for Nanoelectronics, UT/Austin (Sanjay Banerjee, Director): Focuses on a large graphene program, which integrates projects on theory, material fabrication, device structures and metrology, as well as work on magnetic materials, pseudospintronics, magnetic and multi-ferroic materials, and plasmonics. In combination with its NRI funding, SWAN receives support from TI and the Texas Emerging Technology Fund.

Midwest Institute for Nanoelectronics Discovery, Notre Dame (Alan Seabaugh, Director): Focuses on tunneling, nanomagnetics and non-equilibrium phenomena for energy efficient devices and architectures, as well as thermal phonon management. In addition to NRI funding, MIND receives additional support from IBM, Indiana and the City of South Bend.

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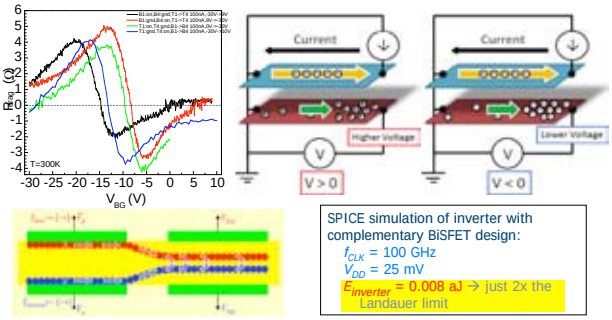
Fig. 06 **Coulomb Drag in Bilayers**
(SWAN – Tutuc, Banerjee, Register, MacDonald, et al, UT-Austin)



Benchmarking Progress: Preparing for Next Phase

One of the most exciting projects initiated in 2009 was an NRI-wide effort to benchmark all of the technologies currently being studied. Unlike the benchmarking of one CMOS technology against another, which is fairly straightforward and involves a known set of agreed upon parameters for measurement, benchmarking NRI devices is an exercise often requiring comparisons of apples to oranges. Many of the devices operate on very different physical principles and may perform computation utilizing unique architectures, so it requires looking at not just the device, but also the circuit implementation and, in some cases, even the specific application or computation algorithm being implemented. Hence, the goal is to find a quantitative set of metrics that can be used to contrast the devices and architectures on a relatively even playing field. The objective is not to judge a device as "good" or "bad," but rather to stimulate continued innovation by the NRI researchers, highlighting both the favorable attributes and the technical challenges. And more importantly, it will help define the areas on which to focus efforts in the next phase of NRI as the search for a new switch is narrowed. This benchmarking work will be a primary focus in 2010; hopefully it will not only lead to a clear roadmap for the NRI program itself, but will also encourage more researchers to consider the "grand challenge" of finding a new device to extend beyond the limits of CMOS.

"The greatest benefit of SRC Membership is the broad exposure and collaborative involvement with the technology research that is challenging our customers."

HANS STORK | Chief Technology Officer & Group Vice President, Silicon Systems Group | Applied Materials

SRC Student Programs
Producing Leaders. Making a Difference.

The mission of SRC's Student Programs is to work in a strategic partnership with SRC Members, Sponsors, faculty and students to improve student quality, as well as facilitate the transition of relevantly educated, diverse students into careers with SRC Member companies and the research community.

Member companies benefit greatly from SRC-sponsored Student Programs, which provide valuable access to a pool of talented, experienced student researchers. Since 1982 SRC has supported over 8000 students as part of its unique collaborative research model. Of the SRC-supported students, nearly 61% of graduates have joined sponsoring organizations or university faculties, or have continued on to pursue a higher degree. These students provide a path for technology transfer and an invaluable source of relevantly educated technical talent for the industry.

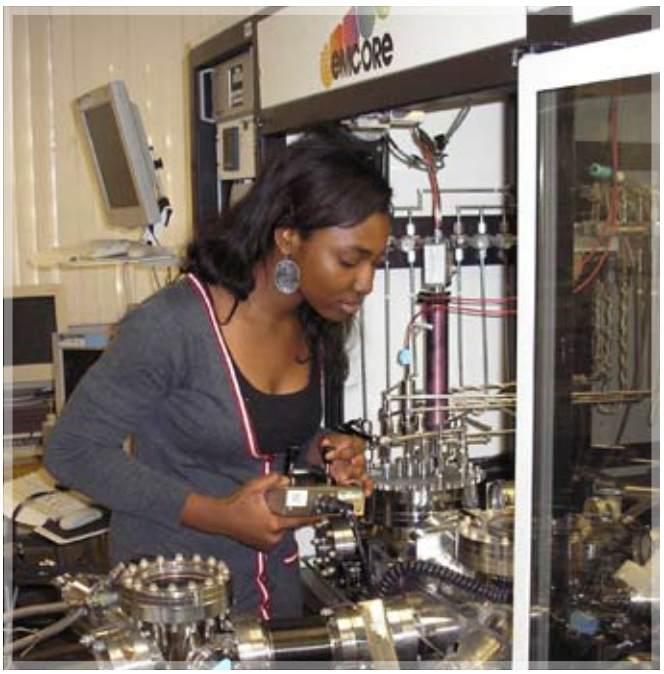
In 2009 SRC provided access to over 1500 students through the various research programs. Member company personnel can search a database of supported students on SRC's secure website to find students whose backgrounds meet their workforce needs. In addition, sponsored events around the country allow industry recruiters to meet and interact with students face to face.

Special programs are designed to meet Member needs for graduates from specific populations. During 2009, 27 GRC Graduate Fellowships, attracting academically qualified students with permanent right to work in the U.S., were co-sponsored by Advanced Micro Devices, Applied Materials, Freescale, GLOBALFOUNDRIES, IBM, Intel Foundation, NIST, Novellus and Texas Instruments; another seven fellowships were supported by GRC. In addition, the first NRI/Hans J. Coufal Fellowship was completed and a second awarded. Intel Foundation and Applied Materials co-sponsored 13 GRC Master's Scholarships targeting a diverse population.

SRC Education Alliance

Several key components of SRC's Student Programs are managed under the SRC Education Alliance. As a private foundation, the Education Alliance seeks to develop additional corporate, government and individual sources of funding, increasing SRC's ability to attract and support a wide diversity of students at various levels of education.

The Education Alliance is home to a number of programs, including fellowships at the PhD and Master degree levels, and the Simon Karecki Award, which recognizes outstanding SRC students in environmental research. The SRC Undergraduate Research Opportunities (URO) program was initiated by SRC through the Education Alliance in July 2009 as an important step in opening doors at the undergraduate level.



Vanessa Evoen is a senior Chemical Engineering major who is conducting semiconductor research with Professor Robert Hicks on the Growth and Fabrication of InGaAs/InP Heterojunction Nanostructures on Silicon under the URO program at UCLA.

TEXAS INSTRUMENTS INCORPORATED (TI) provides innovative semiconductor technologies to help its customers create the world's most advanced electronics. The company's analog, embedded processing and wireless technologies permeate daily life in many different ways, from digital communications and entertainment to medical services, automotive systems and wide-ranging applications in between.

From TI's earliest days, the objective has been to use the company's unique technical skills to fundamentally change markets and create entirely new ones. A constant thread throughout its history has been the use of progressively more complex real-time signal processing technology—with advances ranging from the incremental to the revolutionary—to literally and repeatedly change the world.

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SRC Undergraduate Research Opportunities (URO) is an innovative program made possible by a generous grant from the Intel Foundation, providing undergraduates with valuable research experience and mentoring. Participating undergraduates not only gain confidence in their ability to perform hands-on research and augment their classroom learning, but they also come to appreciate the doors that are opened to those with an advanced degree.

The objectives of the SRC URO program are to increase academic retention among undergraduates who express interest in a broad range of physical science and engineering disciplines, and encourage them to continue their education beyond a four-year degree. The SRC URO program actively engages a diverse student population, including women and under-represented minorities.

In 2009 the URO comprised programs at 14 universities, supporting meaningful hands-on research and on-campus activities and programs to help students select and apply to graduate school. In addition, the Education Alliance created a Faculty Resource Center to help connect qualified URO students with SRC-funded graduate research opportunities. URO Program Managers attended TECHCON 2009; students from each of the participating universities will be invited to present posters at TECHCON 2010.

"TI's greatest benefits from SRC memberships include GRC core projects and custom projects with flexibility to direct GRC funds in alignment with our interest areas, GSRC mid-range research Focus Centers with increased efforts on system-level issues, and NRI long-range research beyond current technology scaling — all with significant government funding leverage and graduate student preparation."

VENU MENON | Vice President | Texas Instruments

2009 STUDENT PROGRAMS HIGHLIGHTS

- 37 SRC student alumni represented their companies as members of various SRC technical advisory boards, and another 176 acted as mentors to SRC research projects.
- 95 former SRC students had active research funding with one or more SRC entity.
- Over 1500 students participated in SRC research across GRC, FCRP and NRI, with 176 completing MS or PhD degrees.
- At the beginning of the 2009 fall term, 33 GRC Graduate Fellowships, 1 NRI Fellowship and 12 SRCEA Master's Scholarships were in place.
- 132 undergraduate students from 11 universities participated in the URO program in the 2009 fall semester; another 45 students from 3 additional universities will join the program for the spring and summer of 2010.
- Student/industry networking events were held at the University of Arizona, the UT/Dallas, Carnegie Mellon University, UCLA, MIT, UC/Berkeley and Georgia Tech.
- The 2009 Simon Karecki award was presented to Nandini Venkataraman, University of Arizona, at the Center for Environmentally Benign Semiconductor Manufacturing Review.
- Phase 2 of the SRC/SIA IC Design Challenge, Performance at the Limits, was completed with winners announced at the ICCSS Conference. First place went to the team from Purdue led by Professor Byunghoo Jung.

For further information on SRC Student Programs and the Education Alliance, please go to src.org/member/students/about.asp.

Mentor Graphics®

MENTOR GRAPHICS CORPORATION (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing electronic design automation (EDA) products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. The company provides best-in-class technologies for design for manufacturing, integrated PCB-FPGA systems design and functional verification, plus the EDA industry's most comprehensive suite of electronic system-level (ESL) design tools for hardware creation. The company also offers products in areas not traditionally addressed by EDA, such as embedded software, electrical system and harness engineering, and thermal analysis and electronics cooling.

Established in 1981, and with over 70 offices worldwide, Mentor Graphics reported revenues over the last 12 months of about $800 million and employs approximately 4425 people worldwide. Corporate headquarters are in Wilsonville, Oregon.

Please visit www.mentor.com for more information about Mentor Graphics.

"SRC benefits us at the level of both the new hire and the experienced senior engineer. SRC education funding has created an outstanding employment pool of work-ready new engineers with excellent training, able to hit the ground running. SRC e-seminars keep our experienced engineers constantly aware of relevant leading-edge research."

WALDEN C. RHINES | Chairman & CEO | Mentor Graphics

TECHCON 2009
Technology & Talent for the 21st Century

TECHCON 2009, SRC's annual technical conference, followed the long-standing tradition of excellent research presentations and networking among industry, students and faculty. This event showcases the quality of the SRC research portfolio, the excellence of SRC students and faculty, and the magnitude of the collaborative research investment made by the semiconductor industry through SRC. TECHCON 2009, hosted at the Renaissance Hotel in Austin, Texas, on September 14 and 15, marked the eleventh anniversary of TECHCON and proved to be one of the most successful events to date. Sessions reflected all SRC entities, with 144 student-presented technical papers and posters representing a broad cross-section of SRC-funded research. Seventeen students won Best-in-Session awards, with industry judging based on technical content, perceived value, technology/information transfer and presentation. Twenty-nine SRC student alumni are current faculty advisors to 37 student presenters; four of those presenters are third generation.

Total attendance reached 377, including 136 industry participants, 37 faculty, 172 students and 32 others (staff, etc.), making for outstanding networking and technical exchange. Among the attendees were 40 alumni of SRC student programs who are now maintaining connection with SRC for their current organizations.

Invited speakers from industry and academia provided a glimpse of a very exciting future for the semiconductor industry. Dr. Walden Rhines, Mentor Graphics President and CEO, delivered the keynote address entitled "Less of Moore." Professor Paul Rothemund, FCRP researcher from the University of Southern California, and Professor Frank Register, GRC and NRI researcher at UT/Austin, were the speakers at the New Frontiers Session on Monday afternoon, providing a look at the exciting possibilities for new graphene-based devices and the DNA-inspired methods for integrated circuit assembly.

Seventeen students won Best in Session Awards at TECHCON 2009.

Larry Sumney *(3rd from L)* presented the 2009 Aristotle Award to Professor Chenming Hu *(4th from L)*, accompanied by Mrs. Hu, at TECHCON 2009. Professor Hu's nomination was supported by former students Professor Dennis Sylvester *(second from R)*, University of Michigan, and Professor Michael Orshansky *(R)*, UT/Austin. Also pictured: Darsen Lu *(L)*, and Dr. Clement Wann *(2nd from L)*, TSMC.

TECHCON also provides a forum for recognizing excellence in the SRC research community. Inventor Recognition Awards recognize those university researchers whose creativity and innovations lead to patentable inventions, thereby increasing the competitiveness of SRC Member companies. This year 31 innovative research faculty and students were recognized for this prestigious award during TECHCON 2009.

The Aristotle Award recognizes excellence in teaching through the research process, as well as an exceptional commitment to students. This year's recipient, Professor Chenming Hu, has been an integral part of SRC-sponsored research at the UC/Berkeley since 1989 and has been faculty advisor to a host of PhD graduates, many of whom continue their support for SRC research programs.

2009 MAHBOOB KHAN OUTSTANDING LIAISON AWARD WINNERS

The GRC Industry Liaison Program is a powerful partnership that brings together university researchers, graduate students and semiconductor industry experts. The program allows Member companies to effectively extract value from GRC, and it gives students an increased breadth of academic experience through real-world industry research. As an integral part of the research team, Liaisons are actively involved in task planning and guidance throughout the process, and the long-term relationships formed in the program impact and enrich the lives of both mentor and student.

The Mahboob Khan Outstanding Liaison Award, named in memory of a longtime program advocate from AMD, is presented to those individuals who have made significant contributions in their roles as Industry Liaisons. These recipients represent "ideal mentors" whose commitment meaningfully enhances the GRC research program.

Christian A. Witt, GLOBALFOUNDRIES, Celia Merzbacher, SRC and Shih-Lien Lu, Intel. *Not pictured:* Sanu Mathew, Intel, Wilman Tsai, Intel, and Matthew Miller, Freescale

NOVELLUS

Founded in 1984, **NOVELLUS SYSTEMS, INC.** is a leading supplier of chemical vapor deposition (CVD), physical vapor deposition (PVD), electrochemical deposition (ECD), ultraviolet thermal processing (UVTP), and surface preparation equipment used in the manufacturing of semiconductors. The company's legacy PECVD, HDP CVD, W-CVD, PVD, and ECD products are used to deposit extremely thin films of insulating and conductive materials that are used to create the wiring on a chip.

Other Novellus products are used to clean the surface of the chip in-between manufacturing steps or to post-treat deposited films in order to improve mechanical properties. As circuit geometries decrease in size, the deposition, surface preparation and film treatment systems manufactured by Novellus become increasingly critical technologies for manufacturing advanced semiconductor devices.

An S&P 500 company, Novellus is headquartered in San Jose, California with subsidiary offices across the globe.

Please visit www.novellus.com for more information about Novellus.

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"Novellus has been a member of the SRC since 1995. Access to trained students, networking opportunities and relevant consortial research, are historically the values received. Today with the technical problems confronting the industry the impact of the GRC and FCRP research programs is taking on an increasing significance."

JOHN KELLY | Senior Director, External R&D | Novellus

UNIVERSITIES SUPPORTED IN 2009

Arizona State University
Auburn University
Binghamton University/SUNY
Boston College
Boston University
Brigham Young University
Brooklyn College, City Univ. of NY
Brown University
California Institute of Technology
Carnegie Mellon University
Case Western Reserve University
City College of New York
Clarkson University
Colorado School of Mines
Colorado State University
Columbia University
Cornell University
Dartmouth College
Delft University of Technology
Drexel University
Duke University
Emory & Henry College
Georgia Institute of Technology
Harvard University
Hiroshima University
Howard University
Illinois Institute of Technology
Indian Institute of Science
Indian Institute of Technology/Bombay
Indian Institute of Technology/Delhi
Indian Institute of Technology/Guwahati
Indian Institute of Technology/Kharagpur
Iowa State University
Johns Hopkins University
Lehigh University
Louisiana State University
Macalester College
Massachusetts Institute of Technology
McGill University
Michigan State University
Nanyang Technological University
National University of Singapore
New Jersey Institute of Technology
New York University
North Carolina A&T State University
North Carolina State University
Northeastern University
Northwestern University
Oklahoma State University
Oregon State University
Pennsylvania State University
Politecnico di Torino
Portland State University
Poznan University of Technology
Princeton University
Purdue University
Rensselaer Polytechnic Institute
Rice University
Rochester Institute of Technology
Royal Institute of Technology (KTH)
Rutgers University
San Jose State University
Southern Illinois University
Southern Methodist University
Stanford University
Stony Brook University/SUNY
Swiss Federal Inst. of Technology
Technion-Israel Inst. of Technology
Tel Aviv University
Temple University
Texas A&M University
Texas Tech University
The Ohio State University
Tufts University
Univ. at Albany/SUNY
Univ. at Buffalo/SUNY
Univ. of Alabama
Univ. of Arizona
Univ. of Arkansas/Fayetteville
Univ. of Bayreuth
Univ. of Bologna
Univ. of British Columbia
Univ. of California/Berkeley
Univ. of California/Davis
Univ. of California/Irvine
Univ. of California/Los Angeles
Univ. of California/Riverside
Univ. of California/San Diego
Univ. of California/Santa Barbara
Univ. of California/Santa Cruz
Univ. of Central Florida
Univ. of Colorado/Boulder
Univ. of Connecticut
Univ. of Delaware
Univ. of Denver
Univ. of Florida
Univ. of Glasgow
Univ. of Houston
Univ. of Illinois/Urbana-Champaign
Univ. of Iowa
Univ. of Kentucky
Univ. of Louisiana/Lafayette
Univ. of Louisville
Univ. of Maryland
Univ. of Massachusetts
Univ. of Michigan
Univ. of Minnesota
Univ. of Nebraska/Lincoln
Univ. of Nebraska/Omaha
Univ. of North Carolina/Chapel Hill
Univ. of North Carolina/Charlotte
Univ. of North Texas
Univ. of Notre Dame
Univ. of Oklahoma
Univ. of Pennsylvania
Univ. of Pittsburgh
Univ. of Rochester
Univ. of South Florida
Univ. of Southern California
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Univ. of Texas/Arlington
Univ. of Texas/Austin
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Univ. of Toronto
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Univ. of Utah
Univ. of Virginia
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Univ. of Wisconsin/Madison
Vanderbilt University
Virginia Tech
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Washington State University
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Topical Research Collaboration

Applying Collaborative Research to New Horizons

A Topical Research Collaboration (TRC) is an SRC initiative to create synergistic opportunities between the semiconductor industry and other sectors. These newest areas of investigation form an integral component of SRC's long-term strategy to address ***innovative applications research***—research in the adjacent spaces for both SRC members and non-members. While they apply the same revolutionary pre-competitive collaborative research methodologies that made SRC pioneers in the semiconductor industry, and so are expected to garner *big-time results*, TRC programs involve relatively *short-term commitments* from industry and academia.

BIOELECTRONICS: *Discovery and Innovation*

The overarching purpose of SRC's Bioelectronics TRC is to advance science and technology at the intersection of biology and semiconductor electronics in support of applications ranging from medicine and healthcare to environmental monitoring and food safety. Potential high impact and wide-reaching opportunities in bioelectronics are emerging as the understanding of disease and biological processes grows and as electronic technologies continue to become smaller and more functional. But there are fundamental challenges to be overcome including power supply, data management and communication, and controlling interactions between engineered and biological materials.

The SRC Bioelectronics TRC aims to strategically invest in basic, pre-competitive university research on behalf of Sponsors comprising of Member companies from the biomedical and semiconductor industries that have interest in and need for bioelectronics technologies and government agencies that support research in the area.

ENERGY: *Seeking Tomorrow's Smart Solutions*

The growing global demand for clean, affordable, secure and reliable sources of electricity for powering lives, communities and economies is the driver for SRC's energy initiative. To overcome the technological barriers to meeting this demand, SRC is applying its proven model of pre-competitive collaborative university research. The Energy Research Corporation (TERC), a subsidiary of SRC, has been formed to create and manage a university-industry partnership designed to spur basic, use-inspired research that will enable Member companies to compete in meeting the global demand for clean energy.

The initial research focus areas for TERC are photovoltaics (PV) and smart grid, and two Research Centers are being established — a Photovoltaic Research Center at Purdue University and a Smart Grid Research Center at Carnegie Mellon University — to provide a firm foundation for addressing these important topics. The Photovoltaic Research Center at Purdue will initially focus on modeling and simulation of photovoltaics to optimize cell performance and reliability, as well as to facilitate scale-up of PV manufacturing processes. The primary focus of the Smart Grid Research Center at Carnegie Mellon will be on modeling, simulation and software to control and optimize the smart grid and ensure security and reliability of the electricity network. With the establishment of these two Centers, as well as a future Center to address the related topic of energy storage, SRC is spearheading the fundamental pre-competitive energy research that will have broad benefits as the world strives to meet its future energy needs.

DOW ELECTRONIC MATERIALS, a global supplier of materials and technologies to the electronics industry, brings innovative leadership to the semiconductor, interconnect, finishing, display, photovoltaic, LED and optics markets. From advanced technology centers worldwide, teams of talented Dow research scientists and application experts work closely with customers, providing solutions, products and technical service necessary for next-generation electronics. These partnerships energize Dow's power to invent.

Dow's portfolio includes: CMP, lithography, metallization and ceramic materials for semiconductor applications; surface preparation, metallization and imaging materials for interconnect, electronic and industrial finishing, and photovoltaic applications; precursor materials for LED, solar and semiconductor manufacturing; OLED materials, display films, and display chemicals for LCD and plasma display fabrication; and zinc-based materials for optics.

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NANOENGINEERING: ***Discovering Nano-enabled Solutions. Developing Innovation Leaders.***

The nanoengineering TRC involves multi-disciplinary research projects focused on developing nano-enabled solutions to critical national challenges. SRC has partnered with Sandia National Laboratories and the Department of Energy (DOE) to offer the kind of industry-academia collaboration for which SRC is best known. The same model of success that teams university researchers, brilliant engineering and technology students, and industry greats within GRC, NRI and FCRP, is now being harnessed for the crucial area of nanoengineering.

National Institute for Nanoengineering (NINE),

SRC's first nanoengineering TRC, is hosted by Sandia in Albuquerque, NM, and focuses on technical projects that develop nano-enabled solutions to current national issues, ranging from energy alternatives to national security. And similar to every area within SRC, NINE also is a key opportunity to develop student researchers into the next generation of engineering and technology leaders for the United States. The industry Members for this program are ExxonMobil, Goodyear and Intel. SRC has formed a new entity to be the administrative manager for the program and is currently managing projects in the area of sensors, nano-patterning, directed self-assembly and nano-composite materials.

"In the past decade, the semiconductor industry has gone through tremendous changes, and SRC has consistently been at the forefront of these changes. Dow Electronic Materials has had a longstanding affiliation with SRC. This has been highly beneficial in ensuring that Dow is well informed and aligned with leading-edge industry directions, and is prepared to bring new technology solutions to our customers in a timely manner."

JEFFREY M. CALVERT | Technology Director, Advanced Packaging Technologies | Dow

SRC By The Numbers

Thanks to our valuable Members, Sponsors and university partners, SRC has made a significant impact on the industry and the academic research community over the years. And the numbers are quite impressive.

SRC RESEARCH PROGRAMS

$834M invested by SRC Members

$715M total leveraged funding

- $146M directed
- $215M collaborative
- $354M influenced

3097 contracts

8287 students

1905 faculty members

247 universities

DELIVERABLES

47,197 technical documents

353 patents granted

803 patent applications

940 inventor awards

624 software tools

2598 research tasks/themes

MICRON TECHNOLOGY, INC. is one of the world's leading providers of advanced semiconductor solutions. Through its worldwide operations, Micron manufactures and markets DRAMs, NAND flash memory, other semiconductor components, and memory modules for use in leading-edge computing, consumer, networking and mobile products.

Micron's common stock is traded on the NASDAQ under the MU symbol.

Please visit www.micron.com for more information about Micron.

"Micron benefits from the advanced research that is taking place at universities across the country as part of SRC's FCRP and NRI programs. Specifically, research related to new materials and NRI's broad effort to identify technology beyond CMOS. The funding leverage provided by these programs, along with the access to world-class faculty and students, are the reasons Micron chooses to participate."

SCOTT DEBOER | Vice President of Process Development | Micron

SRC Membership

Advanced Micro Devices, Inc. | FCRP, GRC, NRI

Applied Materials, Inc. | FCRP, GRC

Axcelis Technologies, Inc. | GRC

Cadence Design Systems | FCRP, GRC

ExxonMobil Corporation | NINE

Freescale Semiconductor, Inc. | FCRP, GRC

Goodyear | NINE

GLOBALFOUNDRIES Inc. | FCRP, GRC, NRI

IBM Corporation | FCRP, GRC, NRI

Intel Corporation | FCRP, GRC, NRI, NINE

Mentor Graphics Corporation | GRC

Micron Technology, Inc. | FCRP, NRI

Novellus Systems, Inc. | FCRP, GRC

Raytheon Company | FCRP

Rohm and Haas Electronic Materials, an affiliate of Dow Electronic Materials | GRC

Texas Instruments Inc. | FCRP, GRC, NRI

The MITRE Corporation | GRC

Tokyo Electron Limited (TEL) | GRC

United Technologies | FCRP

Xilinx, Inc. | FCRP

GOVERNMENT PARTICIPATION

DARPA | FCRP

NIST | GRC, NRI

NSF | GRC, NRI

Sandia National Labs | NINE

Oregon Nanoscience & Microtechnologies Institute | NRI

Project Future – South Bend, Indiana | NRI

SPAWAR Systems Center | FCRP

State of Arizona | GRC

State of California | NRI

State of Georgia | GRC

State of Indiana | NRI

State of New York | GRC, NRI

State of Texas | GRC, NRI

UK Engineering & Physical Sciences Research Council | GRC

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SEMI | FCRP, GRC

SIA | FCRP, GRC, NRI

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The Annual Report of Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program and provide information on activities and events of the SRC community for the precious calendar year.

A digital version of the 2009 SRC financials are available for Members online at www.src.org. A copy of this report and additional information about SRC are also accessible at www.src.org.


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