IMPACT

SRC, TOGETHER WITH ITS MEMBERS, STUDENTS AND FACULTY,
MAKES A PROFOUND **"REAL-WORLD" DIFFERENCE.**

ANNUAL REPORT **2010**

IN TODAY'S CULTURE OF HIGH-SPEED NANOTECHNOLOGY, there has evolved a certain level of public expectation…you press "send" on your mobile device, and a photo of your newborn baby is sent halfway across the world. Or you plug an address into your GPS, and your vehicle verbalizes exactly how to arrive at your destination with the least traffic. You no longer need a desk to work, as your "desktop computer" now fits into the palm of your hand.

Few people, however, consider the actual science behind the current marvels of technology (not to mention the countless innovative individuals and organizations capable of envisioning those possibilities in the first place). What matters to the masses is the ultimate impact of the technology—*the fact that, because of it, life is easier, more convenient, better.*

If people *could* look behind the proverbial curtain, they would find thousands of talented faculty and students whose SRC research not only enables existing technologies in its Member companies, but also creates the basis for even more powerful technologies through scientific and engineering discovery. Ultimately their research contributes to the magic of the electronic systems our Members produce. Together with the students, professors and Members, SRC is the structure that brings together these forward-thinking individuals and entities to collaboratively address the global challenges of this century.

MOST PEOPLE HAVE NEVER HEARD OF SRC…BUT THEY HAVE EXPERIENCED OUR **IMPACT**.

Table of Contents

A Message from the President

When talented people address challenging and well-posed problems, the possibilities for innovation multiply. At its core, this philosophy has been one of the keystones of the success of SRC for the past 28 years. By engaging the brightest minds in industry, government and the universities, SRC has been able to provide a continuing series of innovative contributions to the semiconductor technology that is empowering people worldwide. And, in partnership with universities, SRC programs have enabled the graduate education of thousands of students specializing in the semiconductor sciences and technologies – thousands of whose professional careers are continuing to expand the reach of our technology.

Within the context of the expanding horizons of semiconductor technology applications, SRC has continued in 2010 to explore new avenues of research to benefit both our Members and the industry at large. The Energy Research Initiative seeks to build on SRC community core expertise in the semiconductor technologies for energy harvesting and conditioning, and at the same time, utilize the powerful information processing technologies that the industry produces to intelligently control increasingly interconnected electrical power grids. And we continued our commitment to research Environmentally Sustainable Manufacturing. In view of the lasting impact that SRC-supported student alumni are making to semiconductor technologies and to the industry, we have redoubled our efforts to increase support for undergraduate and graduate fellowships by encouraging charitable donations to the Educational Alliance Foundation.

I wish to express my appreciation to DARPA, NSF and NIST federal agencies for their steadfast support of SRC programs over a period of decades. We have had assignees from NIST at SRC and have had a long history of working with DARPA. As an example of our partnership with government, in 1996 we jointly funded an Engineering Research Center on ESH with NSF, which continued for the 10-year lifetime of ERCs. At that point, we began to jointly fund the Center with SEMATECH and, over the years, the focus has moved to Environmentally Sustainable Manufacturing. We at SRC look forward to many more years of working together with various government agencies. Indeed, SRC stands ready to expand its strategic partnerships with government agencies in response to President Obama's call for a new innovation strategy as key to economic growth. We believe that our well established working relationships with key knowledge-based entities, i.e., industry and universities, ideally position SRC to rapidly and effectively respond to the innovation challenge. Continued discoveries in semiconductor technologies are needed, and are possible, and they will lead to incredible inventions that will improve the economy and the quality of life for all.

Sincerely,

Larry W. Sumney, *President & CEO*

about SRC

RESEARCH IN ACTION

Semiconductor Research Corporation (SRC) is the world's leading technology research consortium. With Member companies and university research programs spanning the globe, SRC plays an indispensable part in the R&D strategies of industry's most influential entities. SRC-sponsored university research is of the highest caliber and creates knowledge breakthroughs that will define the technologies of tomorrow.

MAKING A DIFFERENCE

Since 1982 Members of SRC programs have invested millions in cutting-edge semiconductor research supporting thousands of elite students and hundreds of the world's best faculty at scores of universities worldwide. The diverse programs engage and challenge the most talented students in science, engineering and technology. SRC graduates are immediately able to contribute to Member operations, and, moreover, Member companies and partners/sponsors secure access to a continuous flow of relevant research results.

SRC by the Numbers

$ 869 M	invested by SRC Members
$ 819 M	total leveraged funding
3,177	contracts
8,821	students
2,000	faculty members
257	universities

DELIVERABLES

51,376	technical documents
373	patents granted
877	patent applications
992	inventor awards
661	software tools
2,853	research tasks/themes

IMPACT: ENVIRONMENT, SAFETY & HEALTH

What comes to mind, when someone mentions environmental technology? Perhaps it's an image of a manufacturing plant that is retrofitted with cumbersome scrubbers to clean the air ejected from exhaust stacks in order to comply with environmental regulations. Or maybe it evokes a presumed added cost of doing business, which may compromise a manufacturer's process, performance and competitive edge. So can "environmental technology" truly be a positive, beneficial aspect of industry?

In 1994 when Intel broke ground on their first $1B semiconductor facility in the southwestern U.S., that facility was projected to consume enough water each year to fill a lake 2.5 miles on a side and 12 feet deep—more water than was available for the local residents. When they were denied the water use permit, SRC was asked to increase its research emphasis on water purification and to examine more closely how water cleans surfaces.

At that time SRC graduate students were developing more efficient ways to use water and special filters to remove different trace impurities from the water coming out of a semiconductor manufacturing facility. They quickly demonstrated that not only was it possible to recycle water, but it was cost effective. The water waste stream coming out of a manufacturing facility is relatively constant, in terms of the type and amount of impurities; conversely, the trace impurities in external water supplies vary seasonally and require significantly more treatment and purification before it can be used. Our members knew: *Being a good environmental steward is good for the bottom line and can enhance competitiveness.*

Based on these and related results, SRC and NSF launched a joint engineering research center for environmentally benign semiconductor manufacturing. Its mission is to develop sustainable, high-performance materials and processes that also reduce manufacturing costs. Today most of the water used in semiconductor manufacturing facilities is recycled, using filtration technologies developed under SRC support. New sensor technologies have enabled a further 40% reduction in water usage during rinses and research is underway that seeks similar breakthroughs throughout the manufacturing line, which may also benefit adjacent industries.

So is "environmental technology" a good thing? Results so far are demonstrating a resounding *yes*. SRC is creating a new vision for sustainable, low-ESH-impact, high-performance technologies at a lower cost, revolutionizing how we approach semiconductor manufacturing.

Global Research Collaboration

INDUSTRY ENGAGEMENT, VALUABLE RESULTS

Global Research Collaboration research has been focused on the current priorities of the semiconductor industry: continued scaling of semiconductor technologies and finding diverse applications for this technology. The 2010 results demonstrate the incredible research portfolio breadth, ranging from new materials and processes to allow the continued improvement in device density, to progress in techniques for making circuits and systems. Robust and reliable circuits and systems are an important emphasis, as are the broader application and environments in which the devices and systems will be required to function. The following are just a few examples of the specific impact of GRC research results that our Member companies have identified.

Much of the research results supporting the increasing density of integrated circuits are in the area of interconnect improvements. Work from the University of Michigan has for several years now been consistently delivering essential software, backed by fundamental chemistry understandings, to help our Members design next-generation processing equipment–in this case plasma tools that are designed to minimize some of the adverse affects of plasma processing. [FIG.1]

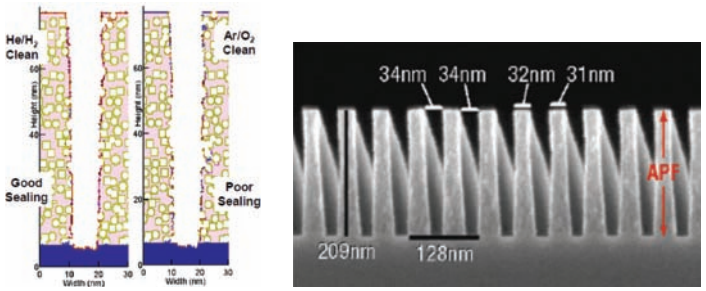


FIG.1
In-situ low-k dielectric pore sealing to minimize processing damage

A long-time research activity from the University of Texas, supported by SRC for many years, has provided unparalleled insight in to the grain structure of Cu. The research addresses an important issue for continued interconnect scaling, namely the effect of grain size on electromigration reliability. The work in this project may be the first indication that grain structure and/or orientation has an impact on electromigration reliability. **[FIGS.2A and 2B]**

The miniaturization of the MOS transistors is continuing to call for its essential elements to be smaller and more defect-free. In particular, the gate dielectric needs to be scaled correspondingly. However, besides thickness scaling, different dielectric materials other than SiO_2 have been used, which have higher dielectric constants (K) for smaller EOT (equivalent oxide thickness). In order to use this new class of dielectrics, it is important to understand electronic defects that will cause performance and reliability problems.

Researchers at the University of Utah have developed a new probing technique to monitor these defects. The technique is based on a novel scanning probe method for manipulating single electrons tunneling to and from individual traps. It provides important atomic-scale understanding of the (1) number, (2) three-dimensional spatial distribution, (3) energy and (4) chemical identity of individual electron trap states in high-K dielectrics. **[FIG.3]**

The ever-shrinking lithography processes for semiconductors have produced dramatic size, speed and cost benefits for the electronics industry. However, the industry faces certain physical and economic constraints as it moves to smaller transistor scales, or nodes. In particular, the industry has yet to find a manufacturing solution to patterning feature sizes beyond the 22 nm node. Block copolymer lithography is a new approach to complement lithography. It offers advantages such as self-healing and low-cost, as compared to double-patterning. Block copolymers are polymer chains made from two different bonded polymers, which inherently self-assemble into nano-scale uniform patterns.

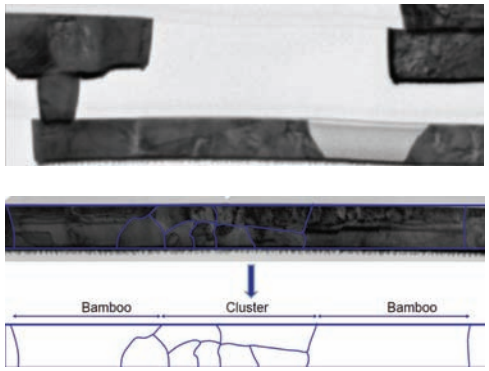


FIG.2A
Void growth during electromigration

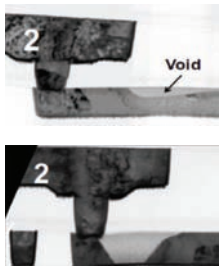


FIG.2B
Grain distribution variation in Cu

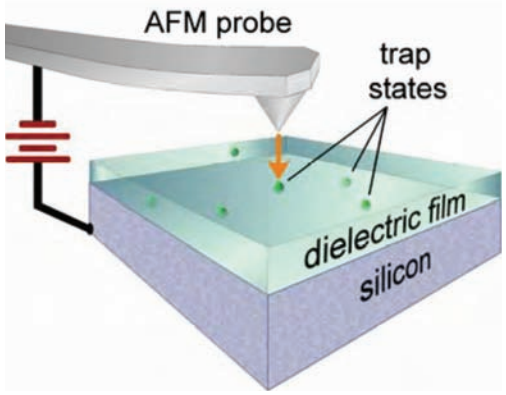


FIG.3
Single Electron Tunneling Force Measurement

Researchers at Stanford University have developed the industry's first top-gated field effect transistor (FET) and CMOS inverter featuring 20 nm contact holes using diblock copolymer lithography. This work has produced the industry's first functional devices and circuits that employ diblock copolymer patterning for sub-22 nm CMOS technologies on a full wafer scale. This development represents a significant step towards integrating self-assembly within a semiconductor manufacturing process flow. It also will help increase the use of nanotechnology for advancements in electronics for years to come. **[FIG.4]**

The circuit design challenges addressed by the Computer Aided Design (CAD) efforts are increasingly more difficult. In particular, verification–assuring that chips perform correctly–is becoming even more critical with growing use of semiconductors in health, transportation and safety applications. Automated formal verification, while essential, is inherently an extremely complex technology, often resulting in exorbitant compute time or memory capacity when applied to larger and more complex designs. Researchers at the University of California/Berkeley, have provided what SRC Member companies describe as "best in class" verification tools that have solved hard combinational equivalence checking problems for industrial examples that could not be handled before, even with commercial tools. Their work has become the new standard in academic and industrial research on verification and logic synthesis, and is used in design flow by several companies. Its increasingly high performance verification capabilities enabled it to win the worldwide 2010 Hardware Model Checking Competition.

Moving to 45 nm technology and below produces standard cells that are prone to lithography proximity and process variations, requiring increasingly sophisticated design-for-manufacturability (DFM) techniques. Designing robust cells under these variations plays a crucial role in the overall circuit performance and yield. Member companies are using several DFM techniques

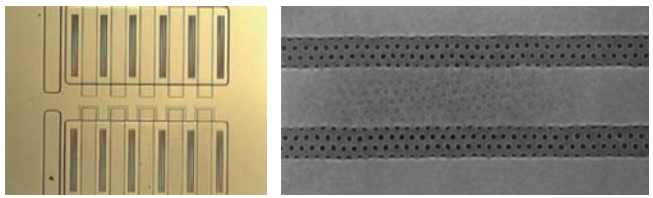


FIG.4
CMOS Inverter circuit. Right: block copolymer self-assembled contact holes (20 nm) in a CMOS inverter circuit

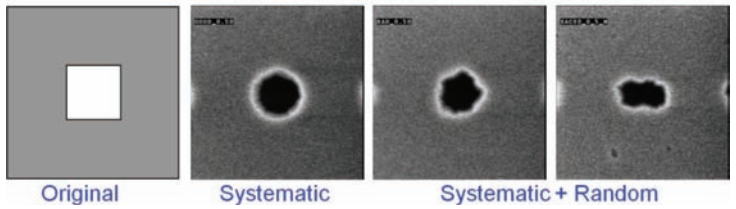


FIG.5
Contact Edge Roughness Effects

from research at the University of Texas/Austin for improving performance and process variability in libraries and internal layout generation and optimization tools. This work has produced robust layout optimization tools that minimize total delay sensitivity and achieve up to 90% reduction in leakage current on 45 nm industrial examples. [FIG.5]

As the penetration of electronics into additional markets continues, the requirements of the end system are imposed on the electrical subsystems. These requirements are then passed down to the underlying integrated circuits. For example, electronic systems in automobiles operate in harsh environments. Components that satisfy the stringent reliability requirements can greatly impact the end user, as technology advances are able to deliver more safety, efficiency and comfort to drivers and passengers. With a lifespan of a dozen years or more, the reliability requirments for circuits in automotive applications can be more stringent than for applications that are used for a shorter length of time, such as a mobile phone. Thus, reliable operation in harsh environments and over time is of increased importance.

As integrated circuits are used for long periods of time, they are subject to electronic wear-out through various effects, such as hot carrier injection (HCI), bias temperature instability (BTI) and time-dependent dielectric breakdown (TDDB). Monitoring and characterizing these effects is critical for reliable operation of circuits manufactured with advanced technologies. Researchers at the University of Minnesota have developed an all-in-one "silicon odometer" test chip capable of separately monitoring the stated reliability degradation effects. This gives circuit and system designers the information needed to ensure reliable circuit operation over long operating lifetimes.

In many systems, moving data between computing elements and memory is the key bottleneck that determines how much computation can be done. Thus, the communications channel between subsystems is pushed to the limits to deliver data with reliability, while using the least amount of power and chip area. These links are stacked together to form a dense data communication channel and thus can be subject to electronic crosstalk noise, often generated by a nearby lane. GRC research at the University of Minnesota, supported through the Texas Analog Center of Excellence (TxACE), has investigated low-power techniques to cancel the crosstalk that may be present in such channels, thus enabling more reliable data transmission at low power levels. This research, applied to a 4X4 multiple-input-multiple-output circuit running at 10 Gbps, is projected to use only 25% of the power of previously published techniques. [FIG.6]

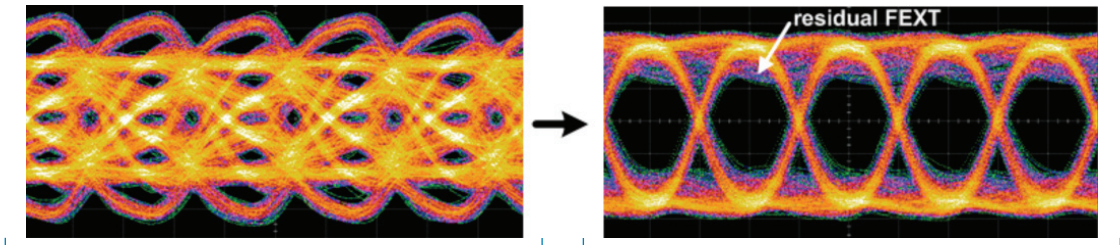
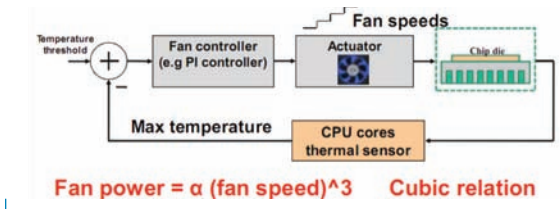


FIG.6
Before crosstalk cancellation

After crosstalk cancellation

Focus Center Research Program



MuSyC
Fan control and cooling cost

RESEARCH FOCUS: U.S. SECURITY & ECONOMY

Established in 1998 to conduct innovative, multi-university research in semiconductor technology with an eight+ year horizon, the Focus Center Research Program (FCRP) targets the intractable challenges in semiconductor-based technology on behalf of its Sponsors, which include the Department of Defense (DARPA), the microelectronics industry and the defense contractor community. FCRP research employs a hierarchy of approaches for integrated electronics, ranging from nanomaterials, novel devices and circuit techniques, to system level design methodology including new "chip" architectures, all the way to full system platforms and multi-scale systems design. Research in such technology enablers generates crucial results for both micro- and macro-electronic systems of the future, maintains a world-leading academia-based semiconductor research engine, and is aimed at providing leading edge solutions to the U.S. Department of Defense, while addressing the technology needs of the semiconductor and defense systems industries.

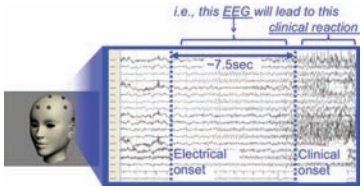
This year was the first full year of research for the newest center, MuSyC, conducting research beyond the integrated circuit realm and into multi-platform systems. The FCRP collaborative endeavor to extend the CMOS transistor roadmap involves 41 universities, 333 faculty and over 600 graduate students through six centers. FCRP research, led by the university Center Directors and guided by the industry and DoD Sponsors is creating the breakthroughs that are critical to U.S. security, healthcare, and economic competitiveness goals and gives participating companies a tremendous advantage in their ability to develop leading products and systems in this race along the technological revolution.

FCRP CENTER 2010 HIGHLIGHTS

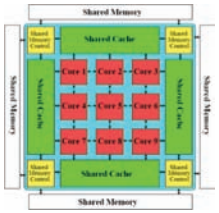
MULTI-PLATFORM SYSTEMS RESEARCH CENTER (MuSyC)

In state-of-the-art systems such as those found in data centers, workload scheduling and server fan speed operate independently leading to cooling inefficiencies. In this work the researchers propose GentleCool, a proactive multi-tier approach for significantly lowering the fan cooling

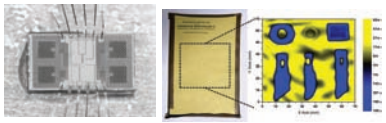
MuSyC
Mapping of brain activity zones



GSRC
EEG based seizure onset detection



GSRC
Multi-core processor



C2S2
Imaging chip for recognizing objects through packaging

costs without compromising performance. The technique manages fan speed through intelligent allocation of the workload across different machines. Experimental results show this approach delivers average cooling energy savings of 72% and improves the mean time between failures (MTBF) of the fans by 2.3X compared to the baseline.

Researchers are also investigating local cortical computation and long-range communication relating to brain-machine-interfaces (BMI). They have found that neuronal oscillations may play a key role in coordinating both local and large-scale activity and that phase coherence influences effective connectivity between cortical areas. A dynamic oscillatory hierarchy serves as an organizing structure for multiple spatial and temporal scales.

GIGASCALE SYSTEMS RESEARCH CENTER (GSRC)

The goal of embedded healthcare is to provide a high-level of monitoring and therapy over a very large population by using as few clinicians as possible. A low-power seizure detection system for chronic use by epilepsy patients is being investigated. The key technology is a System-on-Chip (SoC) that integrates a low-noise instrumentation amplifier, ADC, and digital processor to stream feature vectors to a machine learning classifier. This device also serves as a vehicle to highlight the specific needs and opportunities presented by embedded healthcare in terms of low-power computing platforms, application-level resiliency, and noisy processor outcomes.

Cores/threads in a multi/many-core system share multiple hardware resources in the memory subsystem. If threads are not prioritized intelligently in shared memory subsystem resources, system performance can degrade significantly, and some important threads may be starved for long time periods. In fact, effective programs can be written to deny service to other concurrent programs by exploiting the unfair prioritization mechanisms in shared multi-core resources. Recent research has focused on solving these problems by designing control mechanisms for shared resources (memory controllers, on-chip networks and caches) that improve both system performance and system fairness.

CENTER FOR CIRCUITS & SYSTEMS RESEACH (C2S2)

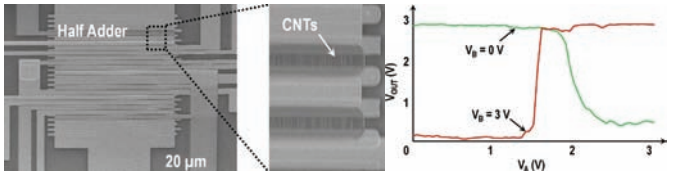
Researchers have recently implemented and demonstrated the use of diode detectors operating at 270-290 GHz for sub-millimeter wave applications such as imaging. Their recent experiments showed a circuit responsiveness of approximately 210 V/W (without amplification), that is about three times better than anything previously reported. The use of Schottky diodes in CMOS was shown to be significantly superior to using MOS transistors.

In another research effort, carbon nanotubes (CNTs) are grown using chemical synthesis, and the exact positioning and chirality of CNTs are very difficult to control. As a result, "small-width" carbon nanotube field-effect transistors (CNFETs) can have a high probability of containing no semiconducting CNTs, resulting in CNFET failures. Upsizing these vulnerable small-width CNFETs is an expensive design choice since it can result in substantial area/power penalties. C2S2 researchers have introduced a processing/design co-optimization approach to reduce the probability of CNFET failures at the chip-level by enforcing the active regions of CNFETs to be aligned with each other. This approach relaxes the device-level failure probability requirement by 350X at the 45 nm technology node, leading to significantly reduced costs.

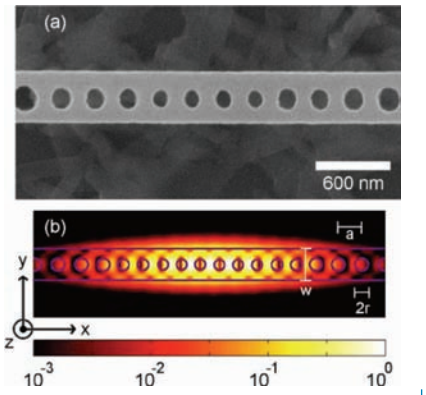
INTERCONNECT FOCUS CENTER (IFC)

State-of-the-art optical modulators are based on resonator structures in which the refractive index modulation is performed by free carrier injection, which subsequently alters the cavity resonance and the transmission of the signal beam. Using silicon micro-ring resonators, researchers have been able to achieve GHz modulation with ~100 fJ control pulses. Achieving operation at sub-10 fJ control with speeds exceeding 10 GHz, as is required by the ITRS roadmap, however, remains a big challenge and requires radical approaches. IFC researchers are working on modulators based on photonic crystal nanocavities, and the demonstration of single quantum dot-nanocavity modulators that can operate at sub-fJ control energies with the speeds exceeding 20 GHz.

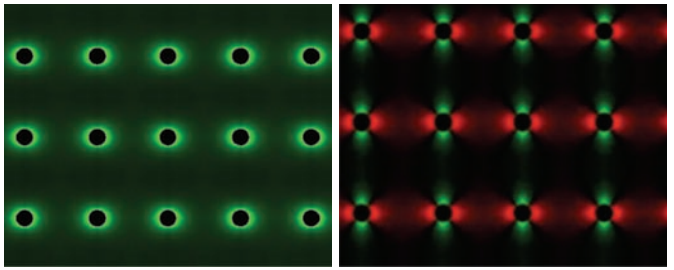
In another IFC effort, through-silicon via (TSV) fabrication causes tensile stress around TSVs which results in significant carrier mobility variation in the devices in their neighborhood. Keep-out zone (KOZ) is a conservative way to prevent any devices/cells from being impacted by the TSV-induced stress. However, owing to already large TSV size, large KOZ can significantly reduce the placement area available for cells, thus requiring larger dies which negate improvement in wire length and timing due to 3D integration. Researchers in this center propose a new TSV stress-driven force-directed 3D placement that consistently provides placement result with, on average, 21.6% better worst negative slack (WNS) and 28.0% better total negative slack (TNS) than wirelength-driven placement.



C2S2
Half Adder using CNT Logic



IFC
Photonic Crystal Cavity



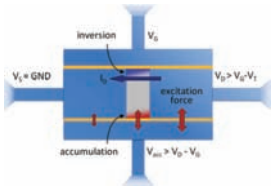
(a) Hole mobility (b) Electron mobility

IFC
Carrier mobility variation surface surrounding TSVs

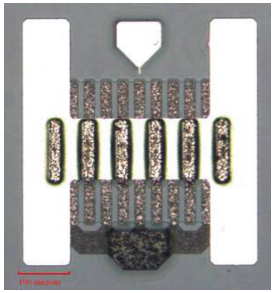
MATERIALS, STRUCTURES AND DEVICES RESEARCH CENTER (MSD)

With quality factors (Q) often exceeding 10,000, vibrating micromechanical resonators have emerged as leading candidates for on-chip versions of high-Q resonators used in wireless communications systems. However, as in the case for transistors, extending the frequency of MEMS resonators generally entails scaling of resonator dimensions. Unfortunately, smaller size often coincides with lower-power handling capability and increased motional impedance. Resonant Body Transistors (RBTs) have excellent figure of merit (f x Q) for use as acoustic resonators. Researchers in this Theme have introduced novel solid-state transduction techniques and have proposed mechanisms for coupling MEMS resonators with silicon photonics, spin-torque oscillators and mechanical systems in the quantum regime.

Power electronics represents 20% of the semiconductor business. It is not only important from an economics point of view, but it also has a tremendous impact on global energy consumption and the ultimate performance of many electronic systems, such as microprocessors. It has been estimated that more extensive utilization of power electronics could lead to a reduction of roughly 15-20% of electricity consumption in the U.S. At the same time, roughly 30% of power losses in modern microprocessors could be saved with improved power electronics. A new generation of power electronics based on GaN semiconductors is currently being developed to address these opportunities by providing lower power losses and unprecedented integration capability.



MSD
Resonant Body Transistor

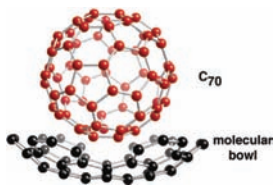


MSD
GaN Power Transister

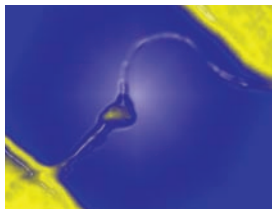
FUNCTIONAL ENGINEERED NANOARCHITECTONICS CENTER (FENA)

FENA researchers have synthesized a new type of bowl-shaped polycyclic aromatic hydrocarbon, formed by joining the proximal carbons of contorted hexabenzocoronenes. These methods begin to tap a wealth of structural diversity available from these core structures. The bowl-shaped hydrocarbons more easily accept electrons than the molecular bowls and C_{70}. This work, published in *Chemical Science*, may provide a route to a highly functional device ("Bending Contorted Hexabenzocoronene into a Bowl", A. C. Whalley, K. N. Plunkett, C. L. Schenck, A. A. Gorodetsky, C.-Y. Chiu, M. L. Steigerwald, C. Nuckolls, 2010, Chem. Sci.).

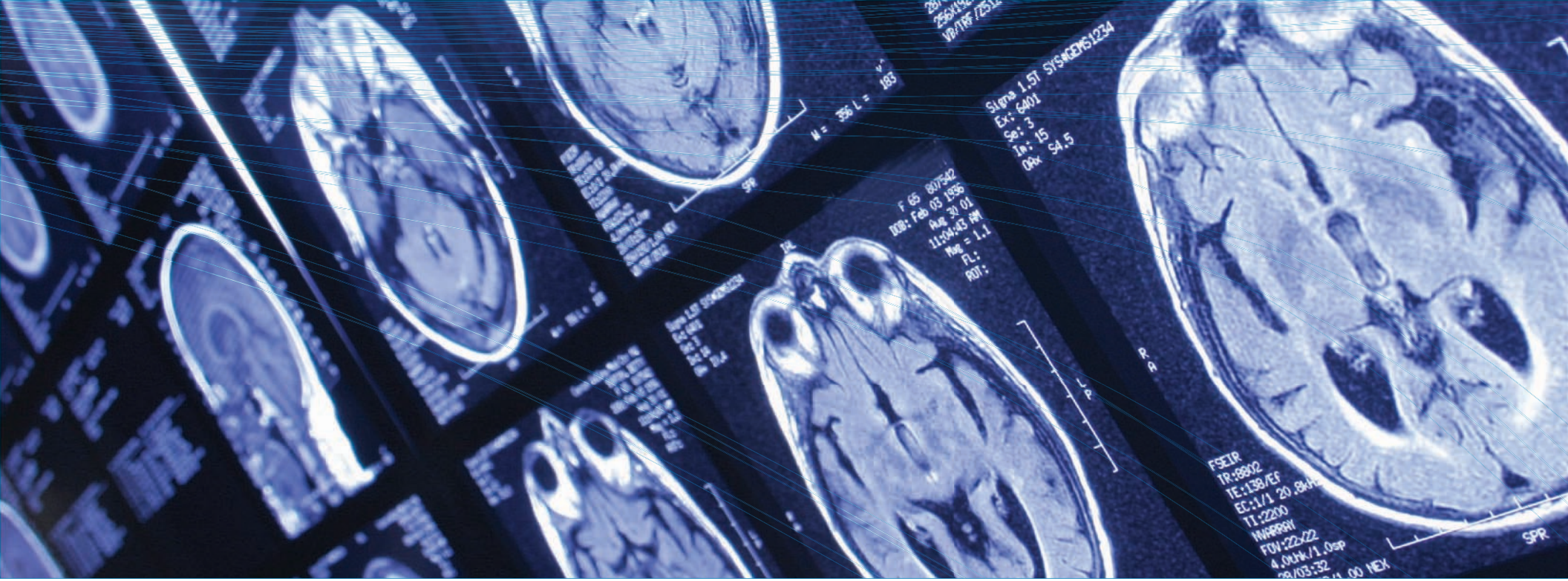
The semiconductor industry is developing lithographic technology for feature sizes below 22 nm and exploring new classes of transistors that use carbon nanotubes or silicon nanowires (NWs). A major goal of this nanotechnology is to couple the self-assembly of molecular nanostructures with conventional microfabrication, which will enable the researchers to register individual molecular nanostructures and integrate them into functional devices. One strategy uses the inherent recognition and self-assembly capabilities of DNA. Researchers report the use of DNA towards the assembly and electronic functionality of nanoarchitectures based on conjugates of CNTs and NWs, as well as DNA computing on a Si-CMOS platform.



FENA
Molecular Bowl



FENA
CNT-ss DNA-CNT fixed between metal contact s



IMPACT: EMERGING RESEARCH

Recent advances in neuroscience and engineering using miniature, implantable neural sensors have the potential to make substantial differences in the lives of millions who are paralyzed or have suffered a devastating stroke or the loss of a limb. Brain-Machine Interfaces (BMI), a young multidisciplinary field that has huge potential as a therapeutic technology, has grown tremendously during the last decade. Researchers have already exhibited compelling demonstrations of BMIs in animals and humans. This technology holds the potential to improve the quality of life for those who are physically impaired.

BMI is about transforming thought into action, or conversely, sensation into perception. For this technology to make the step from laboratory experiments on animals to true application in humans, dramatic improvements are required in many different areas. Among these are micro-sensors, data acquisition, intelligent signal processing and the power and data transmission interface. For instance, it has been demonstrated that amputees can be outfitted with prosthetic arms directly controlled by cortical signals, enabling them to perform everyday reaching and grasping movements that would otherwise be impossible. But much more work is needed in this area and SRC is addressing this research need. Neural prosthetic systems aim to help severely disabled patients suffering from neurological injuries and diseases by decoding neural activity into control signals for assistive devices.

Neural sensing nodes must be the size of a few square millimeters, communicate with the outside world using secure, low-power wireless, and be completely self-contained from an energy perspective. The small size, combined with safety regulations, puts an upper limit on the power available for establishing wireless connectivity and performing additional tasks such as data acquisition. Researchers from SRC's Focus Center Research Program (FCRP) have created a mixed-signal data acquisition channel that is a record-breaking 1/100 of a square millimeter in size (3 times smaller than the best of the state-of-the-art) and consumes only 5 μW of power, while presenting only 6 μV rms of noise to the channel over a 10 kHz bandwidth. The ability to interpret physiologically-complex patient signals on a continuous basis and at microwatt power levels will enable intelligent, closed-loop biomedical devices, as well as unobtrusive chronic health monitors that can provide actionable clinical-decision support for highly scalable and geographically dispersed healthcare.

Nanoelectronics Research Initiative

SEEING 2020 & BEYOND

The Nanoelectronics Research Initiative (NRI) is a consortium of companies in the Semiconductor Industry Association seeking to find a device that can scale computer technology beyond the ultimate limits of current CMOS transistors. This university-based research, cooperatively funded by industry and federal and state governments, is looking toward nanoelectronics in the year 2020. With a goal of discovering the next switch–a new mechanism for computing that goes beyond simply improving today's transistor, NRI engages the most talented students to become the innovators and leaders of tomorrow's technology industry.

Groundbreaking NRI research was conducted at over 35 universities in 22 states in 2010. The projects are organized into multi-university centers, which are jointly funded with the National Institute of Standards and Technology (NIST), and at National Science Foundation (NSF) nanoscience centers. And given the exploratory nature and potential benefits of the research, which seeks out entirely new device and computation technologies, it is particularly significant that industry, government and academia work together closely to rapidly identify and develop emerging research paths that show potential to extend the historical cost and performance trends for information technology.

NRI PROGRAM HIGHLIGHTS

One of the primary challenges for NRI is to foster strong connections between the physicists and chemists doing the basic science work (often in emerging fields where new discoveries come at a rapid pace), and the engineering researchers who must figure out how these phenomena could enable a new device. This year was a particularly pivotal year for NRI, as the centers each focused their work to identify the most promising device concepts that would continue into the next phase of NRI research in 2011–maintaining NRI's vision of being a goal-oriented, basic-science research program. Moreover, the individual researchers working on the NRI-NSF projects continued to interact directly with the NRI centers, making key scientific contributions that both increased the understanding and development of the devices within the centers, and also pointed to new phenomena that could lead to additional device concepts in the future.

To encourage even more interaction between NRI and government agencies and researchers, the fifth NRI Annual Review was held in Gaithersburg, Maryland, adjacent to the NIST labs. Many NIST personnel attended, as well as numerous invited visitors from other federal agencies in the DC area. NRI is considered a model for public-private research partnerships, both at the federal and state level, and we continue to seek opportunities to grow our existing partnerships and expand our work with new agencies. Our partnership with NIST, for example, continues to grow beyond just the funding that NIST provides; the end of 2010 saw over a dozen NRI-related projects being performed at the NIST labs in direct collaboration with NRI university researchers, as well as an NRI post-doc supported at NIST, taking advantage of the unique tools and capabilities of those facilities. In addition, we were very happy to announce a new $20M joint program with NSF on "Nanoelectronics Beyond 2020", and we plan to launch the new projects in mid-2011.

NRI RESEARCH HIGHLIGHTS

Throughout 2010 NRI has been focused on carefully analyzing its research portfolio, including an extensive benchmarking effort to gauge the opportunities and challenges presented by the various new device approaches. The highlights of this effort were seen in the readout of the benchmarking study at a workshop in August, and then in the final selection of projects at the end of the year, which will continue into NRI Phase 1.5 in 2011-2012.

The Benchmarking Study was one of the most comprehensive ever attempted for such exploratory device concepts. It looked at all aspects of the devices, not only in isolation but also in small circuits, such as inverters and adders, which better judge the devices' potential for doing computation. Given the intense interest in the NRI research by both industry and academia, the IEEE Proceedings requested an invited paper giving an overview of the current results ("Device and Architecture Outlook for Beyond CMOS Switches," K. Bernstein, R.K. Cavin, W. Porod, A. Seabaugh, and J. Welser, *Proceedings of the IEEE Special Issue – Nanoelectronics Research: Beyond CMOS Information Processing,* Vol. 98, No. 12, December 2010). A good summary of these results is captured in [FIG.1], showing how various devices compare on key metrics for an inverter including speed, energy and interconnect delay. The results were very enlightening: many of the devices showed major advantages in power, but most also had challenges in speed as compared to modern CMOS. This has led to a renewed focus on the importance of architecture for NRI's mission, and the benchmarking work will expand in Phase 1.5 to look at more novel circuit applications for the devices.

The Phase 1.5 Projects were chosen using both the benchmarking results and extensive technical discussions at the NRI center onsite reviews and the Annual Review. This balance between quantitative and qualitative inputs is crucial to the NRI approach: benchmarking is not a weapon intended to prematurely cut off new, out-of-the-box ideas; it's a tool for guiding the research on these ideas in the most successful directions.

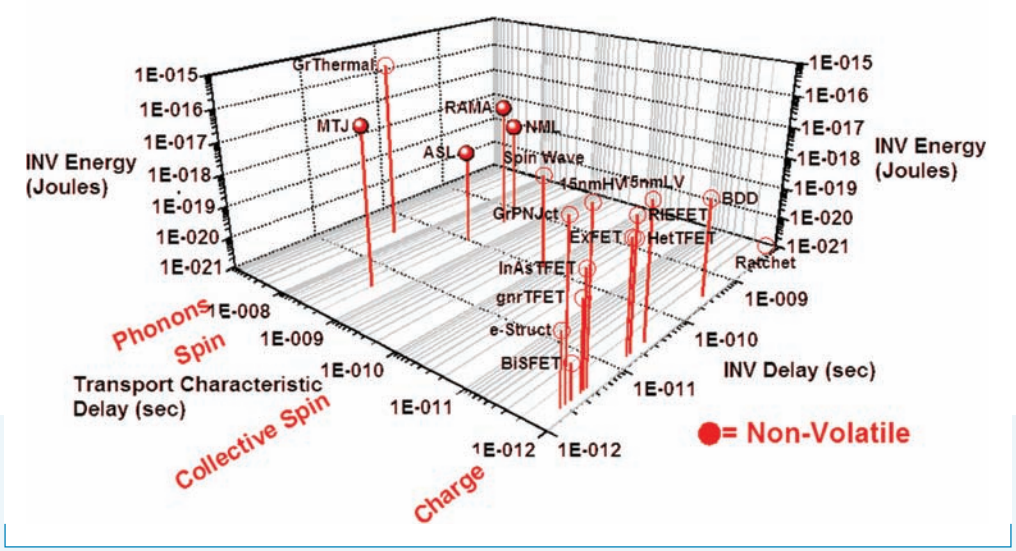


FIG.1
Intrinsic Switch / Transport Venue Composite Benchmarking

WIN: Western Institute of Nanoelectronics, UCLA (Kang Wang, Director)

WIN will continue to research spintronics and related phenomena for logic applications, with a focus on four primary devices. The Spin-Wave device [FIG.2] focuses on manipulating and transporting spin directly (without actually moving charge), offering the potential for very low energy operation. The Spin-Torque device [FIG.3] capitalizes on the progress being made in memory and storage devices on manipulating spin with currents, looking for novel ways to adapt this to logic devices. The SpinFET [FIG.4] is a more traditional spintronic transistor, but with potentially improved performance due to the discovery of a novel channel material structure based on MnGe that could act as a room temperature dilute magnetic semiconductor. And finally, the NanoMagnetic Logic (NML) program [FIG.5], which is being done in conjunction with the MIND Center, will look for ways to advance the use of nanoscale magnets for doing logic, taking advantage of their natural non-volatility for potentially very low energy applications.

MIND: Midwest Institute for Nanoelectronics Discovery, Notre Dame (Alan Seabaugh, Director)

In addition to the work on NML with WIN, the MIND Center is looking at a number of tunneling devices which show great promise in overcoming the low on-off current ratio which has plagued these devices in the past. The primary approaches being researched include the use of staggered-gap heterojunctions, one-dimensional nanowires and the use of graphene as the channel material. [FIG.6] MIND has also taken the lead on pursuing novel architectures for a variety of NRI devices and has been spearheading the benchmarking effort across the program.

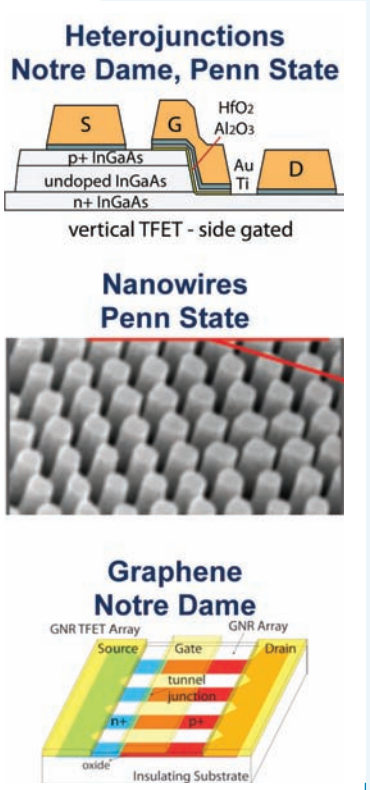


FIG.6
Tunnel Devices
MIND – Notre Dame

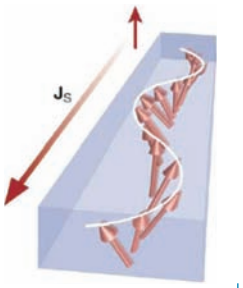


FIG.2
Spin Wave Device
WIN – UCLA, UCSB

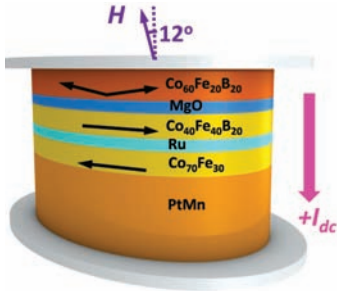


FIG.3
Spin – Torque Device
WIN – UCI

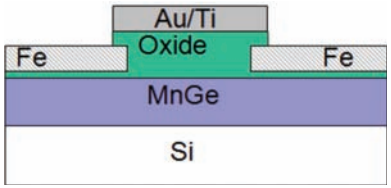


FIG.4
Spin – FET
WIN – UCLA

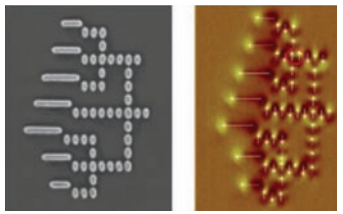


FIG.5
Nanomagnet Logic
MIND – Notre Dame
WIN – Berkeley

SWAN: SouthWest Academy for Nanoelectronics, UT/Austin (Sanjay Banerjee, Director)

In Phase 1.0, the SWAN Center proposed a novel device, the Bilayer pseudoSpintronic FET (BiSFET), which relies on the formation of a room temperature exciton condensate between graphene bilayers. [FIG.7] Extensive simulation work, ranging from basic physics through circuit modeling, indicates that this device has the potential to run at speeds comparable to CMOS while consuming orders of magnitude less power; and in Phase 1.5 the center is launching a large experimental effort to test whether this theory will prove viable. Moreover, the teams working on all aspects of the device materials, fabrication and characterization will greatly advance capabilities for building any future graphene structure, so significant collateral benefits are also expected.

INDEX: Institute for Nanoelectronics Discovery and Exploration, SUNY/Albany (Alain Kaloyeros, Director)

The INDEX Center is taking advantage of two other unique properties of graphene, which should allow for very low energy transport and switching. In one case, they are building devices and interconnects that use p-n junctions to steer the electron current in different directions. [FIG.8] In the other, they are using the very long spin lifetime of graphene to build an all-spin logic circuit [FIG.9] that uses magnets for non-volatile input, output and storage. INDEX will also maintain its strong focus on fabrication, taking advantage of the extensive capabilities of the Albany Nanotech Center by developing a method to integrate graphene onto 300 mm silicon wafers for a more mainstream process flow.

At the Annual Review it was noted that much of the work in 2010 really honed in on finding ways to address the key NRI challenge: *finding a new device that can operate at room temperature but at much lower power than existing technology.* Many of the resulting breakthroughs have now laid the groundwork for a focused set of projects in Phase 1.5 that show great potential not only for making progress towards the "next switch", but also for producing exciting discoveries that could launch a host of related new technology innovations for the future.

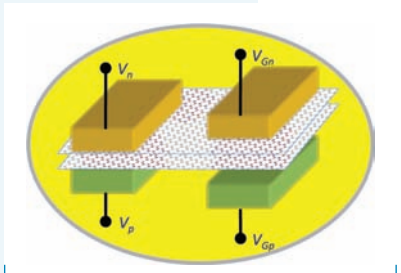


FIG.7
Bilayer pseudoSpin FET
SWAN – UT Austin

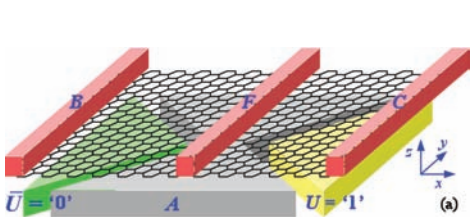


FIG.8
Graphene PN Junction
INDEX – SUNY Albany

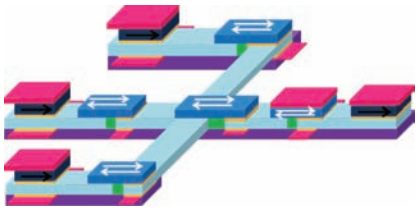


FIG.9
All-Spin Logic
INDEX – Purdue

IMPACT: ENERGY

As the sun rises, a gentle chime signals the surge of solar-generated power, while simultaneously the status of household electrical appliances and Plug-in Electric Vehicles appears on a screen. The morning is crystal clear, and as electricity from distant solar farms and overnight winds is seamlessly merged into the grid, clean and sustainable energy begins yet another day.

ENDLESS ENERGY? It is not just a dream. SRC's Energy Research Initiative (ERI) is developing the tools and technology that will enable us to cheaply produce solar electrical power and efficiently harness and store not only solar energy but other renewable energy resources as well. At Purdue University, researchers are exploring and discovering the secrets of solar cell technology at the atomistic level in order to develop models that will enable manufacturing process optimization for improved performance and reliability–as well as lower cost. Models for semiconductor device fabrication that were developed decades ago had a profound effect on that industry, and a similar impact is expected for the photovoltaic (PV) industry.

However, integrating renewable energy resources into the grid is not an easy task due to fluctuations in electricity output from passing clouds, varying winds, etc. Researchers at Carnegie Mellon University are developing simulators that incorporate real-time sensing and control–a "smart grid"–to seamlessly merge renewable energy resources into the electricity grid and also actively manage loads to prevent blackouts. The eventual worldwide rollout of smart grids is projected to grow from approximately $13 billion today to $34 billion by 2020, creating new jobs and business opportunities.

A third and essential component of a sustainable and reliable grid is to efficiently manage and store energy, and during 2011 ERI will establish a new research center for Power Management and Energy Storage to address this important topic. While the complexity of our energy challenges cannot be understated, ERI research will provide a significant contribution towards ensuring that the world's future energy needs are met by a clean, affordable and reliable electrical energy generation and distribution system.

Energy Research Initiative

SEEKING TOMORROW'S SMART ENERGY SOLUTIONS

SRC's Energy Research Initiative (ERI) program brings together a consortium of companies in the global energy sector to collaboratively fund university research for more efficient, responsive and reliable electrical energy systems. ERI's core mission is to enable reliable low-cost renewable energy systems and efficient energy use and distribution through an enabled and optimized smart grid.

KEY ERI OBJECTIVES

> Develop modeling/simulation tools and technologies to address the performance, cost, reliability and manufacturing challenges of photovoltaic technologies that enable grid parity.
> Develop the modeling, simulation and control tools needed to manage, optimize and secure the power grid and enable personal energy systems, thereby creating a new paradigm for the global electricity infrastructure.
> Develop new and more efficient electrical energy storage systems to support the integration of renewable energy resources and personal energy systems into an aware and enabled smart grid.

ERI was officially launched in July 2010 with seven founding members (ABB, Applied Materials, Bosch, First Solar, IBM, Nexans and Tokyo Electron) and two Centers of Energy Research Excellence: the Network for Photovoltaics Technology (NPT) at Purdue University and the Smart Grid Research Center (SGRC) at Carnegie Mellon University. With the establishment of these two centers, as well as a future center to address the related topic of Power Management and Energy Storage [FIG.1], SRC is spearheading the fundamental precompetitive energy research that will have broad benefits as the world strives to meet its future energy needs.

NETWORK FOR PHOTOVOLTAIC TECHNOLOGY (NPT)

The Network for Photovoltaic Technology (NPT) Center at Purdue University is addressing the performance, cost, reliability and manufacturing challenges of photovoltaic technologies. The center will leverage Purdue's extensive modeling/simulation expertise and national Network for Computational Nanotechnology (NCN) framework to provide enabling analytical models and simulation tools for photovoltaic manufacturers, much as Purdue has done for the semiconductor industry.

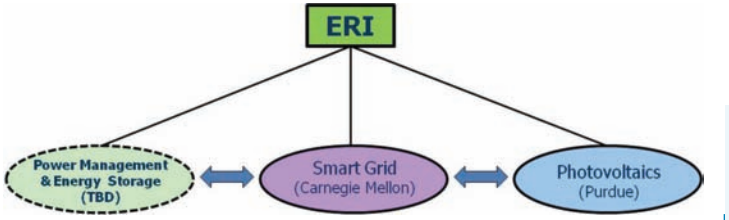


FIG.1
ERI Centers of Energy Research Excellence

INITIAL RESEARCH TASKS WITHIN THE NPT CENTER:

Modeling of Morphology of Micro-crystalline and Poly-crystalline Thin Films | Develop an experimentally-guided simulation methodology and web-accessible software to predict the distribution of grain-sizes, grain-boundaries and surface roughness in materials like CdTe and a-Si/μ-Si.

Morphology-Aware Modeling of Thin-Film Solar Cells | Develop a simulation framework for thin-film solar cells that correlates electrical performance with grain boundary properties as a function of process parameters.

Solar Cell Characterization for Device Analysis and Modeling | Develop accurate, efficient and validated procedures for characterizing the critical material and device parameters that determine solar cell performance, with emphasis on in-line characterization methodologies.

Physics-Based Compact Models for PV Devices and Systems | Develop an experimentally validated, physics-based compact model for performance and reliability predictions of thin-film and crystalline PV, and a web-enabled modeling framework to translate cell performance to module performance using compact models.

Modeling and Simulation of Si-Heterojunction and Poly-Emitter Solar Cells | Develop a physics-based model for Si-heterojunction and poly-emitter solar cells to provide experimentally verified guidelines for high-performance Si-based solar cell design.

The overarching goal of the NPT Center is to provide predictive models for photovoltaic device performance and reliability. Surface roughness, grain-boundaries and device structure dictate PV performance, yet there is no predictive simulator in the PV industry that can translate process conditions to device structure/morphology to ultimate PV performance and reliability. Predictive simulators, such as SUPREM that were developed decades ago to optimize semiconductor device fabrication, had a profound effect on the semiconductor industry; NPT's goal is to provide models which will have a similar impact on PV manufacturing.

SMART GRID RESEARCH CENTER (SGRC)

A multi-university Smart Grid Research Center (SGRC) at Carnegie Mellon University is working to support the incorporation of renewable energy resources and provide the modeling, simulation and control tools needed to manage, optimize and secure the power grid. SGRC will develop the dynamic monitoring and decision systems (DYMONDS) required to create a new paradigm for the electricity infrastructure. In addition, personal energy systems will be enabled, providing individuals and organizations choices and flexibility in their use of energy.

INITIAL RESEARCH TASKS WITHIN THE SGRC CENTER:

Adaptive Load Management (ALM) | Develop an economic model (software simulation/tools) and decision-making strategies (algorithms and software implementation) for load aggregators that comprehend uncertainty in supply/demand and incorporate adaptive load management.

Dynamics and Control of Smart Grids: Combined Effects of Phasor Measurement Units (PMUs), Dynamic Line Rating Units (DLRs) and System Dispatch | Develop novel concepts for modeling system dynamics, supported by fast and accurate measurements and sensors, for optimized dispatch.

Nonlinear Control of Flexible AC Transmission Systems (FACTS) for Transient Stabilization | Demonstrate use of FACTS to transiently stabilize the response of complex power networks during major equipment failures.

Pushing the Limits to Computing: Managing Resources in a Reliable and Efficient Way in Large-Scale Electric Power Grids | Introduce a new computational framework for managing energy resources in which inter-temporal and inter-spatial dependencies are critical for making the system reliable and efficient.

National Institute for Nanoengineering

A JOINT VENTURE

The National Institute of Nanoengineering (NINE) program is a collaboration among industry participants, Sandia National Laboratories and the Department of Energy. The program is set up to deliver value to the industry Members through access to Sandia's Microsystems and Engineering Sciences Applications (MESA) facilities, including research clean rooms and Sandia's high performance computational research facilities.

The NINE program was initiated to build upon the unique resources available at Sandia in order to address nanoengineering challenges of interest to industry and to Sandia. The program will also develop a pipeline of relevant, skilled individuals to help meet laboratory and industry personnel needs in the future.

NINE has five areas of research pursuit:

> Sensors
> Nano-patterning
> Directed self assembly
> Nano-composite materials
> Energy

The alliance between SRC industry Members and the combined teams of university and Sandia researchers have produced some promising early results. The NINE program recognizes the many unique facilities and skills that Sandia has to offer, and it demonstrates the exceptional strength of SRC's collaborative endeavor among researchers, students and industry Members.

New & Emerging Research Initiatives

APPLYING COLLABORATIVE RESEARCH TO NEW HORIZONS

SRC has the unique ability to launch new research initiatives in response to industry needs. Such initiatives build upon our legacy of creating research communities and finding synergies across disciplines and industry sectors. These newest programs are an integral component of SRC's long-term strategy to continue to provide value by addressing research needs adjacent to historic areas of focus. New initiatives are generally driven by applications important to SRC Members, complementing existing research and applying the same revolutionary pre-competitive collaborative research methodologies that made SRC pioneers in the semiconductor industry. For greater flexibility and to make these initiatives more broadly attractive, they may involve relatively short-term commitments at the outset from industry and academia. The following areas are currently being explored for emerging research initiatives.

Bioelectronics is the interdisciplinary science, engineering and technology at the intersection of semiconductor electronics and biology–often at the nanoscale level. Convergence among these sectors and disciplines points to novel applications and products in the fields of medicine, healthcare, assistive technology, security, etc. Driven by Moore's law, information and communications technologies are making possible the collection, transmission, analysis and delivery of enormous amounts of data/information/knowledge in near real-time. In the longer-term, market opportunities are being driven by aging populations, rising healthcare costs, and the increasing ability to reach underserved populations (in developing countries and rural areas), as well as to meet the needs of persons with disabilities.

Sensors research is an area that has large potential for impact on emerging semiconductor applications, including bioelectronics. Biomedical diagnostics and monitoring, drug discovery and applications such as forensics, food and water safety, and environmental monitoring all depend on sensors. In the future, sensors will be combined with semiconductor and information technology to enable continued development of cyber-physical systems that can network and provide information on a global scale. Research challenges span the range of sensor types–physical, chemical and biological–and integration into systems that include power, communications and analytical capabilities.

Networked, "smart" devices that include sensors are part of the explosive growth in the scale and use of cyber infrastructure, which has led to a parallel demand for cyber security. Connected information technology systems are vital for the functioning of government agencies, critical infrastructure, financial systems and myriad commercial, public and private activities. Not unlike public health, cyber security requires proactive and reactive measures. Research is needed to ensure safe and secure systems without impeding economic and social benefits. A strong partnership with government agencies is particularly important in the area of cyber security.

SRC Education Alliance

DISTINCTIVE RESEARCH, MEANINGFUL ENGAGEMENT

As a private foundation, SRC Education Alliance is home to programs that complement and support SRC's research mission. The Education Alliance develops sources of funding to sustain and grow the pipeline of high quality scientists and engineers. Today, the Education Alliance provides undergraduate and advanced degree science and engineering students with a unique education consisting of traditional coursework, cutting-edge research and direct interaction with industry.

Students are supported by SRC and the Education Alliance through research contracts and grants, fellowships and scholarships, and the Undergraduate Research Opportunities (URO) program. By offering financial support, mentoring and industry-relevant research with SRC-funded faculty who are recognized experts in their fields, the Education Alliance attracts the best and brightest students and helps them forge their pathway to become technology leaders and drive tomorrow's innovations.

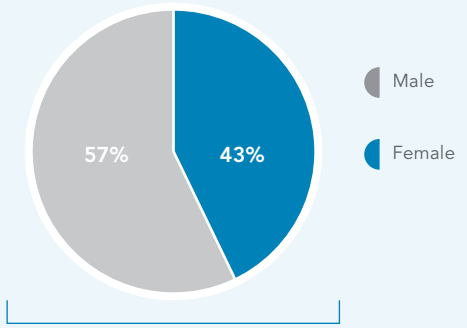
The Graduate Fellowship Program encourages academically gifted students to pursue doctoral degrees, developing a cadre of the highest quality doctoral graduates for careers with Member companies and universities. SRC reaches out to students from under-represented populations via "pipeline programs" including the Master's Scholarship Program and the URO program.

The Education Alliance is now expanding to leverage past successes and broaden its impact. As a private foundation, the Alliance will develop impactful sources of funding, increasing the ability to build the pipeline of students and broaden the diversity at various levels of education. Through fellowships and scholarships, the Education Alliance will continue to connect students with science- and technology-based industries and show them how to transform research results into useful products that influence change.

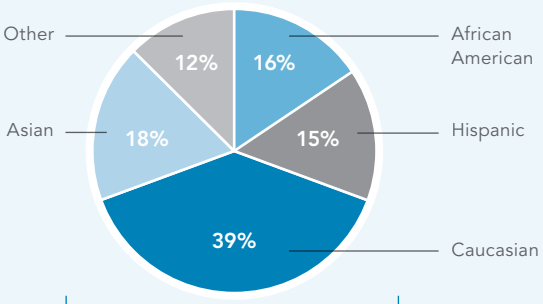
Supported by a grant from the Intel Foundation, URO aims to retain a diversity of high quality undergraduate students in STEM degree programs and increase the number of students that pursue an advanced degree. Students benefit from hands-on research experience, mentoring and programs that promote and support application to graduate school.

2009-2010 URO AT A GLANCE:

- Supported 230 students at 14 universities
- Average GPA of 3.5
- 86% retained in STEM degree program
- More than 40% female & 30% under-represented groups
- 68% progressed to graduate studies in a STEM discipline
- 6 students continued as SRC-funded graduate students, including Master's Scholar and Graduate Fellow
- 7 students co-authored journal articles
- 118 students made presentations outside their research groups
- 29 students presented at TECHCON 2010
- 4 students received university-level awards for outstanding research
- 1 student was included as an inventor in a patent application



GENDER



DIVERSITY

SRC STUDENT RELATIONS

One of the benefits of SRC's cooperative research programs is the number of students being educated to enter the semiconductor and nanoelectronics fields. Each year, SRC supports more than 1,500 advanced degree students on research contracts guided by industry. Since SRC's inception in 1982, more than 8,000 students have significantly contributed to the SRC research portfolio and the dissemination of its results through their participation in national conferences, invention disclosures, technical awards and publications.

These students have demonstrated research capability in disciplines critical to the semiconductor industry. SRC Student Relations facilitates the transition of these relevantly educated and diverse students into careers with SRC Member companies and the research community by sponsoring student/industry networking events around the country and providing access to more than 800 student resumes through SRC's secure website. Between 2000 and 2009, 59% of graduating students took their first job within the SRC community or continued to a higher degree. Our alumni have become industry leaders and renowned faculty researchers.

IMPACT: EDUCATION

A new discovery. Pioneering ideas. Game-changing breakthroughs. Although a company or university might hold claim to a specific invention, innovation begins in the mind of individuals. And to SRC, there is no mind more vital to our future than that of a student.

SRC has made an impact on thousands of students through its investments in university research. The unique collaborative approach of SRC enables universities to work closely with industry and government sponsors on pre-competitive research – research that engages the vibrant minds of students who ultimately become tomorrow's technology leaders. Connecting academia and industry is the pathway not only to exponential technological progress, but also to meaningful careers for the students. They acquire industry-relevant research experience…and the scientific and engineering workforce gets a pool of the best and brightest in the field.

SRC students receive more than just a degree; they acquire an enhanced education. As part of the leading research teams at top universities, our students experience real-world applications of science and engineering principles. In addition to be being mentored by industry scientists and engineers, SRC students have access to myriad interactions beyond the classroom and lab, including an annual technical conference, networking events, e-workshops, contract reviews and more.

In addition to impacting and supporting graduate students, SRC is expanding support for undergraduate students through its Undergraduate Research Opportunities (URO) program. The URO program goal is to retain physical science and engineering students by providing hands-on research experience and mentoring, and to encourage them to apply to graduate school and pursue an advanced degree.

Long-lasting connections are forged among students, faculty and industry representatives working together on SRC research. And this unique bond remains the heart of SRC's success in sustaining U.S. leadership in the highly competitive semiconductor industry.

TECHCON 2010

TECHCON, SRC's annual technical conference, showcases the quality of the SRC research portfolio, the excellence of SRC students and faculty, and the magnitude of the collaborative research investment made by the semiconductor industry through SRC. The twelfth TECHCON was held September 13 and 14, 2010 in Austin, Texas.

Students presented both oral and poster presentations to allow the greatest dissemination of the research results and more interaction among participants. Sessions included papers from GRC, FCRP and NRI, with 144 student-presented technical papers and posters representing a broad cross-section of SRC-funded research. Fifteen students from GRC, one from FCRP and one from NRI won Best in Session Awards. Representatives from member companies served as judges, using a standard set of criteria and considering both paper presentation and poster.

Total attendance reached 437, including 184 industry participants, three government participants, 12 faculty, 210 students and 28 others, making for outstanding networking and technical exchange. Industry and faculty attendees included about 40 SRC student alumni. Thirty of these SRC alums provided insight into the future of the SRC Alumni Association at the first TECHCON Alumni Lunch.

Fifteen Fellows and Scholars presented posters in the TechFair sessions following each of the paper sessions. A new and exciting addition to TECHCON was a section of posters from 29 students participating in the Undergraduate Research Opportunities (URO) program. Many of these undergraduates were participating in their first major technical conference.

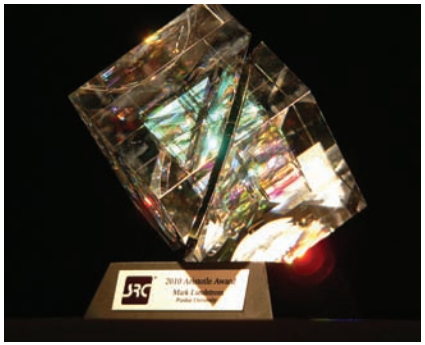
Invited speakers from industry and academia highlighted some of the opportunities that lie ahead for the semiconductor industry. Dr. Michael Mayberry, VP Technology and Manufacturing Group, Intel, delivered the keynote address entitled "A Look Forward". Professor Rob Rutenbar, FCRP researcher from the University of Illinois/Urbana-Champaign, opened the New Frontiers Session with his presentation entitled "Using the Mathematics of Money to Understand the Statistics of Nanoscale Circuits". Dr. Charles Holland, Deputy Director, Transformational Convergent Techniques Office, and Program Manager, High Productivity Computing Systems, DARPA, concluded this session with his presentation, "Sustaining High Performance Computing".

17 students won Best in Session Awards at TECHON 2010

AWARDS

ARISTOTLE AWARD

TECHCON also provides a forum for recognizing excellence in the SRC research community. The Aristotle Award recognizes excellence in teaching through the research process, as well as an exceptional commitment to students. Professor Mark Lundstrom's nomination for the Aristotle Award was submitted by an Industry Liaison who recognized the quality of students coming from his research at Purdue University. As the founder and director of the Network for Computational Nanotechnology, Professor Lundstrom was noted as being uniquely positioned to provide students with opportunities for scientific leadership, high impact and visibility.



2010 Aristotle Award was presented to Mark Lundstrom, Purdue University

TECHNICAL EXCELLENCE AWARD

The Technical Excellence Award recognizes researchers who have made key contributions to technology that have significantly enhanced the productivity of the semiconductor industry. This year, the $5,000 award was presented to Professor Li-C Wang and his team at the University of California/Santa Barbara, for their work in "Data Mining and Learning for Test and Validation". Professor Wang was an SRC-supported student at the University of Texas/Austin, an Industry Liaison while at Motorola, and is now an SRC-supported investigator in the areas of test and verification.

Professor Li-C Wang (center), University of California/Santa Barbara, 2010 Technical Excellence Award winner with Larry Sumney (left), SRC President & CEO and Dr. Tze-Chiang Chen (right), IBM, 2010 SRC Board of Directors Chairman

INDUSTRY LIAISON PROGRAM

The Industry Liaison Program captures the essence of SRC. It brings together faculty researchers, graduate students and technical experts from SRC Member companies and provides for interactions that benefit each. Industry Liaisons provide input and feedback to the researchers during the course of the project, act as mentors to students, and facilitate technology transfer back to the Member companies.

The Mahboob Khan Outstanding Industry Liaison Award, named in memory of a long-time mentor and advocate for the Industry Liaison program from Advanced Micro Devices, is presented to those individuals who have made significant contributions to the GRC community in their roles as Industry Liaisons. Sixteen individuals were recognized for their extraordinary commitment to the program.

2010 Office of the Chief Executive & Board of Directors

LARRY W. SUMNEY
President &
Chief Executive Officer

BETSY WEITZMAN
Executive Vice President,
SRC & Executive Director FCRP

STEVEN HILLENIUS
Executive Vice President,
SRC & Executive Director GRC

Board of Directors

[T.C. Chen (2010 Chairman)] IBM Corporation

[Chekib Akrout] Advanced Micro Devices, Inc.

[Sami Issa] Advanced Technology Investment Company

[Hans Stork] Applied Materials, Inc.

[Ken Hansen] Freescale Semiconductor, Inc.

[Gregg Bartlett] GLOBALFOUNDRIES

[Michael Mayberry] Intel Corporation

[Walden C. Rhines] Mentor Graphics Corporation

[Wilbert van den Hoek] Novellus Systems, Inc.

[Larry W. Sumney] Semiconductor Research Corporation

[Venu Menon] Texas Instruments Inc.

[Masayuki Tomoyasu] Tokyo Electron Limited (TEL)

EX-OFFICIO:
[Dan Armbrust] SEMATECH

NON-VOTING MEMBER:
[Brian Toohey] SIA

Board Secretary

[W. Clark McFadden II] Dewey & LeBoeuf, LLP

SRC Membership

[ABB, Inc.] ERI

[Advanced Micro Devices, Inc.] GRC, FCRP, NRI

[Advanced Technology Investment Company (ATIC)] GRC

[Applied Materials, Inc.] GRC, FCRP, ERI

[ExxonMobil Corporation] NINE

[First Solar, Inc.] ERI

[Freescale Semiconductor, Inc.] GRC, FCRP

[GLOBALFOUNDRIES] GRC, FCRP, NRI

[Goodyear] NINE

[IBM Corporation] GRC, FCRP, NRI, ERI

[Intel Corporation] GRC, FCRP, NRI, NINE

[Mentor Graphics Corporation] GRC

[Micron Technology, Inc.] FCRP, NRI

[Nexans] ERI

[Novellus Systems, Inc.] GRC, FCRP

[Raytheon Company] FCRP

[Robert Bosch, LLC] ERI

[Rohm and Haas Electronic Materials, an affiliate of Dow Electronic Materials] GRC

[Texas Instruments, Inc.] GRC, FCRP, NRI

[The MITRE Corporation] GRC

[Tokyo Electron Limited (TEL)] GRC, ERI

[United Technologies Corporation] FCRP

[Xilinx, Inc.] FCRP

Government Participation

[DARPA] FCRP

[NIST] GRC, NRI

[NSF] GRC, NRI

[Oregon Nanoscience & Microtechnologies Institute] NRI

[Project Future – South Bend, Indiana] NRI

[Sandia National Labs] NINE

[SPAWAR Systems Center] FCRP

[State of Arizona] GRC

[State of California] NRI

[State of Georgia] GRC

[State of Indiana] NRI

[State of New York] GRC, NRI

[State of Texas] GRC, NRI

[UK Engineering & Physical Sciences Research Council] GRC

Strategic Partners

[SEMATECH] GRC

[SEMI] GRC, FCRP

[SIA] GRC, FCRP, NRI

1101 Slater Road
Brighton Hall, Suite 120
Durham, North Carolina 27703

PO Box 12053
RTP, North Carolina 27709-2053
919.941.9400

Visit **Semiconductor Research Corporation** online at **www.src.org**.