Research Challenges in CAD and Test
Semiconductor Research Corporation
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The Computer-Aided Design and Test thrust at the Semiconductor Research Corporation is soliciting university proposals mainly in system, logic, and physical design tools to address the challenges below. Some additional work in Verification and Test will be considered, if aligned with the listed needs (which have been abbreviated and limited in scope in this solicitation cycle). These challenges have been developed by experts in SRC member companies and they have indicated that machine learning techniques, applied to the challenges, are of keen interest. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

SRC seeks university research which is pre-competitive, and promotes interaction between faculty and industry to address challenges that members see in future systems and technologies. Unfortunately, only a very small number of proposals will be selected for funding.

Be sure to follow the instructions in the Request for Research when responding.

Note: the following needs are not listed in an organized priority ordering .

System, Logic, and Physical Design Tools

S1 Tools for Design Robustness

S1.1 Electrically aware design rules and models, including extraction and modeling of manufacturability requirements specific to design needs, design rules for specific design / performance targets, etc.

S1.2 Techniques to synthesize library cells and designs to circumvent and/or tolerate manufacturing defects and variability with limited power/performance penalty

S1.3 Design techniques that can reduce infant mortality and comprehend in-field degradation mechanisms to achieve graceful failure.

S1.4 Yield-aware and yield optimization tools including resolution enhancement techniques.

S1.5 Bounded IR drop and power EM closure including stimulus selection and automated fixing of failures in physical design database

S1.6 Tools and optimizations for accurate timing margins of analog, digital and mixed signal designs at functional and physical levels for automotive (high reliability & high yield) and low power designs. Tools to explore design techniques or strategies to reduce silicon to physical design gap.

S2 Analog Tools

S2.1 Tools for analog DFM that focus on critical devices (matched pairs, current mirrors, etc.) and minimize unaccounted exposure to random and systematic variations (e.g., layout dependent effects).

S2.2 Tools for modeling and automation of design of multiple passives (MEMS, inductors, capacitors) as well as sensors.

S2.3 Advanced simulation tools for analog design including sensitivity to latent and hard defects or aging effects.

S2.4 Analog synthesis and optimization, taking into account designer intent

S2.5 Tools for verification and design of SoCs containing analog, digital and mixed signal.

S3 System Tools: Key Design Goals – Power Efficient High-performance Designs, Long Term Reliability

S3.1 Tools for system-level tradeoff analysis and design. This includes, but not limited to:

- Exploring different techniques for a system level design that functions across broad range of performance.
- Tools and methodologies to address reliability and robustness for power efficient high-performance designs.
- Techniques to evaluate and implement adaptive self-test design methods for use at the time of manufacture as well as in-field, to aid in diagnosis, isolation, and repair.

S3.2 Planning, exploration, and design tools for homogeneous/heterogeneous multi-core systems, including innovative and efficient communication fabrics, clock distribution, etc.

S3.3 Advanced logic/physical/high-level synthesis and cross-boundary optimization. Cross-level optimization tools that can consider learning from physical level and propagate up to system level design. This topic includes, but is not limited to • 3D design flow tools and trade-off analyses including synthesis, floor-planning, placement, power delivery, clock-tree synthesis, routing, DFT, thermal analysis, etc. • Predicting the electrical performance impact of mechanical stress
S3.4 Exploration of multiple layers of security during system level design

Test
T1 Test of Machine Learning Systems
T1.1 HW and SW methods to evaluate correctness of on- and off-line learning to ensure continued acceptable performance for learning/prediction during real-time application in the field.
T1.2 Data sets for test and validation of learning system before deployment.
T1.3 Metrics for correctness and acceptably correct inference.

Verification
V1 Verification of Machine Learning Systems
V1.1 Security and Emerging Applications of Formal Methods
V1.2 Advances in techniques to boost the scalability of core verification of ML-oriented and secure hardware, both for falsification and proofs.
V1.3 Learning algorithms for specification and verification of digital and AMS systems
V1.4 Learning algorithms targeted at fast functional verification coverage closure