Analog/Mixed-Signal Circuits, Systems and Devices + TxACE
Research Needs: AMS-CSD + TxACE
June 2019

The Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) program member companies are pleased to release this document that describes the research needs in the research program of Analog/Mixed-Signal Circuits, Systems and Devices including that for Texas Analog Center of Excellence (TxACE). Incorporated into this document are the SRC GRC Executive Technical Advisory Board (ETAB) priorities, the Analog/Mixed-Signal Circuits, Systems and Devices TAB (AMS_CSD) strategic planning process, and TxACE joint discussions.

The Analog/Mixed-Signal Circuits, Systems and Devices design research needs of the members are described in six major categories:

- Circuit Power/Energy Management/Optimization
- Robust, Reliable, and Functionally Safe Circuit Design
- High Performance Circuits
- Circuits in Advanced and Emerging Technologies
- Bridging Research Across Disciplines
- Circuit Design for Emerging Applications

Each of these major categories are broken down into several sub-categories which describe the need in more detail and are written to be broad in nature so as not to restrict the investigator's approach.

Another classification of research needs is also presented which highlights the member's interest in a different way:

- Power Management Circuits
- Mm-Wave Circuit
- Energy Harvesting Circuits
- Analog Signal Processing Circuits and Algorithms for Machine Learning Applications
- AMS Devices and AMS Compact Models
- High Performance Clocking
- Wireline Communication
- Wireless Communications
- Low Power Data Conversion
- Sensors and Information Extraction for Ubiquitous Data Collection/Transmission
- High Voltage and High Power Circuit Design (e.g. motor drive, automotive, LED, etc.)
- Analog/Mixed-signal Circuits for Information Fusion for Autonomous Vehicles (emphasized more elsewhere)

The needs in the AMS-CSD design space cover a broad range of applications, including, but not limited to, high performance processors for data centers, low power processors for mobile computing and communication, healthcare devices, and efficient energy usage and management systems. Investigators are encouraged to link the results of their work with a potential application to help describe the relevance of the proposed work.

This needs document is driving the AMS-CSD solicitation. It is issued to universities worldwide, may be addressed by an individual investigator or a research team. Our selection process is divided into two stages. The interested party is requested to submit a brief 1-page white paper. The white paper should clearly identify what can be done in three years. A successfully selected white paper will result in an invitation to submit a full proposal. These proposals will be further down-selected for research contracts. The number and size of the contracts awarded will be determined by the amount of available funds, and by the number of high-quality proposals.

Investigators who are funded will be expected to publish at top-tier conferences, including but not limited to ISSCC, VLSI, RFIC, ESSCIRC, ASSCC, BCTM, CSICS and CICC. White Papers for all the categories below will be considered for funding. Note that there is no priority assigned to the order of the major categories or the sub categories. Investigators are limited to participation in two white papers in this AMS-CSD solicitation. Submissions should highlight which needs are addressed, such as "C2.1".

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2019 AMS-CSD Needs Categories

C1	Circuit Power/Energy Management/Optimization

This section describes the needs of the members in the area of circuits and architectures for power, energy management, and efficiency improvements. The interest in circuits spans several orders of magnitude in power and energy. Challenges exist at all levels from data centers, racks, line cards, desktops, laptops, mobile processors all the way down to circuits in embedded microcontrollers consuming micro-Watts of active power with nano-amperes of leakage. Current novel circuits are desired for deeply scaled CMOS devices to improve the state of the art in both active and static current consumption along with management of thermal limitations and for early design space exploration into analog signal processing, wireline and wireless communication systems. On the other end of the power spectrum in the ultra-low powered battery and ultra capacitor driven or energy harvesting application space, challenges remain in key areas such as power/performance scalable analog (ADC's, DAC's, voltage comparators, etc). An example would be an analog to digital converter capable of variable precision conversion with power scaling with the conversion precision. Crystal oscillators and oscillator interfaces needed for accurate time references consume much of the standby power for ULP devices that must wake up on specific time intervals to communicate with mesh networks or perform specific tasks on a schedule. ULP low ppm drift time or frequency references are needed. Another key ULP need is for CMOS nano power current sensors for coulomb counting. Nano power current sensors would have many uses such as voltage regulator or voltage converter control or to monitor and/or allow control of current consumption.

C1.1	Energy efficient digital and analog circuits
C1.2	High efficiency integrated (e.g. SoC, SiP, 3D) circuits used for power management, including regulators, DC-DC converters, and new control architectures, such as the examples resonant, or SIMO, etc.
C1.3	Thermal management circuitry including high accuracy compact temperature sensors
C1.4	Control/management of leakage current
C1.5	Ultra-low power frequency or time sources (ppm drift rates suitable for real time clock applications)
C1.6	Nano-power current sensor for digital coulomb counting
C1.7	Power/performance scalable analog circuits for signal processing, wireless and wireline communication systems
C1.8	Fine-grain power management techniques such as state-retention, rapid on/off, etc.

C2	Robust, Reliable, and Functionally Safe Circuit Design

Robust circuit design means designs that meet requirements are insensitive to undesired process and environmental conditions; have high yields and are thoroughly testable. Reliable designs maintain this performance during the product's lifetime. Across the disciplines of analog, digital, RF and memory circuit design, the most traditional way to build robust circuits has been through overdesign; many designs are constructed to overachieve on the highest priority metrics (often speed) when process and environmental parameters are nominal, so that those metrics still meet the desired specs even when degraded by variation in those parameters. The cost of this overachievement is relaxation of lower priority metrics, usually power. Contrastingly, many commercial requirements are to meet minimum performance criteria over all conditions rather than to optimize performance in a narrower range of conditions. Functional Safety is the absence of unreasonable system risk due to hazards caused by malfunctioning behavior of Electrical/Electronic systems. This includes architectural features to detect and mitigate the effects of component failures, but not necessarily fail-operational or fault-tolerant characteristics.

Historically, steady improvement in the tradeoff between performance, area, and power has, however, slowed, while the desire for progress in function/power is as great as ever. At the same time, as supply voltages have become lower and geometries decrease, worst-case variability of device parameters has become more significant. In recent years, robustness has increasingly been achieved by making circuits tolerant to built-in and environmental effects without costly overachievement at nominal conditions. Continued innovation is needed in the design and architecture of these circuits. Member companies are seeking approaches that are robust under variations in global and local process parameters, device mismatches, hard or soft failure of individual components, and under the impact of environmental conditions such as supply and temperature, as well as noise and ESD. In addition, enhanced testability—analogous to IDDQ and scan testing for logic—is desirable for reliable analog and power circuits.

C2.1	Circuits for increased tolerance and adaptability to manufacturing/process variability including parameters with non-Gaussian distributions, such as those that are many deviations away from the mean (6+ sigma)
C2.2	Increasing reliability by design with unreliable components, soft errors and voltage “overstress”; testability including reliable BIST for analog circuits; long term reliability and odometers
C2.3	Noise tolerant (EMC) and aging tolerant circuits/isolation techniques, robust and low-capacitance ESD
C2.4	Systems and circuit techniques that incorporate functional safety features, including fault tolerance, fail-operational, diagnostics and monitoring of critical functions
C3	**High Performance Circuits**
In the "High-Performance Circuits" category high speed communications links and adaptive/high performance power efficient circuits continue to be important needs for members companies. For high-speed I/O, member companies seek a broad array of proposals for electrical and optical communication links. Extending bandwidth edge densities for electrical interconnects through high data rate links as well as pin-efficient signaling is of interest Important wireline components include power and area efficient circuits and systems operating at speeds beyond 50Gb/s, including drivers, equalizers, high-bandwidth amplification, and supporting clocking circuits. Techniques for optical interface circuits to support high data rate, power efficient silicon photonics and VCSEL-based links are desired. Another persistent need is high-density, power efficient (<1pJ/bit) I/O systems aimed at communicating over advanced interconnect materials and 3D stacks. *Scalable, area efficient, high-performance analog and RF circuits continue to be important with a need for configurable and modular architectures that enable reuse. Circuits and systems for emerging wireless applications focusing on higher frequency and/or higher data rate (>(>20Gb/s).* *Another ongoing need is for high-performance data converters. Techniques to improve resolution, dynamic range, sampling rates, and/or energy efficiencies for ADCs and DACs used in a variety of applications such as communication, IoT, and biomedical are appealing to member companies. High-performance, low-jitter clocking techniques including low-phase-noise PLLs as well as efficient multi-phase clock generation continue to be of interest for communication systems and other applications. Power and area-efficient digital techniques to enhance analog and RF circuits in highly-scaled technologies are still required. Where possible, supporting these high performance circuits in highly advanced technology nodes (sub-20nm) is desirable.*	
C3.1	Circuits and systems for high-speed electrical and optical communications links
C3.2	High-speed signaling/modulation schemes with improved spectral and/or pin efficiency
C3.3	High-speed short-distance wireless circuits at very low power
C3.4	High-dynamic-range and/or high-speed data conversion circuits and techniques for communication
C3.5	I/O supporting high data rate communication over high-density, advanced interconnects
C3.6	Power and area efficient, low jitter clock generation circuits for communication systems and other applications.
C3.7	Circuits and systems for high data rate wireless communication at distances up to 10m
C3.8	Digitally enhanced analog/RF circuits, PLLs, I/Os, and radios
C3.9	High-High performance data converters for applications including communication systems such as communications, IoT, and biomedical
C3.10	Automated synthesis, verification and validation methods for communication links, ADCs, DACs, and PLLs

C4	Circuits in Advanced and Emerging Technologies
This category highlights the need for circuit design in advanced and emerging process technologies - especially which enable aggressive process scaling into the sub-20nm range, system 3D integration, SOI techniques and the use of advanced CMOS structures. In the design of analog and RF circuits, emphasis should be placed on scalable designs that take best possible advantage of the capabilities of the process technology node and that easily transition to smaller technology node while achieving required performance and reliability levels and ensuring that area and power scale proportionally. This may involve using time or current as the signal processing quantity rather than voltage or charge and may also require the use of digital techniques, stacked devices, etc. to enhance the performance of the analog and RF. High bandwidth new volatile and non-volatile memory designs with similar requirements are also needed, required to sustain AI development while meeting the requirements of density, power, reliability, and scalability, along with ecosystem circuits that can leverage emerging memory technologies. Signal processing techniques and associated circuit designs that utilize emerging memory technologies are also desired. Finally, circuits that are based on compressed sampling techniques are also of interest.	
C4.1	Area and power efficient analog/RF/Clocking/IO designs that make best possible use of the capabilities of scaled "digital" technologies and that can continue to scale as the "digital" technology scales.
C4.2	Emerging memory design (volatile or nonvolatile) – high performance and power tradeoffs with high reliability and/or 3D scalability
C4.3	Variation tolerant and area efficient analog/mixed-signal circuits in low I head room CMOS processes (e.g. extreme scaled CMOS or high Vt ultra-low power)
C4.4	Low voltage digital and analog circuit optimized to operate in moderate and/or weak inversion regions and utilizing the best available (e.g. current or time) signal processing quantity.
C4.5	Circuit design techniques with advanced CMOS device structures (e.g. carbon nanotubes, spin torque devices, etc.)
C4.6	Reconfigurable Analog/RF design in processes with non-volatile memory bits/tunable devices
C4.7	Robust, low power interface circuits for 3D integration
C4.8	Test structures that target characterization of new sources of variability, (e.g. FinFET/FDSOI/Nanowire devices, emerging memory elements, III-V Integration and 3D, etc.) and associated models and CAD/simulation tools to go with them
C4.9	Low power logic and circuit design utilizing emerging nonvolatile RAM memory technology
C4.10	Silicon circuits based on quantum principles
C4.11	Low power scalable circuits using compressed sampling technology for application such as wireless sensors
C4.12	Hybrid analog digital information processing for artificial intelligence and machine learning circuits and techniques

C5	Bridging Research Across Disciplines

High performance passive components sensors and MEMs have become pivotal in analog and mixed-signal circuits. Sensors provide the initial first-hand information from the real world for subsequent processing. MEMS microphones and resonators have been successfully used in miniaturized SoC Integration of passives and/or sensors along with silicon components that can improve system performance to the next level while reducing overall cost and at the same time improving reliability is also of great interest.

Integrated circuits that include power devices have distinct needs: distributed and non-uniform thermal and Safe Operating Area (SoA) effects, electro migration, energy capability, testability, etc.. Furthermore, the use of novel wide bandgap materials in some applications and research that addresses those needs is also of interest.

Continued device scaling faces many issues: (1) increased susceptibility to layout dependent effects, signal and power-supply noise coupling, and noisy device behavior, (2) reliability issues such as electro migration, device wear out, and aging (e.g. oxide breakdown, NBTI, HCI), and (3) degraded performance (e.g. lower gain, increased noise, decreased matching, etc.) for analog devices, (4) strong temperature dependent effects due to the high localized heat dissipation. In summary, analog/mixed-signal design in deeply scaled technologies is fundamentally changing and solving these issues requires a cross disciplinary approach involving close cooperation between the design, CAD, test, modeling, and process development communities. Operating as isolated silos of expertise will no longer suffice to address the complexity and to find the necessary compromises that will be required in order to enable successful analog/mixed-signal circuit design in the underlying technologies.

C5.1	Semiconductor materials/processes/device and circuit design interactions/co-development, including novel non-CMOS devices, as well as extreme layout regularity
C5.2	Variation-aware device and interconnect modeling in advanced technologies
C5.3	Package and circuit interactions – high frequency, low noise, EMI management, power delivery, stress management and 3D IC heat & temperature management
C5.4	Improved digital and/or analog circuit design optimization and productivity through novel CAD techniques, including, but not limited to, utilizing data mining of process, test, and circuit analysis databases
C5.5	Widely applicable mixed-signal isolation technologies, structures, design rules, and methodology for SoC, SiP and 3D
C5.6	Variation-aware and scalable analog/RF/memory/mixed-signal BIST/DFT circuits
C5.7	Power device techniques including thermal and energy optimization, protection and diagnostic techniques for both the device and load
C5.8	Power devices and associated circuits based on wide bandgap materials such as GaN and SiC suitable for high speed and high power switching applications, its drive, control, reliability and compact modeling
C5.9	Analog CMOS improvement in nodes from 90nm and below: higher voltage, lower noise, higher working junction temperature, lower leakage and better CHC/NBTI/EM/etc. performance
C5.10	High performance SiGe HBT scaling beyond 500GHz (both ft and fmax)
C5.11	High performance capacitors and inductors/magnetics that can be monolithically integrated with a Si process
C5.12	Optical, magnetic, mechanical, MEMs and chemical sensors that can be integrated with a Si process
C5.13	Circuits and techniques for applications requiring compact high voltage galvanic isolation
C6	**Circuit Design for Emerging Applications**
With increased focus on 5G and automotive radar, AMS circuits for millimeter and sub millimeter wave operation and very wide bandwidth/frequency range are needed. Design methodologies in this area are as yet immature, thereby calling for radical new ideas to be developed. Some of these needs are driven by software defined radios and cognitive radios, multi-band multi-standard infrastructure, cellular, connectivity and sensor networks. Also, to enable IoT leaf nodes, there is a strong need to look at novel sampling approaches including sub-Nyquist and compressive sensing techniques. Similarly, circuit techniques are needed to further lower operating power and energy by efficiently exploiting low-bandwidth and low-duty cycle operation of sensors, potentially enabling operation by energy harvesting from temporally and spatially variable ambient sources. Circuits for persistent timekeeping to enable secure deployments are well-aligned in this category. Some of the emerging healthcare applications include wireless health monitors, circuits for patient-monitoring, temperature and other sensors, bio-marker sensing, circuits to enable disposable medical devices, etc. There is a need to look at low-power circuits for RF synchronization with hand shaking methods including wakeup radios and energy efficient wireless power transceivers including antenna structures. High voltage circuits needed for displays and motor control are also areas of significant research interest.	
C6.1	Low power and scalable non-Nyquist and other novel sampling techniques (e.g. compressive sensing)
C6.2	Wearable health monitors: Power efficient body sensor circuitry and/or dry skin contact sensing
C6.3	Efficient and affordable circuits for emerging lighting and display applications
C6.4	Energy efficient wireless power transmit and receive circuits, including the antenna
C6.5	Low power circuits for timing and control of sleep/wake sequences, persistent time-keeping, etc.
C6.6	Circuits for managing multiple energy sources that are not well behaved, such as from energy harvesting
C6.7	Energy Efficient Spectrum Sensing for cognitive radio applications
C6.8	Circuits for multi-band/multi-standard, including front-ends (infrastructure, cellular, connectivity or wireless sensor network)

C6.9	Low-power circuits and techniques for RF synchronization and hand shaking including wakeup radios
C6.10	Signal amplification near and beyond f_{max} for millimeter wave and sub millimeter wave applications
C6.11	Energy efficient motor control and driver circuits, power line communication and conversion.
C6.12	Circuits for millimeter and sub-millimeter applications such as IR imaging, communications, and radar
C6.13	Low power circuits and applications utilizing time-based processing