Research Needs: Packaging

June 10, 2019

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Background

Semiconductor-based computing and communication has revolutionized all aspects of modern life and will continue to play an influential role moving forward. Applications for small, flexible, light, easy-to-use interconnected consumer medical and industrial devices will continue to expand, while emerging technologies such as flexible/stretchable electronics, human body compatible electronics and nanotechnology require additional development for broad acceptance. In addition, there will be increasing packaging needs by devices that perform high performance computing (HPC). In order to support the semiconductor evolution, microelectronics packaging needs to progress along the following directions:

- Component scaling to enable system form-factor and density scaling.
- Power-efficient interconnects (wired, wireless and optical) to enable high bandwidth in 2-D/2.5-D/3-D architectures.
- Enhance thermal management solutions for the proliferation of 2-D/2.5-D/3-D architectures and to ensure consumer devices meet ergonomic constraints.
- Heterogeneous integration of digital, analog, radio frequency (RF), optical and discrete devices into high-performance, low-power, low-cost products of the future.
- Advance packaging for automotive applications with goal of zero defects and high reliability.
- Make progress in sensor packaging.

The Global Research Collaboration (GRC) division of SRC focuses on research in a timeframe 5 or more years ahead of technology release. This timeframe represents the “sweet spot” for pre-competitive, collaborative research, after which the industry focuses on proprietary development for technology differentiation by each company. Successful research proposals will need to match this timing.

This document is not intended to cover the complete landscape of the required research, but rather to identify the most critical areas in need of university research. We highlight key strategic challenges in five categories:

1. Interconnects
2. Power Delivery
3. Thermal Management
4. Metrology, Modeling, and Test
5. New Concepts

More details of each category can be found in the following sections, where the ordering is not intended to reflect the prioritization of a given research need.

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1. Interconnects

Packaging plays a critical role in enhancing system performance by enabling improved inter-component connectivity. High bandwidth is provided both by enabling low-loss interconnects and by increasing the number of inter-package (i.e. system level) and intra-package connections between components, in a cost-effective manner. There is a strong need to both develop new packaging architectures and to enhance current architectures (such as traditional organic and ceramic packaging, socket-able and surface mounted 2.5-D and 3-D architectures). Specific areas of interest include:

A. Heterogeneous integration of separately manufactured components into a higher-level SiP. Such components can be individual dies or packaged dies, MEMS devices, passives, sensors, light sources, detectors, etc. Low-cost and secure implementation is desirable.
B. Power-efficient, high-bandwidth density I/O. New packaging and system architectures (including electrical and optical interconnects) for improved package (per socket and overall system) bandwidth and I/O power efficiency. Specific targets are:
    - Data rate per line > 200 Gb/s; electrical interconnects should target a reach of > 100 mm and optical should target a reach of > 25 m.
    - Power efficiency better than 2 pJ/b for optical and better than 0.3 pJ/b for electrical (for parallel links up to 15mm and serial links up to 50mm).
C. As interconnects push for higher and higher speeds, design requires almost full isolation of these signals from one another to avoid interference. Thus even though higher per-lane signaling rates and overall bandwidth are achieved, they do not necessarily always improve bandwidth density. Research should target a linear bandwidth density > 10 Pb/s·m (at die edge).
D. Materials for sub-20 μm pitch vertical interconnects:
    - Current carrying capability > 1 x 10^5 A/cm^2.
    - Resistivity < 10 μΩ·cm.
    - Maximum joining temperature < 180°C (reduce delta between room temperature and melting point) to reduce stress and warpage in large devices.
E. Mechanical properties at least as good as tin-silver-copper (SAC) solder over a wide temperature window (-65°C to 150°C), i.e., modulus 20 – 60 GPa, CTE ~ 20 ppm/K, elongation > 35%, tensile strength > 55 MPa, shear strength > 30 MPa; creep, fatigue strengths, and fracture toughness (strain hardening exponents) at least equal to that of the SAC solders. Allows for seamless integration into existing interconnect manufacturing environment. Low-cost, non-planar, scalable interconnects for large format processing (300 – 500 μm pitch).

2. Power Delivery

Future power delivery applications are expected to require transient current densities of 5 – 10 A/mm^2 at 1 V or less. There is also a drive to smaller form factors so the power delivery solutions should fit within the footprints of either the package or the die, and have a small z-height. Specific areas of interest include:

A. New efficient power delivery for 2-D/2.5-D/3-D architectures.
B. Integration with lateral power field effect transistors (FETs): low parasitics (< 0.1 nH source inductance), high thermal dissipation (> 60 W/mm^2), enhanced reliability (10 V/μm E-field), and compact form factor.
C. Voltage regulator (VR) technologies that can support the high current densities with a relatively small footprint. The input voltage can range from 4 to 48 V and the output voltage can range from 0.3 to 1 V. The VR technology can be either two-stage or single-stage but the overall efficiency should be in the > 90% range.
D. High-efficiency, high-density inductors:
    - Magnetic materials with resistivity > 1 mΩ·cm, higher anisotropy fields while maintaining a high B_{sat} > 1 T, and that maintain permeability at frequencies up to 1 GHz.
    - Other novel materials.
E. High-density, low-impedance, and/or low-profile capacitors, with improved reliability.
F. Wireless power delivery environmentally friendly for consumer applications, targeting > 80% efficiency.
G. Concepts for low-cost, reliable, high-voltage packaging (> 1 kV).

3. Thermal Management

Reliable and affordable thermal management technology remains a major packaging challenge driven by the continuous drive towards miniaturization due to the explosion of mobile devices, and by the increase in compute density in data centers and servers. There is continued interest in new and improved thermal management techniques and metrologies to address hotspots, Joule heating and overall thermal design power (TDP) management in space constrained and/or high power and power density environments to ensure device performance and reliability. Specific areas of interest include:

A. Thermal management for packages (transient response, hot spots) – materials and substrate development, characterization, and reliability.
B. Materials development for thermal management (e.g., high thermal/electrical isolation of digital/analog components).
C. Low-cost thermal solutions for mobile and industrial converters, power supplies, etc.
D. Thermal management strategies for 3-D stacks, with two or more stacked dies that maintain junction temperatures T_j < 85°C for memory and T_j < 90°C for logic. The TDP envelope is intended to cover 2 W handhelds to 1000 W logic devices for high-performance computing with Ta <= 55°C.
E. Form factor restricted thermal solutions to meet both reliability and ergonomic requirements. Passive cooling of handheld systems is limited by heat rejection from the entire platform. Typical thermal solutions are expected to address both sustained and “burst” use conditions under both reliability and ergonomic requirements (e.g., skin temp < 40°C for up to 8 hours of power on).
F. Hot-spot metrology and low-cost mitigation schemes including novel materials to address hot spots at thermal densities > 500 W/cm^2.
G. Novel thermal management approaches for harsh environments such as automotive applications (meets or exceeds AEC-Q006 grade 0).

4. Metrology, Modeling, and Test

Metrologies, test, and simulation that enable fundamental understanding of package performance and reliability, help improve manufacturability, and are critical for packaging technology development and optimization. Particular research interests are:

A. Metrologies enabling fundamental understanding of package performance, reliability, and chip-package interaction effects.
B. High-resolution, non-destructive metrologies for failure analyses that are able to resolve defects (such as voids, delamination, bump, die, and interface delamination cracks) at a size scale of < 1 μm.
C. Metrologies that measure package in-situ surface roughness, surface energy and mechanical properties such as fracture toughness and coefficient of thermal expansion (CTE) in intricate spaces such as < 10 μm spaces between the neighboring interconnect bumps. Metrologies to measure surface energy and polarity with fine spatial resolution are desired. Ability to measure surface energy and polarity variation across a package surface area at a spatial resolution of 2 – 5 μm or better, and surface energy accurate to 1 – 2 dyn/cm, as a function of temperature (room temperature to 250°C) and humidity (30% to 60%), is desired. Mechanical properties should be measurable over a wider temperature range, -55°C – 250°C.
D. Chemical mapping: Metrology to detect organic and organo-metallic flux residues in intricate spaces such as < 10 μm spaces.
E. Interfacial adhesion: Metrology to measure adhesion strength of deeply buried interfaces across polymers-polymers, polymers-ceramics, and polymers-metals as a function of temperature and humidity ranges as described above. It is especially important to characterize adhesion at the small surface areas encountered in the sub-20 μm joints. Metrologies to measure adhesion strength of interfaces under cyclic loading.
F. Characterization of high-V and high-T materials (ionic conduction and polarization models).
G. High-frequency and high-temperature dielectric characterization of low-loss materials (encapsulants, mold compounds, substrates, etc.)
H. Predictive models for materials interface reliability.
I. Modeling and characterization tools for new and existing power-delivery architectures that enable co-design of the power-delivery network with circuit design.
J. Electromagnetic full-wave solvers for inhomogeneous, anisotropic lossy dielectrics and conductors, with algorithms optimized for both computation time and memory and approaching linear computational complexity.
K. Efficient and multi-physics performance, electromigration, and thermomechanical modeling.
L. Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation.
M. Packaging co-design with emphasis on enabling cost-effective, high-precision/accuracy testing (to ppb levels).
N. Multiple concurrent stress accelerated tests for more realistic use condition reliability prediction.
O. Validation methodologies and experimental techniques for material, component, and system characterization. Specific targets are:
    - Dielectric characterization up to 300 GHz and beyond. Scope includes anisotropic and inhomogeneous materials.
    - Surface roughness modeling with experimental validation up to 300 GHz.
    - Rigorous de-embedding for S-parameter measurements up to 300 GHz.

5. New Concepts

Revolutionary concepts are sought to enable the electronics industry to reach new levels of integration and address emerging applications in packaging. Specific areas of interest include:

A. Mechanically stretchable interconnects and flexible packaging for applications including wearable Internet of Things. Focus is on stretchable conductive materials/composites (as opposed to spring type structures where geometry enables stretching).
   - Interconnect conductivity should be as high as possible, with a target value range of 10,000 – 25,000 S/cm and a desired envelope target of 40,000 – 60,000 S/cm (~ 10x lower than that of Cu).
   - The cyclical stretching ability (i.e. no plastic/permanent deformation) should be as high as possible. Target at least 20% elastic stretch, with an envelope target of 30%.
   - Target materials to achieve a flexible interconnect bend radius of < 5 mm with < 1% drain current variation for attached CMOS die sizes < 2x2 mm^2.

B. Materials and interface challenges involved with low-cost, high-voltage, and high-power packaging: Concepts for minimal silicon-package interactions (e.g., charging properties, interface conductivity) in plastic packages under humid, high temperature, and high bias that can cause high-voltage device breakdown shift.

C. Polymeric encapsulants for 2-D/2.5-D/3-D architectures with < 20 μm pitch interconnects.
   - Effective thermal conductivity > 10 W/m·K.
   - Materials that allow for independent tailoring of CTE (5 – 20 ppm) and modulus (10 – 25 GPa).
   - Material viscosity that is tailorable to allow flow through < 10-μm gaps.
   - High adhesion strengths to silicon, metal and polymer interfaces (Si die, Cu bump, solder bump, and organic packages).
   - Glass transition temperatures > 150°C.
   - Fracture toughness (K_{1c} > 2 MPa·$m^{1/2}$).
   - Electrical insulation at < 10 μm length scales.
   - Breakdown field one order of magnitude higher than that in current polymer materials, which is only in the range 20 – 30 V/μm.

D. Material opportunities for printed circuit board (PCB) technology; high reliability (up to 100,000 hrs), high temperature (150 – 250°C), high voltage (> 100 V), high frequency, and high density.

E. Corrosion resistance through high temperatures up to 175°C for automotive and harsh environment applications.

F. New solders, under-bump metallurgies (UBMs), and alternatives to solder-based interconnects for enhanced electromigration and board level reliability performance.

G. Compact, low-cost ball grid array (BGA) form factor.

H. Integration of antenna arrays into packages for a bandwidth of 28 – 90 GHz.

I. Radical low-cost packaging for SiP.