Research Needs Document: Nanomanufacturing Materials and Processes

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Background

This document is prepared to accompany the Call-for-Research in the research program of Nanomanufacturing Materials and Processes (NMP). The research needs in this area are very broad. We present here selected areas of high priorities as identified by our sponsor members.

There is no doubt that nanomanufacturing is getting increasingly difficult. Feature sizes are already 10 nm or less in production; accordingly, research must be directed towards 5-nm or smaller dimensions. For lithography, EUV is in production yet sustainable patterning scaling requires continued research on various aspects of the technology. Metrology and defect detection are critical and their effectiveness must be improved in order to ensure that capable solutions exist in a timely and cost-effective manner. For unit processes, new materials are sought after for logic and memory devices. These material options must be paired with manufacturable deposition and patterning techniques. In addition, functional diversification calls for a wide range of other devices, such as required by analog applications and the Internet of Things. For interconnects, the reduced size (thickness, line width, vias) introduces-significant line, via, ad line-via resistance challenges aside increased reliability problems. Interlayer dielectrics also experience increasing difficulty in further reducing the dielectric constant. Manufacturing methods and process materials which reduce device and interconnect variability are required.

For an overview, we divide nanomanufacturing into five major groups:

(1) Patterning
(2) Front-end processes (FEP)
(3) Back-end processes (BEP)
(4) Common areas
(5) ESH (Environment, Safety, and Health)

It should be noted that the boundary between FEP and BEP is not clearly defined in the industry, due to the increasing kinds of devices fabricated between the semiconductor substrate and the first metal level. Here we simply put FEP as processes for devices of all kinds, including memories, passives, TFTs, sensors, etc., and BEP as those for interconnects and interlayer dielectrics.

Research Needs

The research needs for nanomanufacturing are obviously very wide. In this call, due to limited resources, we have identified what our members have considered to be the most critical items for university research. The list of topics within these five groups are shown as follows:

(1) Patterning

a. Resist, patterning, and mechanistic insight for EUV lithography with focus on:
    i. EUV mask defect control.
    ii. High numerical aperture (NA) resist concepts beyond chemically amplified resist
b. Directed self-assembly (DSA) advances for:
    i. defect improvement through material synthesis
    ii. multi-pitch using single block copolymer
    iii. implementing vertical orientation.
c. Self-aligned patterning processes.
d. Material informatics in lithography, e.g. modeling solvent/solute behavior during coating and gap filling
e. Etch-free feature patterning (i.e., guided or controlled deposition).
f. Pattern transfer, including new material combinations.

(2) Front-End Processes

a. Emerging materials for devices: Chemistry and synthesis (e.g., complex oxides, C-based, novel dielectrics/conductors; for transistors, memories, memory selection devices, etc.).
b. Interface/surface physics (SiGe, Ge, Ge-Sn, III/V, contacts, 1-D/2-D materials).

c. Hybrid materials with tunable properties.
d. Materials and processes enabling functional diversification on CMOS platform (RF and mm-wave devices, MEMS, sensors, photonics…).
e. Methods to create fluid transport in features that are <200nm in diameter and > 1 micron deep
f. Understanding and measuring the physical and chemical behavior of liquids in highly confined spaces, e.g. <20nm wide trenches
g. Gas phase, non-reactive ion based methods to selectively etch Si based materials (SiOCN, SiO2, Si3N4, Si) at temperatures below 300°C

(3) Back-End Processes

a. Novel ultra-low resistance interconnect materials and concepts
b. Low-k dielectrics and processing.
c. Interconnect contacts and interfaces with defect mitigation.

(4) Common areas

a. Atomic-layer deposition (ALD) and area-selective ALD
b. Atomic-layer etch (ALE)
c. Molecular Layer Deposition (MLD)
d. Novel/alternative area selective deposition techniques
e. Metrology and analytic techniques. 3-D imaging (3-D STEM, atom probe…) and functional imaging (STEM with EELS/EDS, high-resolution strain mapping...).
f. Modeling/understanding/detection/process control of critical unit processes:
    i. halogen diffusion mechanism and behavior in silicon
    ii. new sensors/techniques for improved process control
    iii. imperfections in epitaxial growth
    iv. defects formed in liquid solution
    v. Model-based approach that predicts the gap-filling behavior of spin-on materials within high aspect ratio (3-15) with particular interest allowed for statistical analysis
g. Fundamental material and process understandings including new analytical techniques to measure intrinsic parameters such as magnetism, spin, electronic states, and small (sub-5 nm) features.
h. Design for manufacturing (DFM).
i. 3-D monolithic heterogeneous integration.
j. AI and ML approaches to process control for yield improvement and/or manufacturing cost reduction (intra-process and inter-process)

For Category-5 (ESH), the Research Needs document can be obtained under a separate link in the call announcement.

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