Research Needs: Packaging

June 1, 2021

Semiconductor Research Corporation (SRC), Durham, NC 27703

Overview

Semiconductor-based computing and communication has revolutionized all aspects of modern life and will continue to play an influential role moving forward. Applications for small, flexible, light, easy-to-use interconnected consumer medical and industrial devices will continue to expand, while technologies such as flexible/stretchable electronics, human body compatible electronics, and nanotechnology that require additional development for broad acceptance, will continue to gain importance. In addition, there will continue to be increased requirements for packaging by devices that perform High Performance Computing (HPC) and communications, to support the performance roadmap. Today there is broad recognition that heterogeneous integration of diverse Intellectual Property (IP) blocks on the package, which serves as a compact, high-performance platform, is critical for the evolution of semiconductors. To support semiconductor evolution, microelectronics packaging needs to progress along the following directions:

- Component scaling to enable system form-factor and interconnect density scaling in heterogeneous packaging architectures.
- Power-efficient interconnects (wired, wireless, and optical) to enable high on-package and off-package bandwidth in 2-D/2.5-D/3-D architectures.
- Cost-effective, thermal management solutions for the proliferation of 2-D/2.5-D/3-D architectures and to ensure consumer devices meet ergonomic constraints.
- Heterogeneous integration of digital, analog, radio frequency (RF), optical and discrete devices into high-performance, low-power, low-cost products of the future.
- Advanced packaging for automotive applications with the goals of zero defects and high reliability.
- Sensor integration in packaging with improved form factor, energy efficiency and capabilities.
- Small form factor packages with improved high-voltage capability.
- Process engineering (including an understanding of in-process behavior through models, metrologies, and materials) to help develop scalable, cost effective, high-yielding manufacturing and test processes.
- Reliability engineering to ensure “reliable by design” configurations that meet the demands of diverse application environments including HPC, automotive, aerospace, and medical environments.

The Global Research Collaboration (GRC) division of SRC focuses on research in a timeframe five or more years ahead of technology release. Research on advanced tools and techniques such as modeling, simulation, and characterization can be of value with implementation timelines as low as one to two years post project completion. This timeframe represents the “sweet spot” for pre-competitive, collaborative research, after which the industry focuses on proprietary development for technology differentiation. Successful research proposals will need to match this timing.

Moving forward, the SRC is also embarking on an effort to broaden participation in its funded research programs. This aggressive agenda will help us drive meaningful change in advanced information and communication technologies that seem impossible today. In the programs we lead, we must increase the participation of women and under-represented minorities as well as strike a balance between U.S. citizens and those from other nations, creating an inclusive atmosphere that unlocks the talents inherent in all of us. Please visit https://www.src.org/about/broadening-participation/ for more information about the 2030 Broadening Pledge.

This document is not intended to cover the complete landscape of the required research, but rather to identify the most critical areas in need of university research. We highlight key strategic challenges in five categories:

1. Design Enablement and Tools
2. Interconnects and Architectures
3. Power Delivery, Thermal Management, and High-Speed Signaling
4. Metrology and Modeling
5. Materials

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More details of each category can be found in the following sections, where the ordering is not intended to reflect the prioritization of a given research need.

Contributing Members include:			
Arm	IBM	Intel	MediaTek
NXP	Samsung	Texas Instruments	Semiconductor Research Corporation

1. Design Enablement and Tools

Modeling and characterization tools for new and existing architectures that enable codesign and manufacturing of 2D, 2.5-D, and 3-D architectures.

- Electromagnetic full-wave solvers for inhomogeneous, anisotropic lossy dielectrics and conductors, with algorithms optimized for both computation time and memory and approaching linear computational complexity; electrical and optical frequency (wavelength) ranges should be covered.
- Design and characterization tools for optical and wireless interconnects.
- Component and system level simulation tools for thermal management and power delivery that fully accommodate steady state and transient conditions, comprehend dimensional and design complexity, and allow seamless integration with design layout tools.
- Simulation tools that allow for the complete thermomechanical description of packages during manufacturing (to help with yield projections), reliability, and use conditions for correct-by-design configuration development.
- Multiphysics based tools and algorithms to enable efficient co-optimization across multiple domains, e.g., thermals, power integrity, signal integrity, reliability, and manufacturability.
- Artificial intelligence (AI) and machine learning (ML) algorithms and tools for design and optimization.

Specific areas of interest include:

A. Heterogeneous integration of separately manufactured components into a higher-level System-in-Package (SiP). Such components can be individual dies, die stacks/subassemblies, or packaged dies/die stacks, micro-electromechanical system (MEMS) devices, passives, sensors, light sources, detectors, etc. Low-cost, high manufacturing yield, and secure implementation are desirable. Temperature, etc. should be constrained during integration to avoid altering device characteristic especially for those in advanced process nodes.
B. Compact, socketable, and ball grid array (BGA) form factor.
C. Integration of antenna arrays and metal interconnects into packages for a carrier frequency range of 28 – 3000 GHz, and a bandwidth of 28 – 500+ GHz at low loss, small bump pitch, low cost, high reliability, and high manufacturing yield.
D. Innovative, low-cost packaging for SiP.
E. Packaging co-design with emphasis on enabling cost-effective, high precision testing.
F. Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation.
G. Validation methodologies and experimental techniques for material, component, and system characterization. Specific targets are:
    - Dielectric characterization up to 500 GHz and beyond. Scope includes anisotropic and inhomogeneous materials.
    - Surface roughness modeling with experimental validation up to 500 GHz.
H. Rigorous de-embedding, including transitions, etc., for S-parameter measurements up to 500 GHz.
I. High-efficiency, high-density, cost-effective inductors:
    - Magnetic materials with resistivity > 1 mΩ·cm, higher anisotropy fields while maintaining a high

saturation magnetic flux B_{sat} > 1 T, and that maintain permeability at frequencies up to 1 GHz.
- Other novel materials.

J. High-density, low-impedance, and/or low-profile capacitors, with improved reliability.
K. Concepts for low-cost, reliable, high-voltage packaging (continuous operation over 2 kV and transient over voltages up to 15 kV).
L. Memory (SRAM, DRAM, NVM, etc.) is becoming an important big part for all edge applications, where systems need to be more and more tailored to use cases and integrated through custom packages.
M. Modeling and characterization tools for new and existing power-delivery architectures that enable co-design of the power-delivery network with circuit design.
N. High accuracy sensors and battery management.

2. Interconnects and Architectures

Packaging plays a critical role in enhancing system performance by providing improved inter-component connectivity. High bandwidth is enabled both by providing low-loss interconnects and by increasing the number of inter-package and intra-package connections between components, in a cost-effective manner. There is a strong need to both develop new packaging architectures and to enhance interconnect density of the current packaging architectures. Specific areas of interest include:

A. Power-efficient, high-bandwidth density I/O. New packaging and system architectures (including electrical, optical, and wireless interconnects) for improved package (per socket and overall system) bandwidth and I/O power efficiency. Specific targets are:
   - Refer to the IEEE EPS Roadmap (https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html) for interconnect density targets.
   - Data rate per line > 200 Gb/s; electrical interconnects should target a reach of > 100 mm and optical links should target a reach of > 25 m.
   - Power efficiency of the entire link including supporting circuits such as CDR, etc., should be better than 2 pJ/b for optical and better than 0.3 pJ/b for electrical (for parallel links up to 15 mm and serial links up to 50 mm).
   - Power consumption and data rate should be well scaled while minimizing the power/performance/cost overhead such that the power efficiency can be generally maintained across multiple use scenarios (e.g. at both high and low data rates).
B. As interconnects push for higher and higher speeds, design requires almost full isolation of these signals from one another to avoid interference. Thus, even though higher per-lane signaling rates and overall bandwidth are achieved, they do not necessarily always improve bandwidth density. Research should target a linear bandwidth density > 10 Pb/s·m (at die edge).
C. At THz frequencies and beyond, interfaces to the outside world are challenged by parasitic effects from traditional resistance, capacitance, and inductance to fringing, roughness, and index of refraction at multi-GHz frequencies. Research in understanding and minimizing these effects to help increase interconnect capability is of interest. Optical links with transceivers supporting high-order modulations such as 64/128+ APSK/QAM are of interest.
D. Cost-effective packaging technology including low-cost material/process, high precision in optical (sub)wavelength scale, and high manufacturing throughput, to support optical-electrical integration with high optical port counts in the order of hundreds to thousands.

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3. Power Delivery, Thermal Management, and High-Speed Signaling

Future power delivery applications are expected to require transient current densities of 5 – 10 A/mm^2 at 1 V or less. There is also a drive to smaller form factors so the power delivery solutions should fit within the footprints of either the package or the die and have a small z-height. Reliable and affordable thermal management technology remains a major packaging challenge driven by the continuous drive towards miniaturization due to the explosion of the number of mobile devices, and by the increase in compute density in data centers and servers. There is continued interest in new and improved thermal management techniques and metrologies to address hotspots, Joule heating and overall thermal design power (TDP) management in space constrained and/or high power and power density environments to ensure device performance and reliability. Specific areas of interest include:

A. New efficient power delivery for 2-D/2.5-D/3-D architectures.
B. Integration with lateral power field effect transistors (FETs): low parasitic (< 0.1 nH source inductance), high thermal dissipation (> 60 W/mm^2), enhanced reliability (10 V/µm E-field), and compact form factor.
C. Voltage regulator (VR) technologies that can support the high current densities with a relatively small footprint. The input voltage can range from 4 to 48 V and the output voltage can range from 0.3 to 1 V. The VR technology can be either two-stage or single-stage, but the overall efficiency should be in the > 90% range.
D. Embedded voltage regulators (eVR) including the inductors and capacitors that can be integrated on Logic dies with minimal cost overhead to the Logic wafers. Balls/pins and the metal interconnects inside and outside the package should have low resistance and electromigration to minimize the overall footprint.
E. Wireless power delivery environmentally friendly for consumer applications, targeting > 80% efficiency including loss from air links.
F. Thermal management for packages (transient response, hot spots) – materials and substrate development, characterization, and reliability.
G. Materials development for thermal management (e.g., high thermal conductivity/electrical isolation of digital/analog components).
H. Low-cost thermal solutions for mobile and industrial converters, power supplies, etc.
I. Thermal management strategies for 3-D stacks, with two or more stacked dies that maintain junction temperatures Tj < 85°C for memory and Tj < 90°C for logic. The Thermal Design Power (TDP) envelope is intended to cover 2 W per chip and 5W per handheld systems to 1,500 W logic devices for high-performance computing with ambient temperatures up to 55°C.
J. Form factor restricted thermal solutions to meet both reliability and ergonomic requirements. Passive cooling of handheld systems is limited by heat rejection from the entire platform. Typical thermal solutions are expected to address both sustained and “burst” use conditions under both reliability and ergonomic requirements (e.g., skin temperatures < 40°C for up to 8 hours of power on).
K. Novel thermal management approaches for harsh environments such as automotive applications (meets or exceeds standard AEC Grade 0 (Automotive Electronics Council)). Refer to:
http://www.aecouncil.com/Documents/AEC_Q100_Rev_H_Base_Document.pdf
http://www.aecouncil.com/Documents/AEC_Q006_Rev_A.pdf
L. Package-level integration utilizing heat sinks and air cooling is becoming limited by thermal constraints; while more exotic cooling solutions exist, these tend to be impractical in production environments due to the cost and support requirements. Alternative breakthrough solutions are needed.
M. Hot-spot metrology and low-cost mitigation schemes including novel materials to address steady state and transient hot spots at thermal densities > 500 W/cm^2.

4. Metrology and Modeling

Metrologies, test, and simulation that enable fundamental understanding of package performance and reliability, help improve manufacturability, and are critical for packaging technology development and optimization. Specific areas of interest include:

A. Metrologies enabling fundamental understanding of package thermal, mechanical, and electrical performance, degradation, reliability, and chip-package interaction effects.
B. High-resolution, non-destructive metrologies for failure analyses that are able to resolve defects (such as voids, delamination, bump, die, and interface delamination cracks) at a size scale of < 1 µm.
C. Metrologies that measure package in-situ surface roughness, surface energy and mechanical properties such as fracture toughness and coefficient of thermal expansion (CTE) in intricate spaces such as < 10 µm spaces between the neighboring interconnect bumps. Metrologies to measure surface energy and polarity with fine spatial resolution are desired. Ability to measure surface energy and polarity variation across a package surface area at a spatial resolution of 2 – 5 µm or better, and surface energy accurate to 1 – 2 dyn/cm, as a function of temperature (room temperature to 250°C) and humidity (30% to 60%), is desired. Mechanical properties should be measurable over a wider temperature range, -55°C – 250°C.
D. Chemical mapping: Metrology to detect organic and organo-metallic flux residues in intricate spaces such as < 10 µm in sizes.
E. Interfacial adhesion: Metrology to measure adhesion strength of deeply buried interfaces across polymers-polymers, polymers-ceramics, and polymers-metals (include organic and inorganic dielectrics) as a function of temperature and humidity ranges (AEC Grade 0 conditions). It is especially important to characterize adhesion at the small surface areas encountered in the sub-20 µm joints. Metrologies to measure adhesion strength of interfaces under cyclic loading.
F. Characterization of high-voltage and high-temperature materials (ionic conduction and polarization models).
G. High-frequency and high-temperature dielectric characterization of low-loss materials (encapsulants, mold compounds, substrates, etc.).
H. Non-invasive, quick-turn metrologies for thermal mapping and characterization of 3D stacks.
I. Quick-turn metrologies for repeatable and accurate characterization of thermal contact resistances in the range of 0.001 – 0.01°C·cm^2/W.
J. Multiple concurrent stress accelerated tests for more realistic use condition reliability prediction.
K. Predictive models for materials interface reliability.
L. Efficient and multi-physics performance, electromigration, and thermomechanical modeling.
O. Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation.
P. Multiple concurrent stress accelerated tests for more realistic use condition reliability predictions.
Q. Validation methodologies and experimental techniques for material, component, and system characterization. Specific targets are:
    - Dielectric characterization up to 500 GHz and beyond. Scope includes anisotropic and inhomogeneous materials.
    - Surface roughness modeling with experimental validation up to 500 GHz.
R. Rigorous de-embedding, including transitions, etc., for S-parameter measurements up to 500 GHz.

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5. Materials

Interconnect mechanical properties at least as good as tin-silver-copper (SAC) solder over a wide temperature window, harsh environments, and individual parameters at least equal to that of the SAC solders. Package materials suitable for automotive and harsh environments, flexible applications, and medical applications. Specific areas of interest include:

A. Materials and interface challenges involved with low-cost, high-voltage, and high-power packaging: Concepts for minimal silicon-package interactions (e.g., charging properties, interface conductivity) in plastic packages under humid, high temperature, and high bias that can cause high-voltage device breakdown shift.

B. Polymeric encapsulants for 2-D/2.5-D/3-D architectures with < 20 µm pitch interconnects.
   - Effective thermal conductivity > 10 W/m·K.
   - Materials that allow for independent tailoring of CTE (5 – 20 ppm) and modulus (10 – 25 GPa).
   - Material viscosity that is tailorable to allow flow through < 10 µm gaps.
   - High adhesion strengths to semiconductor, dielectric, metal, and polymer interfaces (Si die, Cu bump, solder bump, and organic packages).
   - Glass transition temperatures > 150°C.
   - Fracture toughness (K_{1c} > 2 MPa·$m^{1/2}$).
   - Electrical insulation at < 10 µm length scales.
   - Breakdown field one order of magnitude higher than that in current polymer materials, which is only in the range 20 – 30 V/µm.

C. New solders, under-bump metallurgies (UBMs), and alternatives to solder-based interconnects for enhanced electromigration and board level reliability performance.

D. Mechanical properties at least as good as tin-silver-copper (SAC) solder over a wide temperature window (-65 to 150°C), i.e., modulus 20 – 60 GPa, CTE ~ 20 ppm/K, elongation > 35%, tensile strength > 55 MPa, shear strength > 30 MPa; creep, fatigue strengths, and fracture toughness (strain hardening exponents) at least equal to that of the SAC solders. Allows for seamless integration into existing interconnect manufacturing environment. Low-cost, non-planar, scalable interconnects for large format processing (300 – 500 µm pitch).

E. Mechanically stretchable interconnects and flexible packaging for applications including wearable Internet of Things (IoT). Focus is on stretchable conductive materials/composites (as opposed to spring type structures where geometry enables stretching).
   - Interconnect conductivity should be as high as possible, with a target value range of 10,000 – 25,000 S/cm and a desired envelope target of 40,000 – 60,000 S/cm (about 10x lower than that of Cu).
   - The cyclical stretching ability (i.e. no plastic/permanent deformation) should be as high as possible. Target at least 20% elastic stretch, with an envelope target of 30%.
   - Target materials to achieve a flexible interconnect bend radius of < 5 mm with < 1% drain current variation for attached die sizes < 2 x 2 mm^2.

F. Solders with peak reflow temperature < 140°C for decreased stress between joined components.

G. Material opportunities for printed circuit board (PCB) technology; high reliability (up to 100,000 hours), high temperature (150 – 250°C), high voltage (> 100 V), high frequency, and high density.

H. Corrosion resistance through high temperatures up to 175°C for automotive and harsh environments.

I. Package process compatible corrosion resistant coating/materials to prevent or mitigate (e.g., Cu wirebond) corrosion by ions such as Cl^-.

E. Materials for sub-20 µm pitch vertical interconnects:
   - Current carrying capability > 1 x 10^5 A/cm^2.
   - Resistivity < 10 µΩ·cm.
   - Maximum joining temperature < 180°C (reduce delta between room temperature and melting point) to reduce stress and warpage.

J. Packaging materials for advanced chips integration such as GaN/SiC.

K. Packaging materials for high temperature automotive applications capable for AEC Grade 0 and beyond, ambient temperature of 180°C and Tj of 200°C.
L. Materials research for better compatibility with extreme or non-standard environments such as immersion cooling, high radiation (e.g. space, disaster recovery), and chemically harsh (e.g. space, IoT edge devices).