Research Needs: Analog/Mixed-Signal Circuits, Systems, and Devices (AMS-CSD) + TxACE

June 1, 2022

Semiconductor Research Corporation (SRC), Durham, NC 27703

The Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) program member companies are pleased to release this document that describes the research needs in the research program of Analog/Mixed-Signal Circuits, Systems and Devices including that for Texas Analog Center of Excellence (TxACE). The principal goal of this program is to create fundamental innovations in analog/mixed-signal integrated circuits and systems across a broad range of applications, including traditional information processing as well as newer areas of emphasis—such as automotive, industrial, and medical.

The Analog/Mixed-Signal Circuits, Systems and Devices design research needs of the members are described in eleven major categories below

1. Power Delivery and Management
2. Wireline Communications
3. Mm-wave and THz Circuits and Systems
4. Wireless Communications
5. Data Conversion
6. Sensors and Information Extraction for Ubiquitous Data Collection/Transmission
7. AMS Device Models and System Models
8. Clocking
9. Efficient Circuits
10. Reliable and Functionally Safe Circuit Design
11. Analog Design Productivity and Automation

Each of these major categories are broken down into several sub-categories which describe the need in more detail and are written to be broad in nature so as not to restrict the investigator's approach.

The needs in the AMS-CSD design space cover a broad range of applications, including, but not limited to, high performance processors for data centers, low power processors for mobile computing and communication, healthcare devices, and efficient energy usage and management systems. Investigators are encouraged to link the results of their work with a potential application to help describe the relevance of the proposed work.

This needs document is driving the AMS-CSD solicitation. It is issued to universities worldwide, may be addressed by an individual investigator or a research team. Our selection process is divided into two stages. The interested party is requested to submit a brief 1-page white paper. The white paper should clearly identify what can be done in three years. A successfully selected white paper will result in an invitation to submit a full proposal. These proposals will be further down selected for research contracts. The number and size of the contracts awarded will be determined by the amount of available funds, and by the number of high-quality proposals.

SRC has also released a document called the Decadal Plan for Semiconductors (www.src.org/about/decadal-plan/) which describes five "Seismic Shifts" facing the electronics industry in the coming decade. Research should address issues arising from one of them:

- Smart Sensing – The Analog Data Deluge
- Memory & Storage – The Growth of Memory and Storage Demands
- Communication – Communication Capacity vs. Data Generation
- Security – ICT Security Challenges
- Energy Efficient – Compute Energy vs. Global Energy Production

While a particular research submission might address the challenges of multiple shifts, each investigator should choose one which best aligns to their effort, perhaps at the end application level.

Moving forward, the SRC is also embarking on an effort to broaden participation in its funded research programs. This aggressive agenda will help us drive meaningful change in advanced information and communication technologies that seem impossible today. In the programs we lead, we must increase the participation of women and under-represented minorities as well as strike a balance between U.S. citizens and those from other nations, creating an inclusive atmosphere that unlocks the talents inherent in all of us. Please visit, https://www.src.org/about/broadening-participation/, for more information about the 2030 Broadening Pledge.

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Investigators who are funded will be expected to publish at top-tier conferences, including but not limited to ISSCC, VLSI, RFIC, ESSCIRC, ASSCC, BCTM, CSICS and CICC. White Papers for all the categories below will be considered for funding. Note that there is no priority assigned to the order of the major categories or the subcategories. Investigators are limited to participation in two white papers in this AMS-CSD solicitation. Submissions should highlight which needs are addressed, such as "2.1".

CONTRIBUTORS

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1	**Power Delivery and Management**
This section describes the needs of the members in the area of circuits and architectures for power delivery, energy management, and conversion efficiency improvements. The interest in circuits spans many orders of magnitude in power and energy. Challenges exist at all levels from data centers (kW), racks, line cards, desktops, laptops, mobile processors down to circuits in embedded microcontrollers consuming microwatts of active power with nanoamperes of leakage. *Power delivery performance challenges increase at advanced nodes, needing improved accuracy, transient response, reliability, and fault tolerance.*	
1.1	High efficiency integrated (e.g. SoC, SiP, 3D) circuits used for power delivery, including regulators, DC-DC converters, and new control architectures, including resonant, SIMO or hybrid techniques improving transient response, efficiency and robustness. Technologies for cost-effective integration of passives
1.2	Integrated Isolated or non-isolated Gate Drivers**:** In-package integration of isolated communications and power transfer for safe isolation and control of HV circuits, including powerline, HV Electric Vehicle and BMS applications
1.3	High efficiency power management integrated circuits, including regulators, DC-DC converters, new control architectures, and thermal resistance co-design techniques for minimal Ti rise
1.4	New control architectures, including improving transient response, droop monitoring, droop mitigation and control robustness and adaptive circuits
1.5	Electromagnetic Compatibility: Development of new circuit techniques or algorithms to reduce emissions produced by the switching regulators. Low noise (1/f and thermal) controllers
1.6	High Voltage Power (0.2 – 1 kV): Novel power distribution systems, topologies, and controllers that leverage GaN/SiC improved switching performance. Monolithic GaN/SiC power stages/circuits
1.7	High conversion ratio DCDC converters(step-up and -down)~~:~~ novel topologies, novel packaging and magnetic/circuit co-optimization for high power density, high efficiency converters
1.8	Robust and reliable power delivery systems including predictive reliability and ageing or imminent failure detection, and fault tolerance
1.9	Fine-grain power delivery techniques such as state-retention, rapid on/off, phase shedding, limited di/dt rates etc
1.10	High efficiency 48V to 1.8V or less voltage conversion (10A – 600A scalable) circuit solutions for silicon ICs
1.11	Voltage regulation circuits for AMS designs with focus on improved power efficiency, performance, and modularity. Including efficient small-footprint modular low dropout regulators that can current-share without impacting stability

2	**Wireline Communications**
In this category, member companies seek a broad array of proposals for electrical and optical communication links. Needs in the area of electrical serial links aim to improve communication bandwidth edge densities in processor and ASIC applications. Circuits, systems, and architectures for achieving this through improved spectral efficiency, as well as improved pin efficiency are desired. Important wireline components include power and area efficient circuits and systems operating at speeds beyond 100Gb/s, including drivers, equalizers, high-bandwidth linear amplifiers, and supporting low-jitter clocking circuits. Techniques for optical interface circuits to support high data rate, power-efficient silicon photonics, and VCSEL-based links are of interest. Another persistent need is high-density, power-efficient (<1pJ/bit) I/O systems aimed at communicating over advanced interconnect materials and 3D stacks. *Power efficiency is also an important requirement as well as bandwidth. This includes good power scaling with bandwidth for intermittent bursty traffic. ESD improvements are also needed to support higher electrical data rates and low power.*	
2.1	Electrical and optical serial transceivers, circuits and architectures to enable beyond 100Gb/s applications. Including designs that can integrate on silicon
2.2	Signaling and modulation techniques with improved spectral efficiency beyond NRZ and PAM4
2.3	Pin-efficient signaling for high-density interconnects. Including high bandwidth/low power dense/short range wireline interconnects for in-package applications
2.4	Digital signal processing techniques supporting ADC-based wireline links
2.5	Area and power efficient wireline IO designs that make best possible use of the capabilities of scaled “digital” technologies and that can continue to scale as the “digital” technology scales
2.6	Power improvements for wireline IO designs, to allow reduced pJ/b as well as better power scaling with bandwidth. Can include fast start/stop or state retention options for intermittent traffic
2.7	Improved system noise/channel modelling – to enable high speed wireline IO design with predictable silicon performance
2.8	Area efficient and low capacitance ESD for 3D and SiP solutions as well as traditional IO

3	**Mm-wave and THz Circuits and Systems**
Millimeter-wave 5G, WiFi and radar sensing are rapidly becoming omnipresent. Viability of 100s of Gbps and Long Range/Short Range sensing, imaging, and spectroscopy enabled at mmW frequencies has been proven in mainstream process technologies. *AMS architectures, circuits and novel use of devices (in existing mainstream processes) for sub-millimeter, millimeter-wave leading into sub-THz and THz operation providing efficient and/or wide bandwidth operation supporting the rapidly growing needs of fine-grain sensing, imaging and high data-rate communications are needed thereby calling for radical new ideas to be developed.*	
3.1	Established (e.g. 5G, radar) and emerging standards (e.g. V2X, future radar, 6G, xG) for existing and future applications addressing radar, sensing, imaging and high-speed, broadband communications covering. Innovations in any/all the following categories: a. Block/Module level innovations and techniques stretching energy efficiency and noise boundaries on Amplification and Signal frequency translation b. Circuit and system level architecture solutions that address the cost and form-factor constraints of handheld and mobile devices (as distinct from automotive) and support simultaneous communication and sensing c. Active and passive sensing for mobile/handheld to enable new models of device interaction d. Packaging innovation addressing heterogeneous integration, silicon to package transitions, low-loss signal conduits (transmission lines, waveguides) and antenna(e)/launch(es), photonics integration
3.2	Innovative architecture, circuits, devices, and packaging including hybrid electronic circuits and silicon photonics architectures addressing sub-THz (<300GHz), THz (0.3-30THz), and Optical Wireless and/or guided medium communications, sensing, imaging, and spectroscopy
3.3	Integrated and/or stand-alone millimeter/sub-THz Micro Electromechanical Structures (MEMS) addressing filtering, duplexing, interference cancelation, resonator and sensing needs

4	Wireless Communications
Scalable, area-efficient, high-performance analog and RF circuits continue to be important with a need for configurable and modular architectures that enable reuse. Circuits and systems for emerging wireless applications focusing on higher frequency and/or higher data rate (>>30Gb/s). Power and area-efficient digital techniques to enhance analog and RF circuits in highly scaled technologies are required. Where possible, supporting these high-performance circuits in highly advanced technology nodes (sub-16nm) is desirable. In the design of analog and RF circuits, emphasis should be placed on scalable designs that take the best possible advantage of the capabilities of the process technology node and that easily transition to smaller technology nodes while achieving required performance and reliability levels and ensuring that area and power scale proportionally. This may involve using time or current as the signal processing quantity rather than voltage or charge and may also require the use of digital techniques, stacked devices, etc. to enhance the performance of the analog and RF. There is a need to look at low-power circuits for RF synchronization with hand shaking methods including wakeup radios and energy-efficient wireless power transceivers including antenna structures.	
4.1	High-speed short-distance (< 10m) wireless circuits at very low power
4.2	Low power scalable circuits using compressed sampling technology, feature extraction and other analog-to-information techniques for application such as wireless sensors
4.3	Long range (>>1km) sub-1GHz radios, ultra-low power and low data rate
4.4	Low power radios with more complex modulation (e.g. OFDM for 802.15.4g)
4.5	Circuits for fast startup and fast shut down (RF, oscillators, power management) for efficient duty-cycled radios
4.6	Low area, low power RF designs (examples are RF generation / amplification without inductors)
4.7	Higher output power PAs (>+20dBm) with advanced, low voltage technology nodes

5	Data Conversion
Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are fundamental and enabling building blocks for an extremely wide range of applications from energy metering to power management, to communications, to automotive radar, and beyond. As more and more signal processing is performed digitally, the performance, efficiency, and cost of the data converters become ever more critical. Thus, techniques to improve resolution, dynamic range, sampling rates, and/or energy efficiencies for ADCs and DACs are appealing to member companies. In addition, if the developed data converters can achieve improved performance and efficiency (i.e. Figure of Merit (FoM)) while still meeting all requirements for a specific application (e.g. including input/reference buffers, filtering, clock phase noise, yield/cost, etc.), then the research is even more appealing to member companies. *As process technologies scale from 28nm to 16nm to 5nm and beyond, ADC and DAC architectures that take the best possible advantage of the chosen process technology are also of very high interest to member companies. Using time as the signal processing variable in an ADC or using AI/machine learning to improve data converter performance are examples of this trend.*	
5.1	ADC architectures that are capable of variable precision conversion that also scale the power with the conversion precision
5.2	ADC architectures that take advantage of novel sampling approaches including sub-Nyquist and compressive sensing techniques
5.3	Time-based ADC architectures for high-speed (Gs/s) applications
5.4	Time-based ADC architectures for continuous-time sigma-delta ADCs
5.5	ADC/DAC architectures that employ AI/machine learning to improve performance in advanced process technologies (sub-16nm)
5.6	Ultra-wide bandwidth (>200MHz) continuous-time Sigma-Delta ADC architectures for radio/radar receiver applications
5.7	Highly efficient, high-dynamic range ADC and DAC architectures for sensor interface/Internet of Things (IoT) applications
5.8	High-speed (>>10 Gs/s), high-dynamic range (>8-bit) ADC/DAC architectures for 5G/6G radio and Digitally Modulated Radar (DMR) transmit/receive applications, etc.
5.9	ADC circuits and solutions for high-speed wireline Ultra-high Speed ADCs for wireline applications (>100Gs/s with 6-bit).

6	**Sensors and Information Extraction for Ubiquitous Data Collection/Transmission**

This section describes the needs of the members in the area of low cost, highly integrated smart sensors for data collection and transmission, especially in the ultra-low-power application space.

Circuit challenges are in different areas: low-power high-precision scalable analog (ADC's, DAC's, voltage comparators, etc), power-efficient and long-range wireless communications, nano-power accurate time references for RTC and wake-up functions as well as TX/RX.

Sensor challenges mostly reside in integrating high-performance sensors and MEMs with analog and mixed-signal circuits using standard CMOS process and measure or detect temperature, light, voltage, current, vibration, sound, magnetic field, electric field, gravity, acceleration, etc.

Sensors provide the initial first-hand information from the real world for subsequent processing, so improving sensors will also improve system performance and reliability while reducing overall cost. The major area of sensor development are in CMOS nano-power current sensors for coulomb counting; techniques to improve resolution, dynamic range, sampling rates, and/or energy efficiencies for ADCs and DACs used in a variety of applications such as communication, IoT, and biomedical; high-performance, low-jitter clocking techniques including low-phase-noise PLLs as well as efficient multi-phase clock generation continue for communication systems and other applications; power and area-efficient digital techniques to enhance analog and RF circuits in highly-scaled technologies. Where possible, supporting these high-performance circuits in highly advanced technology nodes (sub-20nm) is desirable to enable IoT leaf nodes.

6.1	Optical, magnetic, mechanical, MEMs and chemical sensors that can be integrated with a Si process
6.2	Low power scalable circuits using compressed sampling technology, feature extraction and other analog-to-information techniques, for application such as wireless sensors
6.3	Hybrid analog digital information processing for artificial intelligence and machine learning circuits and techniques. Including low area/power overhead machine learning techniques for remote sensors and in-situ sensors (should go to machine learning?)
6.4	Hybrid analog digital circuits and systems for PUF (physical unclonable function) with low area/power overhead (Hardware security? Why PUF only for remote sensors (i.e. RFID)?)
6.5	Wearable health monitors: Power efficient body sensor circuitry and/or dry skin contact sensing; also sensing circuits, devices, and systems on flexible materials
6.6	Efficient and affordable circuits for emerging lighting and display applications
6.7	Energy efficient wireless power transmit and receive circuits, including the antenna
6.8	Low power circuits for timing and control of sleep/wake sequences, persistent timekeeping, etc.
6.9	Circuits for managing multiple energy sources that are not well behaved, such as from energy harvesting (combined with power management?)
6.10	Energy Efficient Spectrum Sensing for cognitive radio applications
6.11	Circuits for multi-band/multi-standard, including frontends (infrastructure, cellular, connectivity or wireless sensor network)
6.12	Low-power circuits and techniques for RF synchronization and hand shaking including wakeup
6.13	Circuits for millimeter and sub-millimeter applications such as IR imaging, communications, and radar
6.14	Low power circuits and applications utilizing time-based signal processing
6.15	Emerging sensors solutions including artificial intelligence or advanced device structures

7	**AMS Device Modelsand System Models**

This section describes the needs for improved modeling of analog circuits and devices. Key modeling challenges include better modeling and predictability between schematic and layout, better handling of variation effects inactive, passive, and parasitic elements. This includes modeling of system interconnect channels and environmental effects including both accidental and malicious environmental effects. ESD is also a priority area for better modeling including for advanced packaging cases beyond regular IC packages.

Analog circuits can also benefit from improvements in devices to support higher performance designs. This includes improvements in passive devices as active devices such as devices to support beyond 500GHz. Improved ESD protection

devices and solutions are also a priority to reduce area, power, and performance limitations for high performance and/or dense IO for 3D and system-in-package solutions.	
7.1	Compact ESD modeling improvements
7.2	IO/channel model correlation to silicon, including modeling of silicon, package, and interconnect. Including time-domain, frequency domain, and statistical analysis RTS noise, and flicker noise for non-quasi-static modeling
7.3	Improvements in modeling and prediction between pre-layout and post-layout performance. Also accurate modeling of device ageing and other parametric drifts in sub-22nm and below process technologies
7.4	Improved system noise/channel/power integrity modeling – to enable high speed IO design with predictable silicon performance
7.5	Area efficient and low capacitance ESD for 3D and SiP solutions as well as traditional IO
7.6	Variation-aware device and interconnect modeling in advanced technologies, including modeling variation of advanced interconnects. For example: extend Monte-Carlo simulations to include interconnect and supply
7.7	High performance capacitors and inductors/magnetics that can be monolithically integrated with a Si process or package
7.8	High performance SiGe HBT scaling beyond 500GHz (both ft and fmax)
7.9	Package and circuit interactions – high frequency, low noise, EMI management, power delivery, stress management and 3D IC heat & temperature management
7.10	Quantum computing cryogenic temperature devices, circuits, and technologies.

8	**Clocking**
High-performance, low-jitter clocking techniques including low-phase-noise PLLs continue to be of interest for communication systems and other applications. Equally important is frequency scaling, power reduction, purity improvement and area reduction techniques for fully integrated clock generation. *Low power fully programmable monolithic clock generators are required for clocking low-cost digital systems. Crystal oscillators and oscillator interfaces needed for accurate time references consume much of the standby power for ULP devices that must wake up at specific time intervals to communicate with mesh networks or perform specific tasks on a schedule. ULP low ppm drift, time, or frequency references are needed for these applications. For a large SoC in a noisy power/ground environment, and for CPU complex with multiple power and multiple synchronous and asynchronous clock domains, low power and low-cost techniques to distribute a clean clock signal is required.* *Frequency stability is often limited by component aging, so there is a need to design stable frequency references without expensive integrated or external components for high-stability integrated oscillators. Fast startup crystal oscillators with low phase noise and fast frequency settling is required. We also need to support these high-performance, low-phase noise clock sources with high performance phase noise BIST.*	
8.1	Power and area efficient, low jitter clock generation circuits for communication systems and other applications. Wide dynamic range frequency synthesizers (few kHz to tens of GHz) with sub-100fs integrated jitter Including high performance, low-jitter PLLs and digitally enhanced PLLs
8.2	Frequency scaling, power reduction, purity improvement and area reduction techniques for fully integrated clock generation (including multiple clock generation, temperature stability and long-term drift)
8.3	Techniques for high-accuracy multi-phase clock generation and phase correction. Including solutions to enable low IO clock jitter for high performance
8.4	Low power fully programmable monolithic/integrated clock generators for clocking low-cost and low-power digital systems and connectivity applications and High-Q resonators
8.5	Low power, high stability integrated oscillators and resonators – frequency stability is often limited by component aging, so we need a way to design stable frequency references without expensive integrated or external components; circuit and system techniques to address temperature coefficients on integrated reference oscillators
8.6	Ultra-low power frequency or time sources with drift rates suitable for real time clock applications, and for controlling sleep/wake sequences emphasizing standard CMOS solutions
8.7	Clock solutions for CPU complex with multiple power and multiple synchronous and asynchronous clock domains: low power / low-cost techniques to distribute a clean clock signal around large SoC in a noisy power/ground environment

8.8	Fast startup crystal oscillators with low phase noise and fast frequency settling
8.9	Ultra-low jitter (<100fs) small area ring oscillator-based frequency synthesizers
8.10	Power efficient clocking solutions, including fast start/stop for power efficiency during intermittent traffic to enable power scaling with bandwidth
8.11	Low-cost testing techniques to support compensation of high stability oscillators
8.12	High performance phase noise BIST
8.13	Clock distribution and synchronization for chiplet systems

9	**Efficient Circuits**

This section describes the needs of the members in the area of circuits and architectures energy and power-efficient circuits. The interest in circuits spans many orders of magnitude in power and energy. Challenges exist at all levels from data centers (kW), racks, line cards, desktops, laptops, mobile processors down to circuits in embedded microcontrollers consuming microwatts of active power with nanoamperes of leakage. Novel circuits and controls are desired for deeply scaled CMOS devices to improve the state of the art in both active and static current consumption At the lower end of the power spectrum is the ultra-low powered battery and ultracapacitor driven or energy harvesting application space, challenges remain in key areas such as power/performance/stability scalable analog (ADC's, DAC's, voltage comparators, etc). An example would be an analog to digital converter capable of variable precision conversion with power scaling with the conversion precision. Crystal oscillators and oscillator interfaces needed for accurate time references consume much of the standby power for ULP devices that must wake up at precise time intervals. ULP low ppm drift time or frequency references are needed. Another key ULP need is for CMOS Nanopower current sensors for coulomb counting. Nanopower current sensors would have many uses such as voltage regulator or voltage converter control or to monitor and/or allow control of current consumption.

Power consumption performance challenges increase at advanced nodes, continuing to need improved accuracy, reduced leakage, and stable and predictable circuits.

9.1	Energy efficient digital and analog circuits, especially those tolerant of wide supply and temperature ranges. Including nano-power current sensor for digital coulomb counting and ultra-low power time & frequency, voltage or current references
9.2	Temperature, process, and voltage insensitive, low power, low area CMOS current (or voltage) reference that operates down to 0.5V with good noise rejection
9.3	Control/management of leakage current, ultra-low voltage and low temperature MOS circuit technologies including Cryogenic operation.
9.4	Thermal management circuitry including high accuracy compact temperature sensors with efficient calibration
9.5	Power/performance scalable analog circuits for signal processing, wireless and wireline communication systems
9.6	Auto Calibration, high speed CMOS voltage comparators for voltage detection (sub 50ps range)
9.7	Fast-start analog circuits (including regulators) to allow efficient power gating

10	**Reliable and Functionally Safe Circuit Design**

Robust circuit design means designs that are insensitive to process and environmental conditions; they have high yields and are thoroughly testable. Reliable designs maintain this performance during the product's lifetime. Functional Safety is the absence of unreasonable system risk due to hazards caused by malfunctioning behavior of Electrical/Electronic systems. This includes architectural features to detect and mitigate the effects of component failures, but not necessarily fail-operational or fault-tolerant characteristics.

Historically, steady improvement in the tradeoff between performance, area, and power has, however, slowed, while the desire for progress in function/power is as great as ever. At the same time, as supply voltages have become lower and geometries decrease, worst-case variability of device parameters has become more significant. Continued innovation is needed in the design and architecture of circuits tolerant to built-in and environmental effects without costly overperformance at nominal conditions. Member companies are seeking approaches that are robust under variations in global and local process parameters, device mismatches, hard or soft failure of individual components, and under the impact of environmental conditions such as supply and temperature, as well as noise and ESD. In addition, enhanced testability—analogous to IDDQ and scan testing for logic—is desirable for reliable analog and power circuits.

10.1	Circuit architectures of clock, power management, and data converters, etc. to achieve safety integrity as individual IP or subsystem with efficient implementations. Possibilities include ADC BIST
10.2	Inter-chip circuit infrastructure to enable in-field monitoring of critical interconnect, I/O, pad-ring, packaging failures and degradation
10.3	Circuits for increased tolerance and adaptability to manufacturing/process variability including parameters with non-Gaussian distributions, such as those that are many deviations away from the mean (6+ sigma)
10.4	Increasing reliability by design with unreliable components, soft errors, ageing and voltage “overstress”; testability including reliable BIST for analog circuits; long term reliability and odometers;
10.5	Circuits for increased tolerance and adaptability to manufacturing/process variability including parameters with non-Gaussian distributions, such as those that are many deviations away from the mean (6+ sigma)
10.6	Noise tolerant (EMC) and ESD techniques including CDM and IEC modeling and analysis
10.7	Systems and circuit techniques that incorporate functional safety features, including fault tolerance, fail-operational, diagnostics and monitoring of critical functions

11	**Analog Design Productivity and Automation**
Improvements in design productivity and automation are critical as the quantity of analog design is driven by an increasing need for system-level devices to interact with the physical world. Two forces are driving a productivity crisis in analog engineering. Analog design becomes more difficult as production moves to smaller nodes. Analog designers are aging out of the workforce at a higher rate than other disciplines, leading to a loss of expertise. This makes a renewed interest in analog productivity and automation quite timely.	
11.1	Improved digital and/or analog circuit design optimization and productivity through novel CAD techniques, including, but not limited to, utilizing AI/Machine Learning-assistance, data mining of process, test, and circuit analysis databases
11.2	Widely applicable mixed-signal isolation technologies, structures, design rules, and methodology for SoC, SiP and 3D
11.3	Architecture or design methods which are more amenable to at least partial automation of design, layout, or verification. This is meant to include both highly domain specific automation of fairly standard sub-circuits and more general applicable automation at a full analog functional block level
11.4	Human comprehensible analog automation. One of the major impediments to the adoption of analog automation has been that the outputs are inscrutable to human inspection and intuition. This leads to a perception of lack of robustness of the outputs. Analog automation that eliminates this problem is of particular interest.
11.5	Automation techniques to improve migration of analog designs from one technology to another. Preference will be given to human comprehensible results
11.6	Functional level modeling, synthesis, and verification of high-performance analog systems. CAD tools, techniques for reliable automated functional-to-circuit level transfer for design and verification.
11.7	CAD tools for the combined design and verification of analog circuits on chiplets and/or heterogeneous technologies systems