Research Needs: Packaging

June 1, 2022

Semiconductor Research Corporation (SRC), Durham, NC 27703

Overview

Semiconductor-based computing and communication has revolutionized all aspects of modern life and will continue to play an influential role moving forward. Applications for small, flexible, light, easy-to-use interconnected consumer medical and industrial devices will continue to expand, while technologies such as flexible & stretchable electronics, human body compatible electronics, and nanotechnology that require additional development for broad acceptance, will continue to gain importance. In addition, to support the performance and energy efficiency roadmap and increasing packaging requirements, innovations will be needed for devices that are deployed in data centers, perform high-performance computing (HPC), and facilitate communications. Today there is broad recognition that heterogeneous integration of diverse Intellectual Property (IP) blocks on the package, which serves as a compact, high-performance platform, is critical for the evolution of semiconductors. To support semiconductor evolution, microelectronics packaging needs to progress along the following directions:

- Component scaling to enable system form factor and interconnect density scaling in heterogeneous packaging architectures.
- Power-efficient interconnects (wired, wireless, and optical) to enable high on-package and off-package bandwidth in 2-D/2.5-D/3-D architectures.
- Cost-effective, thermal management solutions for the proliferation of 2-D/2.5-D/3-D architectures and to ensure consumer devices meet ergonomic constraints.
- Heterogeneous integration of digital, analog, radio frequency (RF), optical, and discrete devices into high-performance, low-power, as well as cost-sensitive products of the future.
- Architecture and structure innovation for both compact and large package sizes to house (sub)system-level integration. Electrical and optical data input/output (IO), low-loss antenna and waveguide integration, power delivery, and thermal dissipation for both high power density and high total power consumption, low manufacturing cost, etc. should be considered.
- Methodology and strategy for circuits, chiplets, package, and (sub)system co-design in 3D integration to yield the best power, performance, and area (PPA) with a combination of, e.g., functional partitioning of the chiplets, architecture & structure of the package, interconnect technology, IO, and channel arrangement, etc.
- Advanced packaging for automotive applications with the goals of zero defects and high reliability.
- Sensor integration in packaging with improved form factor, energy efficiency and capabilities.
- Small form factor packages with improved high-voltage capability.
- Process engineering (including an understanding of in-process behavior through models, metrologies, and materials) to help develop scalable, cost effective, high-yielding manufacturing and test processes.
- Reliability engineering to ensure “reliable by design” configurations that meet the demands of diverse application environments including HPC, automotive, aerospace, and medical environments.
- Predictive modeling to create robust-by-design package designs that incorporate increasing levels of heterogeneity.

This document is not intended to cover the complete landscape of the required research, but rather to identify the most critical areas in need of university research. We highlight key strategic challenges in five categories:

1. Design Enablement and Tools
2. Interconnects and Architectures
3. Power Delivery and Thermal Management
4. Metrology and Modeling
5. Materials

The Global Research Collaboration (GRC) division of SRC focuses on research in a timeframe five or more years ahead of technology release. Research on advanced tools and techniques such as modeling, simulation, and characterization can

be of value with implementation timelines as low as one to two years post project completion. This timeframe represents the "sweet spot" for pre-competitive, collaborative research, after which the industry focuses on proprietary development for technology differentiation. Successful research proposals will need to match this timing.

SRC has also released a document called the Decadal Plan for Semiconductors (www.src.org/about/decadal-plan/) which describes five Seismic Shifts facing the electronics industry in the coming decade. Research should address issues arising from at least one of them:

- Smart Sensing – The Analog Data Deluge
- Memory & Storage – The Growth of Memory and Storage Demands
- Communication – Communication Capacity vs. Data Generation
- Security – Information & Communications Technology (ICT) Security Challenges
- Energy Efficiency – Compute Energy vs. Global Energy Production

Moving forward, the SRC is also embarking on an effort to broaden participation in its funded research programs. This aggressive agenda will help us drive meaningful change in advanced ICT that seem impossible today. In the programs we lead, we must increase the participation of women and under-represented minorities as well as strike a balance between U.S. and non-U.S. citizens, creating an inclusive atmosphere that unlocks the talents inherent in all of us. Please visit https://www.src.org/about/broadening-participation/ for more information about the 2030 Broadening Pledge.

With the expected growth of semiconductor chip manufacturing in the coming years, it is imperative that the chemicals, materials, and processes involved in their manufacturing are as sustainable as possible. Therefore, research must take into consideration the environmental and human health impacts of new chemistries and focus on the development of more environmentally preferable materials and processes that are more efficient, more effective, and safer. In general, processes that are known to use chemicals that are persistent, bio-accumulative, or toxic will benefit from more environmentally benign substitutions. Two specific examples include high global warming potential (GWP) gases used for etching and chamber clean and a diverse class of per- and poly-fluoroalkyl substances known collectively as PFAS. The industry faces particularly difficult challenges with PFAS because the carbon-fluorine bond provides essential function and is used across many applications such as photolithography, wet etch, and advanced packaging (i.e., encapsulations and thermal interface materials, flux, adhesives, hydrophobic coatings, and hermetic materials). Due to public health concerns, emerging legislation and regulations are focused on banning or restricting the entire class of PFAS chemicals which by some definitions include any chemical with a per-fluorinated methyl group (-CF3) or a per-fluorinated methylene group (-CF2-), bringing into scope fluoropolymers.

More details of each category in the list of key strategic challenges above can be found in the following sections, where the ordering is not intended to reflect the prioritization of a given research need.

Contributing Members include:			
Arm	IBM	Intel	MediaTek
NXP	Samsung	SK hynix	Texas Instruments
Semiconductor Research Corporation			

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1	**Design Enablement and Tools**
Modeling and characterization tools for new and existing architectures that enable codesign and manufacturing of 2D, 2.5-D, and 3-D architectures: • Electromagnetic full-wave solvers for inhomogeneous, anisotropic lossy dielectrics and conductors, with algorithms optimized for both computation time and memory and approaching linear computational complexity; electrical and optical frequency (wavelength) ranges should be covered. • Design and characterization tools for optical and wireless interconnects. • Component and system level simulation tools for thermal management and power delivery that fully accommodate steady-state and transient conditions, comprehend dimensional and design complexity, and allow seamless integration with design layout tools. • Simulation tools that allow for the complete thermomechanical description of packages during manufacturing (to increase confidence in yield projections and to define process envelopes), reliability, and use conditions for development of correct-by-design HI configurations. • Multiphysics based tools and algorithms to enable efficient co-optimization across multiple domains, e.g., thermals, power integrity, signal integrity, reliability, and manufacturability. • Artificial intelligence (AI) and machine learning (ML) algorithms and tools for design, optimization, and simulation speedup with controlled accuracy including modeling of complex systems.	
1.1	Heterogeneous integration of separately manufactured components into a higher-level System-in-Package (SiP). Such components can be individual dies, chiplets, die stacks, subassemblies, or packaged dies/die stacks, micro-electromechanical system (MEMS) devices, passives, sensors, light sources, detectors, optical fibers, or waveguides in and out of the package, etc. Low-cost, high manufacturing yield, and secure implementation are desirable. Temperature etc. should be constrained during integration to avoid altering device characteristics, especially for those in advanced process nodes.
1.2	Compact, socketable, and ball grid array (BGA) form factor.
1.3	Integration of antenna arrays and metal interconnects into packages for a carrier frequency range of 28 – 3000 GHz, and a bandwidth of 28 – 500+ GHz at low loss, small bump pitch, low cost, high reliability, and high manufacturing yield.
1.4	Innovative, low-cost packaging for SiP.
1.5	Packaging co-design with emphasis on enabling cost-effective, high-precision testing.
1.6	Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation.
1.7	Validation methodologies and experimental techniques for material, component, and system characterization. Specific targets are: • Dielectric characterization up to 500 GHz and beyond. Scope includes anisotropic and inhomogeneous materials. • Surface roughness modeling with experimental validation up to 500 GHz.
1.8	Concepts for low-cost, reliable, high-voltage packaging (continuous operation over 2 kV and transients over voltages up to 15 kV).
1.9	Memory (SRAM, DRAM, NVM, etc.) is becoming an important part for all edge applications, where systems need to be more and more tailored to use cases and integrated through custom packages.
1.10	Modeling and characterization tools for new and existing power delivery architectures that enable co-design of the power delivery network with circuit design.
1.11	High-accuracy sensors and battery management.

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2	**Interconnects and Architectures**
Packaging plays a critical role in enhancing system performance by providing improved inter-component connectivity. High bandwidth and high bandwidth density is enabled both by providing low-loss interconnects and by increasing the number of inter-package and intra-package connections between components, in a cost-effective manner. There is a strong need to both develop new packaging architectures and to enhance interconnect density of the current packaging architectures.	
2.1	Power-efficient, high-bandwidth and high-density I/O. New packaging and system architectures (including electrical, optical, and wireless interconnects) for improved package (per socket and overall system) bandwidth and I/O power efficiency. Specific targets are: • Refer to the IEEE EPS Roadmap (https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html) for interconnect density targets. • Data rate per lane > 400 Gb/s electrical interconnects should target a reach of > 100 mm with power efficiency of the entire link including supporting circuits such as clock & data recovery (CDR) etc. better than 0.3 pJ/b. • Data rate per lane > 1 Tb/s optical interconnects should target a reach of > 25 m with power efficiency of the entire link including supporting circuits such as CDR etc. better than 1 pJ/b. • Power consumption and data rate should be well scaled while minimizing the power, performance, and cost overhead such that the power efficiency can be generally maintained across multiple use scenarios, e.g., at both high and low data rates. • Fiber/waveguide integration for co-packaged optics (CPO) and optical IO (OIO). • Large package size to simultaneously support both electrical and optical IO at 200 Tb/s, 400 Tb/s, and beyond. Power delivery and thermal solution should consider both total and unit-area power consumption and heat generation. Manufacturability and cost effectiveness need to be considered. • Large antenna arrays with fine interconnect pitch, flexible dielectric thickness, large via aspect ratio for mm-wave and sub-THz applications. • Complex integration with xPUs, multiple types of memories, RF/mm-wave/optical circuits and interfaces. • Antennas and waveguide launchers in package. • Side-channel attack mitigation for security sensitive packaged chips. Research in physical methods of improving security in the package is of interest. • TSV-less interconnects and architectures for low cost, high bandwidth solutions
2.2	As interconnects push for higher and higher speeds, design requires almost full isolation of these signals from one another to avoid interference. Thus, even though higher per-lane signaling rates and overall bandwidth are achieved, they do not necessarily always improve bandwidth density. Research should target a linear bandwidth density > 10 Pb/s·m (at die edge).
2.3	At mm-wave and THz frequencies and beyond, interfaces to the outside world are challenged by parasitic effects from traditional resistance, capacitance, and inductance to fringing, roughness, and radiation at multi-GHz frequencies. Research in understanding and minimizing these effects including with novel architecture and structure to help increase interconnect capability is of interest.
2.4	Optical links with transceivers and algorithms supporting high-order modulations, such as 64/128+ APSK/QAM over DWDM configurations, are of interest.
2.5	Cost-effective packaging technology including low-cost material/process, high precision in optical (sub)wavelength scale, and high manufacturing throughput, to support optical-electrical integration with high optical port counts in the order of hundreds to thousands.

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3	**Power Delivery and Thermal Management**
Future power delivery applications are expected to require transient current densities of 5 – 10 A/mm^2 at 1 V or less. There is also a drive to smaller form factors so the power delivery solutions should fit within the footprints of either the package or the die and have a small z-height. Reliable and affordable thermal management technology remains a major packaging challenge driven by the continuous drive towards miniaturization due to the explosion of the number of mobile devices, and by the increase in compute density in data centers and servers. There is continued interest in new and improved thermal management techniques and metrologies to address hotspots, Joule heating and overall thermal design power (TDP) management in space-constrained and/or high power and power density environments to ensure device performance and reliability.	
3.1	New efficient power delivery for 2-D/2.5-D/3-D architectures.
3.2	Integration with lateral power field effect transistors (FETs): low parasitic (< 0.1 nH source inductance), high thermal dissipation (> 60 W/mm^2), enhanced reliability (10 V/µm E-field), and compact form factor.
3.3	Voltage regulator (VR) technologies that can support the high current densities with a small footprint and high-power rail granularity. The input voltage can range from 4 to 48 V and the output voltage can range from 0.3 to 1 V. The VR technology can be either two-stage or single-stage, but the overall efficiency should be in the > 90% range.
3.4	Embedded voltage regulators (eVRs) including the inductors and capacitors that can be integrated on logic dies with minimal cost overhead to the logic wafers. Balls/pins and the metal interconnects inside and outside the package should have low resistance and electromigration to minimize the overall footprint.
3.5	High-efficiency, high-density, cost-effective inductors: • Soft magnetic materials with resistivity > 1 mΩ·cm, high anisotropy field, and low coercivity while offering a high saturation magnetic flux density B_{sat} > 2 T, and that maintain permeability at frequencies up to 1 GHz. • Other novel materials including but not limited to high-performance magnetic composites and ceramics.
3.6	Super high-density (> 5 µF/mm^2), low-impedance, and low-profile capacitors, with improved reliability.
3.7	Wireless power delivery environmentally friendly for consumer applications, targeting > 80% efficiency including loss from air links.
3.8	Thermal management for packages (transient response, hot spots): Materials and substrate development, characterization, and reliability.
3.9	Materials development for thermal management (e.g., high thermal conductivity/electrical isolation of digital/analog components).
3.10	Low-cost thermal solutions for mobile and industrial converters, power supplies, etc.
3.11	Thermal management strategies for 3-D stacks, with two or more stacked dies that maintain junction temperatures Tj < 85°C for memory and Tj < 90°C for logic. The Thermal Design Power (TDP) envelope is intended to cover 5 – 10 W per chip, 20 W per handheld systems, > 100 W for personal computing to ~ 2,000 W logic devices for high-performance computing (including the high-speed and high-bandwidth IOs) with ambient temperatures up to 55°C.
3.12	Form factor restricted thermal solutions to meet both reliability and ergonomic requirements. Passive cooling of handheld systems is limited by heat rejection from the entire platform. Typical thermal solutions are expected to address both sustained and “burst” use conditions under both reliability and ergonomic requirements (e.g., skin temperatures < 40°C for up to 8 hours of power on).
3.13	Novel thermal management approaches for harsh environments such as automotive applications that meet or exceed standard Automotive Electronics Council (AEC) Grade 0. For details refer to: http://www.aecouncil.com/Documents/AEC_Q100_Rev_H_Base_Document.pdf http://www.aecouncil.com/Documents/AEC_Q006_Rev_A.pdf

3.14	Package-level integration utilizing heat sinks and air cooling is becoming limited by thermal constraints. While more exotic cooling solutions exist, these tend to be impractical in production environments due to cost and support requirements. Alternative breakthrough solutions are needed.
3.15	Higher thermal dissipation and higher level of integration of 6G wireless applications.
3.16	Hot-spot metrology and low-cost mitigation schemes including novel materials to address steady state and transient hot spots at thermal densities > 500 W/cm^2.
3.17	Cooling technologies that improve thermal envelopes in for space applications that have significant space, weight and environmental limitations.

4	**Metrology and Modeling**
Metrologies, test, and simulation that enable fundamental understanding of package performance and reliability, help improve manufacturability, and are critical for packaging technology development and optimization.	
4.1	Metrologies enabling fundamental understanding of package thermal, mechanical, and electrical performance, degradation, reliability, and chip-package interaction effects.
4.2	High-resolution, non-destructive metrologies for failure analyses that are able to resolve defects (such as voids, delamination, bump, die, and interface delamination cracks) at a size scale of < 1 µm.
4.3	Metrologies that measure package in-situ surface roughness, surface energy, and mechanical properties such as fracture toughness and coefficient of thermal expansion (CTE) in intricate spaces such as < 10 µm separation between neighboring interconnect bumps. Metrologies to measure surface energy and polarity with fine spatial resolution are desired. Ability to measure surface energy and polarity variation across a package surface area at a spatial resolution of 2 – 5 µm or better, and surface energy accurate to 1 – 2 dyn/cm, as a function of temperature (room temperature to 250°C) and humidity (30 – 60%), is desired. Mechanical properties should be measurable over a wider temperature range, -55°C – 250°C.
4.4	Chemical mapping: Metrology to detect organic and organo-metallic flux residues in intricate spaces such as < 10 µm in size.
4.5	Interfacial adhesion: Metrology to measure adhesion strength of deeply buried interfaces across polymers-polymers, polymers-ceramics, and polymers-metals (including organic and inorganic dielectrics) as a function of temperature and humidity ranges (AEC Grade 0 conditions – see above). It is especially important to characterize adhesion at the small surface areas encountered in sub-20 µm joints. Metrologies to measure adhesion strength of interfaces under cyclic loading.
4.6	Characterization of high-voltage and high-temperature materials (ionic conduction and polarization models).
4.7	High-frequency and high-temperature characterization of low-loss dielectrics and other materials (encapsulants, mold compounds, substrates, etc.), integrated electrical and optical waveguides, etc.
4.8	Non-invasive, quick-turn metrologies for thermal mapping and characterization of 3D stacks.
4.9	Quick-turn metrologies for repeatable and accurate characterization of thermal contact resistances in the range of 0.001 – 0.01°C·cm^2/W.
4.10	Multiple concurrent stress accelerated tests for more realistic use condition reliability prediction.
4.11	Predictive models for materials interface reliability including under cyclic loading.
4.12	Efficient and multi-physics performance, electromigration, and thermomechanical modeling.
4.13	Board-level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation.
4.14	Multiple concurrent stress accelerated tests for more realistic use condition reliability predictions.
4.15	Validation methodologies and experimental techniques for material, component, and system characterization. Specific targets are: • Dielectric characterization up to 500 GHz and beyond. Scope includes anisotropic and inhomogeneous materials.

	• Surface roughness modeling with experimental validation up to 500 GHz.
4.16	Rigorous de-embedding, including transitions, etc., for S-parameter measurements up to 500 GHz.
4.17	Debug, FA/FI techniques to enhance resolution and access for complex 2.5D/3D structures to improve understanding and resolution of key functional failure modes.

5	**Materials**
Materials with interconnect mechanical properties at least as good as tin-silver-copper (SAC) solder over a wide temperature window, compatible with harsh environments, and with individual parameters at least equal to that of the SAC solders. Package materials suitable for automotive and harsh environments (including copper wirebond compatible materials), sensor applications, flexible applications, and medical applications.	
5.1	Materials and interface challenges involved with low-cost, high-voltage, and high-power packaging: Concepts for minimal silicon-package interactions (e.g., charging properties, interface conductivity) in plastic packages under humid, high temperature, and high bias that can cause high-voltage device breakdown shift.
5.2	Polymeric encapsulants for 2-D/2.5-D/3-D architectures with < 20 µm pitch interconnects. • Effective thermal conductivity > 10 W/m·K. • Materials that allow for independent tailoring of CTE (5 – 20 ppm/K) and modulus (10 – 25 GPa). • Material viscosity that is tailorable to allow flow through < 10 µm gaps. • High adhesion strengths to semiconductor, dielectric, metal, and polymer interfaces (Si die, Cu bump, solder bump, lead frames, and organic packages). • Glass transition temperatures > 150°C. • Fracture toughness (K_{1c} > 2 MPa·$m^{1/2}$). • Electrical insulation at < 10 µm length scales. • Breakdown field one order of magnitude higher than that in current polymer materials, which is only in the range 20 – 30 V/µm. • Materials suitable for high temperature applications, (e.g Tamb of 180°C and Tj of 200°C), which can pass AEC Grade 0 conditions (see above).
5.3	New solders, under-bump metallurgies (UBMs), and alternatives to solder-based interconnects for enhanced electromigration and board level reliability performance.
5.4	Materials for lower-cost lead frame packages, including QFP and QFN packages.
5.5	Materials for advanced wire-bonded packages, including stacked die, high power, higher functionality, high-voltage isolation, and high comparative tracking index (CTI) epoxy mold compounds.
5.6	Mechanical properties at least as SAC solder over a wide temperature window (-65 to 150°C), i.e., modulus 20 – 60 GPa, CTE ~ 20 ppm/K, elongation > 35%, tensile strength > 55 MPa, shear strength > 30 MPa; creep, fatigue strengths, and fracture toughness (strain hardening exponents) at least equal to that of the SAC solders. Seamless integration into existing interconnect manufacturing environment. Low-cost, non-planar, scalable interconnects for large-format processing (300 – 500 µm pitch).
5.7	Mechanically stretchable interconnects and flexible packaging for applications including wearable Internet of Things (IoT). Focus is on stretchable conductive materials and composites (as opposed to spring type structures where geometry enables stretching). • Interconnect conductivity should be as high as possible, with a target value range of 10,000 – 25,000 S/cm and a desired envelope target of 40,000 – 60,000 S/cm (about 10x lower than that of Cu). • The cyclical stretching ability (i.e. no plastic or permanent deformation) should be as high as possible. Target at least 20% elastic stretch, with an envelope target of 30%. • Target materials to achieve a flexible interconnect bend radius of < 5 mm with < 1% drain current variation for attached die sizes < 2 x 2 mm^2.

5.8	Solders with peak reflow temperature < 140°C for decreased stress between joined components.
5.9	Material opportunities for printed circuit board (PCB) technology; high reliability (up to 100,000 hours), high temperature (150 – 250°C), high voltage (> 100 V), high frequency, high density, and corrosion free in high temperature/humidity environment.
5.10	Corrosion resistance through high temperatures up to 175°C (may be up to 200°C) for automotive and harsh environments and compatible with copper wirebond packages.
5.11	Package process compatible corrosion resistant coating/materials to prevent or mitigate (e.g., Cu wirebond) corrosion by ions such as chloride.
5.12	Materials for sub-20 µm pitch vertical interconnects: • Current carrying capability > 1 x 10^5 A/cm^2. • Resistivity < 10 µΩ·cm. • Maximum joining temperature < 180°C (reduce delta between room temperature and melting point) to reduce stress and warpage.
5.13	Packaging materials for advanced chip integration such as GaN and SiC.
5.14	Package materials with excellent near-infrared (NIR) sensitivity for LiDAR applications.
5.15	Packaging materials for high temperature automotive applications capable of AEC Grade 0 (see above) and beyond, ambient temperature of 180°C and Tj of 200°C.
5.16	Materials research for better compatibility with extreme or non-standard environments such as immersion cooling, high radiation (e.g. space and disaster recovery), and chemically harsh (e.g. space and IoT edge devices).
5.17	High relative dielectric constant (> 60) polyimide material with gap fill < 0.1 µm capability.