Research Needs: Logic and Memory Devices (LMD)

May 1st, 2023

Semiconductor Research Corporation (SRC), Durham, NC 27703

This document is prepared to accompany the Call-for-White-Papers for the research program of Logic and Memory Devices (LMD). The research needs in this area are very wide. We present here selected areas of high priorities as identified by our sponsor members.

In an integrated circuit, transistors and memories are the most important and common components. Traditionally, the main goals for scaling are density, performance, and cost. Power reduction, both dynamic and static, is one of the most important limiting factors, the biggest opportunity, to be addressed at the device level.

For transistors, the push is for devices with lower supply voltage to generate same or higher current per unit channel width and have low capacitance at the same current density as state-of-the-art silicon CMOS.

The natural progression beyond the current manufacturing technologies, SOI planar MOSFETs and FinFETs, will be nanowire MOSFETs based on Si channel materials. There are also potential benefits to alternate channel materials with significantly better transport characteristics than silicon. Scaled, smaller, Low-resistivity contacts and wires to those alternate channel materials are equally critical to low-voltage, high performance transistor solutions beyond silicon. Also critical for low-power operation are low-capacitance dielectric materials and work-function modulation technology.

A new area in the LMD program is monolithic heterogeneous 3D integration that will enable greater functionality per footprint including integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics. Therefore, it has the potential to become a truly multi-functional platform.

An alternate signal using spin or magnetism as a state variable rather than charge or voltage can avoid resistive power dissipation and is an attractive option. However, the propagation and logic operation based on spin, or conversion of spin back to electrical signal, is a big challenge.

Memories are classified into major categories of nonvolatile memories (NVMs), SRAM, and DRAM. Each has its trade-offs in different aspects of performance, its unique features and structure, but all are critical to the industry. For NVMs, the industry has been depending on the charge-storage type, which are floating-gate FET and charge-trapping FET. However, both devices have a tunnel gate oxide at the channel interface, but due to the stringent requirement of long retention time, this tunnel oxide is already at its minimum thickness and is no longer scalable. Recent products have turned to 3-D to increase density by using the 3rd dimension. The industry has started to turn to non-charge-storage types of memory cells that are typically two-terminal. For these NVMs, the critical metrics are write/erase power, multi-bit and density, endurance and reliability, low latency, etc. The leading contenders are MRAM, PCRAM, FeRAM, and RRAM, among others.

These NVM cells typically exhibit *I-V* characteristics that are too conducting at low bias and provide leakage paths when utilized in x-bar like memory arrays. A selection device is needed in series with a memory element to curtail the leakage from unselected cells. For density and ease of operation, it is desirable to have a selection device that is two-terminal. Selector device challenges include low turn-on voltage, high current density capability in on state, ultra-low current in off state, and high endurance. Ultimately, an NVM cell with built-in selection device is the preferred solution.

Scaling the 6-transistor SRAM cell and the 1T1C DRAM cell is a formidable challenge. Lower supply voltage, demanded by lower power, causes noise margin issues. Area scaling is also challenged. Revolutionary device concepts to realize the same functions with fewer device components would be extremely beneficial to the industry.

The GRC typically focuses on research in a timeframe 5 – 8 years ahead of technology release. This timeframe represents the “sweet spot” for pre-competitive collaborative research, after which the industry focuses on proprietary development for technology differentiation by each company. Successful research proposals should match this timing.

SRC has also released a document called the Decadal Plan for Semiconductors (www.src.org/about/decadal-plan/) which describes five “Seismic Shifts” facing the electronics industry in the coming decade. Research should focus on one of these:

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- Smart Sensing – The Analog Data Deluge
- Memory & Storage – The Growth of Memory and Storage Demands
- Communication – Communication Capacity vs. Data Generation
- Security – ICT Security Challenges
- Energy Efficient – Compute Energy vs. Global Energy Production

While a particular research submission might address the challenges of multiple shifts, each investigator should choose one which best aligns to their effort, perhaps at the end application level.
Moving forward, the SRC is also embarking on an effort to broaden participation in its funded research programs. This aggressive agenda will help us drive meaningful change in advanced information and communication technologies that seem impossible today. In the programs we lead, we must increase the participation of women and under-represented minorities as well as strike a balance between U.S. citizens and those from other nations, creating an inclusive atmosphere that unlocks the talents inherent in all of us. Please visit, https://www.src.org/about/broadening-participation/, for more information about the 2030 Broadening Pledge.

With the expected growth of semiconductor chip manufacturing in the coming years, it is imperative that the chemicals, materials, and processes involved in their manufacturing are as sustainable as possible. Therefore, research must take into consideration the environmental and human health impacts of new chemistries and focus on the development of more environmentally preferable materials and processes that are more efficient, more effective, and safer. In general, processes that are known to use chemicals that are persistent, bio-accumulative, or toxic will benefit from more environmentally benign substitutions. Two specific examples include high global warming potential (GWP) gases used for etching and chamber clean and a diverse class of per- and poly-fluoroalkyl substances known collectively as PFAS. The industry faces particularly difficult challenges with PFAS because the carbon-fluorine bond provides essential function and is used across many applications such as photolithography, wet etch, and advanced packaging (i.e., encapsulations and thermal interface materials, flux, adhesives, hydrophobic coatings, and hermetic materials). Due to public health concerns, emerging legislation and regulations are focused on banning or restricting the entire class of PFAS chemicals which by some definitions include any chemical with a per-fluorinated methyl group (-CF3) or a per-fluorinated methylene group (-CF2-), bringing into scope fluoropolymers.

In this call, we encourage innovative ideas that are impactful to the semiconductor industry. Proposed work of high-risk and high reward is especially suitable for university research. When submitting the white papers, researchers are asked to indicate the topics (in number and sub-category such as 1.4) into which their research topic can best fit.

Contributors

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Research Needs

In this call, due to limited resources, we have identified topics our members have considered the most critical and relevant for university research. The list of topics with more detailed explanation is shown below:

1	Monolithic Heterogenous 3D Integration (MH3D)
Monolithic heterogeneous 3D integration allows higher density packing and integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics, therefore it has significant advantage for the development of multi-functional platform. Currently, significant progress has been made in III-V wafer bonding to 300 mm wafer sizes and hybrid Ge/III-V devices on Si. Looking further ahead, vertical Tunnel FETs, 2D materials and Spintronics are emerging as post-CMOS alternatives while continued scaling is possible with gate-all-around (GAA) and nanowire devices. C(complementary)FET and 3D integration (e.g., Ge PMOS GAA on Si NMOS FinFET) and possible combinations will be investigated to find the promising CMOS structures. Finally, interconnect technology with low parasitic RC factors and high thermal stability (device formation technology to reduce thermal shock) needs additional research.	
1.1	1D Materials (CNTs & Si-/III-V-based NWs, etc.)
1.2	2D Materials (Graphene, MoS2, WSe2, etc.)
1.3	High-Electron-Mobility-Transistors a.k.a. HEMTs (GaN, SiC, etc.)
1.4	High mobility Semiconducting Oxide thin film transistors compatible with BEOL including reliability and variation improvements
1.5	Next-generation Spintronic MRAM (Spin-Orbit-Transfer a.k.a. SOT-MRAM)
1.6	C(complementary) FET and 3D integration (e.g., Ge PMOS GAA on Si NMOS FinFET)
1.7	Low-thermal budget process modules and new schemes for logic and memory devices

2	*Logic devices*
Many options of materials have been explored: III-V compounds, Si_xGe_{1-x} compounds or pure Ge, graphene, carbon nanotube, TMDs (Transition Metal Dichalcogenides such as MoSe2), other 2-D and 1-D materials and structures, etc. However, the consistent demonstration of high-quality channels and gate-stacks, as well as stable low resistance contacts solutions necessary to exceed the state-of-the-art silicon power AND performance capabilities is yet to be achieved on single n and p-type devices. Tunneling based transistors share the attractive feature of steep subthreshold slope beyond the fundamental limit in MOSFETs. TFET performance and parametric variability remain outstanding challenges in need of innovative materials and device structure innovative solutions. Spin-based devices have also been an active subject of research. Although research progress has been made over the years, their performance and potential applicability as platform-capable devices lack significantly when compared to incumbent advanced CMOs logic devices and their foreseen evolution. Nonetheless, this presents in itself opportunities for innovation in materials and structures tackling efficient spin-to-charge and charge to-spin conversion along with device concepts able to render disruptive levels of performance, power consumption, density, and robust operating windows compared to silicon-based CMOS logic technologies. Novel logic device concepts are sought after beyond those mentioned above.	
2.1	MOSFETs with high-mobility channel materials
2.2	Transistors based on tunneling
2.3	Transistors based on non-tunneling transports & phenomena
2.4	Low capacitance structures or materials for low power operation
2.5	Multi work function materials for having multi-Vt device

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3	*New Concepts for contacts, junctions, and gate structures*
Solicited also are truly innovative concepts that can address the roadblocks encountered on channel materials, gate-stacks, and contacts for devices based-on but not limited-to 1D CNTs, 2D graphene and TMDs, and semiconducting oxides, BEOL compatible transistors, etc. The materials and processes concepts proposed should be self-consistent in the sense of enabling integrated device-level demonstrations exhibiting breakthrough performance compared to published literature, results should be repeatable, and controllable.	

4	*Memories*
Revolutionary concepts to realize the SRAM or DRAM functions with new materials or simpler device and layout structures. Novel physical mechanisms (beyond charge-based) for fast switching (last level cache type) memories. All topics related to electrically switched Magnetoresistive RAMs (MRAM), including new materials and devices for higher performance and increased density. The leading examples are Spin-Transfer-Torque MRAM (STT MRAM), field free Spin-Orbit-Torque MRAM (SOT MRAM), and field free Voltage-Controlled Magnetic Anisotropy-MRAM (VCMA MRAM). Some Key Challenges are: • Development of SOT and VCMA devices and architectures for high density memories • New materials and device structures to lower the switching current while maintaining data retention time and achieving high switching speed with low error rate • New tunnel barrier materials for high magnetoresistance and low resistance-area product to enable continued scaling • New capping layer and etching/passivation techniques for improving MTJ device reliability and yield NVMs based on Ferroelectric materials and effects. All topics related to new dielectric materials and integration schemes with transistors that show high polarization and low coercive field under low thermal budget process. Fundamental understandings of the non-ideality effects (imprint, fatigue, and wakeup) and their temperature and film thickness dependence. Novel methods and platforms to extract memory device performance and related material characteristics. Any other novel NVM cell concepts not referenced above but with the potential to demonstrate viability on performance, state controllability and variability, as well as reliability. Nonvolatile memory cells that are capable of continuum equilibrium states. The challenges are controllability and reliability. They provide high density and are especially suitable for neuromorphic computing architectures. Analog nonvolatile memory elements exhibiting symmetric resistance tuning in response to pulsed inputs are particularly attractive. Problems and solutions that may arise when various new memory materials and devices operate as neuromorphic computing memory are also of interest. A systematic methodology to quantify the error tolerance and yields for EDA/design enablement.	
4.1	Revolutionary SRAM, CAM and DRAM cell concepts
4.2	Magnetic RAM and SOT MRAM
4.3	Ferroelectric RAM
4.4	Metrology for memory devices
4.5	Other novel concepts for digital memories
4.6	Analog Memories

5	*Selection Devices for memory arrays*
A critical component for two-terminal NVM cells. Area efficiency is an important consideration in memory cell design.	

6	*Embedded devices*
Logic, memory, and interconnect devices embedded in monolithic-3D, back-end-of-line (BEOL), or other beyond-TSV/interposer processes. Novel methodology for enabling these embedded devices co-design with front-end logic transistors.	

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7	*Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena*
To help advancement in logic and memory devices, the use of numerical simulation is often required. In this area, we solicit ideas for improvements in modeling capabilities and in developing computationally efficient methods for materials, processes, and device operation. Use of these tools to study new material properties, unit processes, device behaviors, and quantum phenomena arising from nano-scale geometries is of high interest. Modeling of benefits of new power delivery architectures, including Back Side Power Delivery Network (BSPDN) is also of interest. The efforts to perform large-scale Design Technology Co-Optimization (DTCO), and to build multi-physics/domain simulation methodology are highly encouraged. Finally, technology for reliability analysis (simulation/modeling) is needed.	
7.1	Improvements in modeling and simulation capabilities
7.2	Modeling of new power delivery architectures
7.3	Design Technology Co-Optimization (DTCO)

8	*Reliability*
Reliability is a topic of interest for both logic and memory devices. Proposals addressing reliability issues pertaining to a specific device (especially emerging memories) should be submitted to the group of the device type.	

9	*Other topics*
Outside the seven focus areas above, all submissions will be considered if containing outstanding, out-of-the-box ideas.	