Research Needs Document: Nanomanufacturing Materials and Processes

April 10, 2023

Semiconductor Research Corp. (SRC), Research Triangle Park, NC 27703

Background

This document is prepared to accompany the Call-for-Research in the research program of Nanomanufacturing Materials and Processes (NMP). The research needs in this area are very broad. We present here selected areas of high priority as identified by our sponsor members.

There is no doubt that nanomanufacturing is getting increasingly difficult. Feature sizes are already ~10 nm in production. Accordingly, research must be directed at enabling dense and regularly placed smaller feature patterns. For lithography, EUV is in production, yet challenges exist to insure sustainable patterning scalability. Metrology and defect detection are critical, and their effectiveness must be improved to ensure that capable solutions exist in a timely and cost-effective manner. For unit processes, new materials are sought after for logic and memory devices. These material options must be paired with manufacturable deposition and patterning techniques that can render thermally, mechanically, chemically, and electrically stable structures. In addition, functional diversification calls for a wide range of other devices, such as required by analog applications and the Internet of Things. For interconnects, the reduced size (thickness and line width) introduces additional scattering and at the same time, reliability problems increase. Interlayer dielectrics also experience increasing difficulty in further reducing the dielectric constant. Manufacturing methods and process materials which reduce device and interconnect variability are required.

For an overview, we divide nanomanufacturing into four major groups:

I. Patterning
II. Front-end processes (FEP)
III. Back-end processes (BEP)
IV. Materials and Processes for Monolithic Heterogeneous 3D Integration, Metrology, Modeling & Simulation

It should be noted that the boundary between FEP and BEP is not clearly defined in the industry, due to the increasing kinds of devices fabricated between the semiconductor substrate and the first metal level. Here we simply put FEP as processes for devices of all kinds, including memories, passives, TFTs, sensors, etc., and BEP as those for interconnects and interlayer dielectrics.

The Global Research Collaboration (GRC) division of SRC focuses on research in a timeframe five or more years ahead of technology release. Research on advanced tools and techniques such as modeling, simulation, and characterization can be of value with implementation timelines as low as one to two years post project completion. This timeframe represents the “sweet spot” for pre-competitive, collaborative research, after which the industry focuses on proprietary development for technology differentiation. Successful research proposals will need to match this timing.

SRC has released a document called the Decadal Plan for Semiconductors (www.src.org/about/decadal-plan/) which describes five Seismic Shifts facing the electronics industry in the coming decade. Research should address issues arising from at least one of them:

- Smart Sensing – The Analog Data Deluge
- Memory & Storage – The Growth of Memory and Storage Demands

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- Communication – Communication Capacity vs. Data Generation
- Security – Information & Communications Technology (ICT) Security Challenges
- Energy Efficiency – Compute Energy vs. Global Energy Production

Moving forward, the SRC is also embarking on an effort to broaden participation in its funded research programs. This aggressive agenda will help us drive meaningful change in advanced ICT that seems impossible today. In the programs we lead, we must increase the participation of women and under-represented minorities as well as strike a balance between U.S. and non-U.S. citizens, creating an inclusive atmosphere that unlocks the talents inherent in all of us. Please visit https://www.src.org/about/broadening-participation/ for more information about the 2030 Broadening Pledge.

With the expected growth of semiconductor chip manufacturing in the coming years, it is imperative that the chemicals, materials, and processes involved in their manufacturing are as sustainable as possible. Therefore, research must take into consideration the environmental and human health impacts of new chemistries and focus on the development of more environmentally preferable materials and processes that are more efficient, more effective, and safer. In general, processes that are known to use chemicals that are persistent, bio-accumulative, or toxic will benefit from more environmentally benign substitutions. Two specific examples include high global warming potential (GWP) gases used for etching and chamber clean and a diverse class of per- and poly-fluoroalkyl substances known collectively as PFAS. The industry faces particularly difficult challenges with PFAS because the carbon-fluorine bond provides essential function and is used across many applications such as photolithography, wet etch, and advanced packaging (i.e., encapsulations and thermal interface materials, flux, adhesives, hydrophobic coatings, and hermetic materials). Due to public health concerns, emerging legislation and regulations are focused on banning or restricting the entire class of PFAS chemicals which by some definitions include any chemical with a per-fluorinated methyl group (-CF3) or a per-fluorinated methylene group (-CF2-), bringing into scope fluoropolymers.

Research Needs

The research needs for nanomanufacturing are obviously very wide. In this call, due to limited resources, we have identified what our members have considered to be the most critical items for university research. The list of topics within these four groups are shown as follows:

I. Patterning

1. Resist, patterning, and mechanistic insight for EUV lithography with focus on:
    1. High numerical aperture (NA) resist concepts beyond chemically amplified resist:
        1. High absorbance materials (resists and underlayers).
        2. Pattern transfer of <20nm thick films including post-exposure treatments.
        3. Design and understanding of new contrast mechanisms for high NA EUV.
        4. Nanoscale metrology.
        5. Resist and underlayer mechanistic interaction study.
        6. Dry development for CAR.
        7. Model-based PFAS elimination/mitigation in resists.
    2. EUV mask novel material and patterning:

1. High-k (darker) materials for thin absorber binary mask (<50nm).
2. Hard-mask pattern transfer for aggressive resolution and 2D structure fidelity.
3. Damascene patterning process.
4. Positive tone metal containing resist or other resist concepts.
5. Mechanistic study on propagation of secondary electrons from each film, PR, under layer and various inorganic films.
6. Mask 3D effect on anamorphic high NA systems.
7. Understanding/improvement of bright field masks to facilitate contact hole printing with high resolution negative tone resists.

2. Directed self-assembly (DSA) advances for:
    1. Block copolymer alignment defect improvement through new block copolymer and brush synthesis.
    2. Multi-pitch using single block copolymer.
    3. Implementing vertical orientation.
    4. Regular and dense placement of molecular precursor seeds for low-dimensional devices.
    5. Selective infiltration schemes for block co-polymer.
    6. Selective etch for new DSA polymers.
    7. Line/Space needs for DSA:
        1. BCP:
            1. Gen1 High-chi materials 20-24nm pitch.
            2. Gen2 High-chi materials <20nm pitch.
            3. LER and LWR post-etch <1.7nm.
            4. High etch selectivity between the two blocks.
            5. DSA of A-B-C Tri-block copolymer.
            6. Pitch independent self-assembling materials.
            7. Enhancing the thermal stability of PS-PMMA based BCP up to 300^0C.
            8. Functional BCPs (cross-linkable, degradable, chain scissioning, etc.).
        2. Brush/underlayer:
            1. Selective deposition on metal and ILD.
            2. Pitch independent self-assembling materials.
            3. Surface energy compatible with BCP.
            4. ≤ 5nm underlayer thickness.
            5. Etch selective to resist.
            6. Directly patternable underlayers for DSA.
        3. Process:
            1. Sequential infiltration of single BCP block selective to another.
            2. Solvent vapor annealing for BCP.
            3. Dry development rinse material (DDRM) to aid with pattern collapse.
            4. Novel processes for DSA.
        4. Characterization:
            1. Quantification technique for underlayer grafting density.

2. Molecule mapping and orientation for DSA underlayer.
3. Characterization of substrate surface and alterations for metal and ILD.

3. Self-aligned patterning processes:
    1. Patterning material, scheme, and processes (e.g., fully self-aligned Via, COAG, Air-gap spacers, etc.)
4. Etch-free feature patterning (i.e., guided, or controlled deposition):
    1. Direct Write of templated ASD of hardmask.
    2. Controlled deposition.
5. Patterning for sensitive materials.

II. Front-End Processes

1. Emerging materials for devices - Chemistry and Synthesis:
    1. Wafer-scale growth of device-quality TMD, FE and AFE films.
    2. Defects free wafer-scale transfer processes for 2D materials (TMD, graphene).
    3. Low contact resistance for 2D materials $<10^{-9}$ ohm-cm.
    4. ALD gate oxide deposition on 2D materials.
    5. Synthesis of defect-free arm-chair graphene nanoribbons with electrical bandgap ~ 1eV.
    6. CMOS-compatible high-aspect ratio gate dielectrics, ferroelectrics, and gate metal deposition on 2D materials and 1D semiconducting channels.
    7. Novel gate materials for n-type work function metals (WFM).
    8. Synthesis, deposition of BEOL-compatible semiconducting oxides P and N type, dielectrics/conductors and multi-ferroics.
    9. Potential relevant new gate stack materials.
    10. CMOS-compatible epitaxial Perovskite Oxides by Metal Organic Chemical Vapor Deposition (MOCVD) for low power transistors.
    11. CMOS-compatible Epitaxial Perovskite Oxides by Molecular Beam Epitaxy (MBE) for low power transistors.
2. Interface/surface physics:
    1. Ge-based devices.
    2. 1-D/2-D channel materials.
    3. 2-D/3-D materials.
    4. 2-D/3-D contacts.
    5. 2-D material transfer process.
    6. Novel channel materials.
3. Hybrid materials with tunable properties for material hybridization at atomic level.
4. Materials and processes enabling functional diversification on CMOS platform (RF and mm-wave devices, MEMS, sensors, photonics, etc.).
5. CMOS-compatible materials and structures for heat-spreading, seeking, breakthroughs in chip-level/block-level temperature uniformity.
6. Methods to create fluid transport in features that are < 200 nm in diameter and > 1 micron deep and diameter < 10 nm and depth 200-500 um for advance nodes.

III. Back-End Processes

1. Novel ultra-low resistance interconnect materials and concepts:
    1. 2D materials for ultra-thin barrier liner materials and for low contact resistance.
    2. Alternative metals.
    3. Semi-metals.
2. Low-k dielectrics and processing for good thermal conductivity.
3. Interconnect contacts and interfaces with defect mitigation; contact resistance measurement beyond conventional transmission line measurement (TLM).
4. High mobility BEOL compatible p-type semiconductor thin films.
5. Ultrahigh-k, low leakage dielectrics with high breakdown voltage.
6. BEOL-compatible materials and structures for heat-spreading, seeking breakthroughs in chip-level / block-level temperature uniformity.
7. Oxide semiconductors integration and mechanistic study.
8. Non-volatile memory (FE, AFE, ReRAM, MRAM) integration with oxide semiconductors and 2D materials and 1D materials and mechanistic study.
9. Transparent lens material with ultra-high refractive index ($n \geq 2.0$) for CMOS image sensor.
10. Hybrid nanocomposite material with high heat dissipation and high reliability for advanced packaging.

IV. Materials and Processes for Monolithic Heterogeneous 3D Integration, Metrology, Modeling & Simulation

1. CMOS-compatible, low-thermal budget deposition and crystallization of device-quality semiconducting channel regions for high-performance devices.
2. Conformal (with and without line-of-sight) deposition of dielectrics, ferroelectrics, gate metals in high-aspect ratio channel stacks.
3. High-aspect- ratio, high-selectivity etching of with or without direct line of sight of dielectrics, metals, semiconductors, or related film stacks.
4. Methods and processes for CMOS-compatible processed/active-substrates bonding with sub 5nm. registration. Novel/alternative area selective deposition techniques:
    1. Small molecule inhibitors (SMIs).
    2. Inherently selective deposition (CVD, ALD).
    3. Selective metal deposition on semiconductors for FEOL and BEOL. Selective deposition metrology including high aspect ratio features.
5. Metrology and analytic techniques.
6. Modeling/understanding/detection/process control of critical unit processes:
    1. Methods to apply AI/machine learning to accelerate materials discovery.
    2. Modeling defects in ferroelectric and anti-ferroelectric materials.
    3. Models to improve selectivity mechanism.
7. Other materials and processes that enable 3-D monolithic heterogeneous integration, including materials and structures for heat-spreading, seeking breakthroughs in chip-level / block-level temperature uniformity.
8. Understanding and measuring the physical and chemical behavior of liquids in highly confined spaces, e.g., < 20 nm wide trenches.

9. Corrosion inhibitor wet etch and CMP chemistry on metals beyond Cu:
    1. Better atomic-scale control and understanding of corrosion inhibitors.
    2. Improvements in binding efficiency and selectivity between metals.
10. Plasma surface interactions of low-energy ions.
11. 3DI/Wafer Bonding: Alternative bonding materials and modeling/simulation

Research Needs Contributing Member Companies:

ASM International
IBM Corp.
Intel Corp.
Samsung Electronics Co. Ltd.
Siemens EDA
SK Hynix Inc.
Taiwan Semiconductor Manufacturing Company (TSMC)
Tokyo Electron Limited (TEL)
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