Nanoelectronics Research Initiative

History of the NRI Research Centers
2006 - 2012

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Overview

Introduction

This Report marks the successful conclusion of the NRI – NIST cooperative funding agreement for Phase 1.5 of the NRI Research Center program. Disbursement of funds under the NIST Award was completed on September 30, but the NRI centers continued their research with funding from the industrial sponsors until year-end 2012. Centers that had not exhausted available funding by that date had the option, under a no-cost extension, of continuing research until March 31. While the first version of this document was drafted in November of 2012, center directors have updated the summaries of key accomplishments of their centers with any important results results obtained in November 2012 through March 2013, the final period of operation of NRI Phase 1.5.

Because the end of Phase 1.5 marks an important stage in the evolution of the NRI program, this report aims to provide a brief history and summation of each center's key accomplishments over the entire period of its operation. Each center director has listed and assessed the center's most important technical accomplishments, has provided a brief statement of lessons learned, and has listed the most important publications and patents generated during the history of the center.

It is hoped that this report will serve as a resource for NRI sponsors and for directors and principle investigators of future NRI research centers.

Overview of NRI Phase 1.0 and 1.5

NRI was established in 2005 to focus research and resources on specific beyond-CMOS device concepts that could extend the "emerging technologies" of the International Technology Roadmap for Semiconductors (ITRS), particularly those areas covered in the Emerging Research Devices and Materials working groups (http://www.itrs.net/Links/2011ITRS/Home2011.htm), with the goal of sustaining the historical growth trend of the digital electronics industry. The on-going NRI collaboration with NIST is expected to stimulate research that will address long-range semiconductor research needs and identify new device technologies.

The NRI was established in 2005 with a mission to "Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe." Research was primarily aimed at the exploration of devices for logic that could show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical trends in cost and performance. While many new and exciting device concepts have been explored under the program, a clearly superior candidate for the "next switch" has not yet emerged. This increases the urgency of continuing the work, but also indicates the need to think more broadly about how to address the challenge.

NRI was created with a mission to "Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe." During Phase 1.0-1.5, the primary focus was the logic device, and the materials, fabrication processes, and the modeling, characterization and metrology needed to build and test the device.

The teams continued to pursue all the research topics necessary to produce a compelling technology demonstration for each proposed switching device.

- **Novel materials development**, growth, and characterization
- **Novel fabrication techniques**, if required
- **Physics theory and experimental verification** of key phenomena
- **Device** modeling, design, fabrication and characterization
- **Novel circuit & architecture work**

The emphasis in Phase 1.5 was on acquiring experimental evidence to support the results of the extensive theory and modeling work that took place in Phase 1.0.

Highlights of the Device Benchmarking Study

The results of these device performance benchmarking efforts are a very important outcome of Phase 1.5. At the annual NRI Benchmarking Workshop held on August 14, 2012, the results of a comprehensive assessment of Phase 1.5 device and circuit concepts were presented and discussed. Led by Dr. Ian Young and Dr. Dmitri Nikonov of Intel, the principle investigators from each of the university teams had applied a uniform and rigorous engineering methodology to the assessment. Greater consistency in base assumptions and models resulted in a better comparison among all devices for switching energy and switching speed of each device.

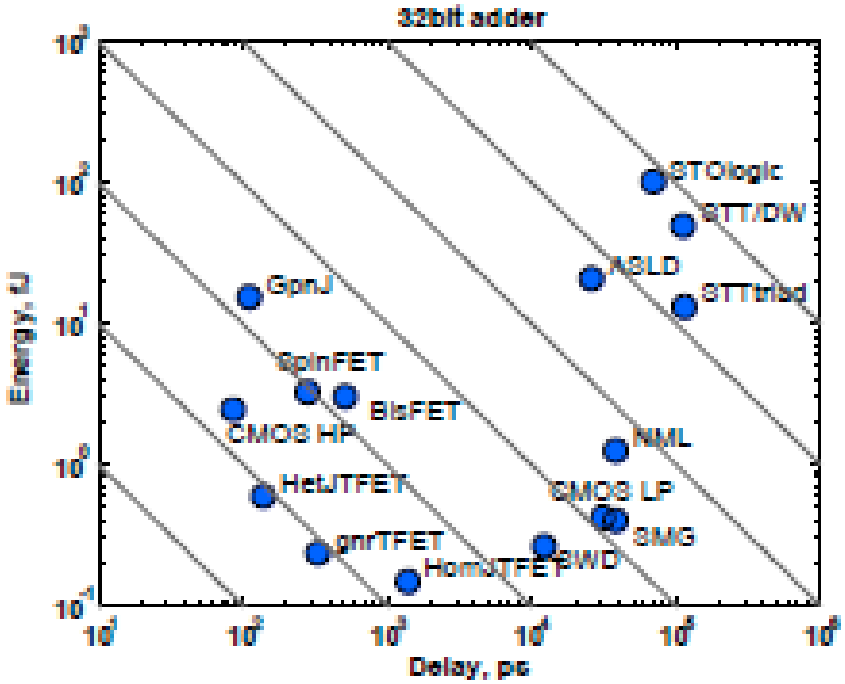

Figure 1. Switching energy vs. switching delay of 32-bit adders. In this example, magnetostrictive voltage-controlled switching is assumed for the magnetic devices (except for ASLD, STT/DW and STO logic which rely on spin torque switching.)

Figure 1 above is from the white paper of Nikonov and Young, "Overview of Beyond-CMOS Devices and A Uniform Methodology for Their Benchmarking. It plots projected switching energy versus switching delay for each NRI device concept if the device were fabricated with 15 nm generation manufacturing technology and ground

rules. Electronic devices form the group of data points on the left, all with relatively small switching delays determined by the dynamics of capacitive charging (RC delay). Nanomagnetic devices are grouped on the right with significantly longer delays determined by the slower dynamics of magnetic precession switching in achievable ferromagnetic materials. The nanomagnetic devices also exhibit a very broad range of switching energies. Those on the upper right depend on the inherently inefficient spin torque switching mechanism, while those on the lower right take advantage of the more efficient switching mechanism of voltage-controlled magnetostriction. Nikonov and Young succinctly state the most important conclusions of the benchmarking study:

1. *For electronic devices, the most promising avenue of improvement is decreasing the operational voltage. Tunneling FETs seem to be the leading option.*
2. *Spintronic devices have an advantage in implementing complex logic functions with a smaller number of devices/elements. The key factor toward making them competitive with CMOS is using voltage controlled switching.*

Nikonov and Young also point out that the benchmark circuits studied to date do not capture potential advantages of non-volatility and reconfigurability that are a characteristic of many of the magnetic devices.

NRI research results and the conclusions of this benchmarking study are strongly impacting the direction of device research both within NRI and outside of the NRI program. In electronic devices, the focus will be on new low-voltage device concepts – versions of tunnel-FETs based on new materials, or entirely new low-voltage device concepts, such as the graphene pn-junction device mentioned in the research highlights of the INDEX center. In magnetic devices, research will focus on new, more efficient mechanisms for magnetic switching, including a very efficient mechanism based on the spin-Hall effect, discussed in the highlights of the WIN center.

Looking Forward: NRI Phase 2

As Phase 1.5 of NRI has drawn to a conclusion, a great deal of effort has gone into planning and realization of Phase 2. In April of 2012 NRI responded to a NIST Federal Funding Opportunity. In the following months, each of the five NRI industrial members renewed their commitment to NRI for the 2013 – 2017, thus affirming the effectiveness of NRI in promoting university research relevant to their long-term success. With this funding commitment, a new Request for Proposals for the Nanoelectronics Research Initiative (NERC RFP #S201215), was posted on August 3, generating intense university interest.

The ground work for this solicitation had been set in discussions about the future of NRI between NRI Directors Jeffrey Welser and (beginning in July) Thomas Theis and the NRI Technical Program Group (TPG) and the NRI Governing Council (GC). NRI was created with a mission to “Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.” During Phase 1.0-1.5, the primary focus was the logic device, and the materials, fabrication processes, and the modeling, characterization and metrology needed to build and test the device. Although a clear successor the CMOS FET has not yet emerged, the performance benchmarking studies, grounded by laboratory results demonstrating the relevant device physics, suggest fruitful paths for further exploration and development – but with some modification of goals.

First, NRI research results have made it clear that any new device based on physical principles that avoid the power and performance limitations of the conventional FET, will have characteristics that are different (perhaps *very* different) from those of the FET. New circuits architectures will therefore be required to optimally express the characteristics of the new device at the system level. Phase 1.5 of NRI has thus an increasing focus on circuit architectures suited for each new device. *The consensus view of the NRI TPG and GC is that the emphasis on architectures should increase in NRI Phase 2*.

Second, the NRI TPG and GC perceived a need for a broadening of program goals beyond devices aimed purely at logic. NRI research in nanomagnetic devices has already resulted in inventions relevant to memory devices and compact radio frequency oscillators. Such possibilities were reflected in the new Request for Proposals for NRI Phase 2 which stated that *"These computation-focused technologies should include both novel device and architecture approaches to achieve low-energy, high-functionality solutions, and can include logic, memory, analog and other components."*

Third, NRI research results clearly show the value of and need for advanced metrology research. It is impossible to reproducibly build that which cannot be reproducibly measured. In the long run, advances in our ability to characterize materials and device structures will translate to advances in our ability to manufacture. Thus the new Request for Proposals stated, *"All proposals should include a strong characterization and nano-metrology component, to link between the experimental and simulation work."*

In September, NIST announced approval of an award to NRI. This new cooperative funding agreement, complimenting the financial commitments of the industrial members, allowed NRI to move confidently forward with the solicitation of new center proposals for Phase 2 of the program. NIST was a strong partner in the ensuing selection process. Selection of proposals was ompleted by the NRI TPG in December. The TPG recommendations were then taken to the NRI GC in January, 2013. With the GC's acceptance of those recommendations, contracts for the new centers are currently being negotiated with the lead universities by Semiconductor Research Corporation with start dates targeted for April 1, 2013.

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History and Accomplishments of the WIN Center

Date: 11/30/2012

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A Brief History of WIN

The Western Institute of Nanoelectronics (WIN Center) working together with its industry partners was established as the first NRI center of excellence in 2006. We were very much involved during the process of creating the Nanoelectronics Research Initiative (NRI) and I was pleased to learn that WIN then served as the model for later NRI centers. From its inception, the WIN Center took the collective wisdom and consensus of stakeholders and PIs that it should address the *key energy dissipation challenge* of scaled CMOS and explore alternative low-energy switches. We focused on spintronics, and ensured all co-PIs were razor focused on obtaining results to ascertain the feasibly of our proposed spintronic devices. We believed that magnetic spintronics (devices using *collective spins)* would operate at room temperature, in contrast with devices based on isolated spins which work mostly at low temperature. Indeed, magnetism is the only collective electron phenomenon working above room temperature. To address the objective of creating an alternative low energy device, we set a grand challenge/question for WIN Phase 1.0: *"Do spintronic device concepts provide a feasible path for information processing beyond the CMOS platform?* In doing so, we formulated three thrust areas: devices (and materials), circuits, and performance benchmarking. At that time, we clearly recognised the importance of materials; however, these were integrated into the device thrust area. From the very beginning we also realized the importance of benchmarking new device ideas against CMOS devices, circuits and systems. We are indeed very pleased that the benchmark effort was expanded to a higher NRI level, which was coordinated by Dr. Kerry Bernstein and expanded more recently by Dr. Dmitri Nikonov and Dr. Ian Young. Looking back, it is clear that our research efforts in the last 6 years have confirmed our concepts and answered positively that, "yes indeed"**,** spintronic device concepts do indeed provide a feasible path for information processing beyond-CMOS.

Phase 1.5 started on 1/31/2011 and ends on 12/31/2012. Many projects were dropped after Phase 1.0 due to the need of consolidation and, at the same time, the reduced level of funding. The current state of WIN includes 7 projects, 11 co-PIs and 20 researchers working on the four focused themes: (1) Nano Magnetic Logic, (2) Spin Waves, (3) Spin torque, and (4) Spin FET.

The areas of strength that have emerged from the research came from our discoveries of mechanisms for electric field controlled collective spin switching and modulation. These mechanisms include interface carrier modulation of magnetic phase transition and the control of interface magnetic anisotropy due to the spin orbit interaction. The discovery of voltage-controlled switching mechanisms is critical for reducing energy in magnetic devices - in line with the conclusions of the benchmarking study of Nikonov and Young, In addition, the Center is constantly on the lookout for new breakthroughs in science. As such, we plan to incorporate the newly-discovered large Spin Hall effect in metals to reduce the energy dissipation by 100X in magnetic devices based on spin torque transfer (STT) switching.

Another surprise during WIN Phase 1.5 was the coupling of STT and spin wave technologies. We demonstrated that STT could be a very efficient means to generate and detect spin wave energy and an efficient mechanism to couple from electronic to magnetic domains. This tight marriage between spin wave and STT concepts was not foreseen nor planned at the beginning of this program. The discovery arose in part through our collaboration with NIST's research programs.

Some of the most important research achievements of the Center over its entire history include:

- **Highlight 1: Discovery of Voltage control of anisotropy of the metallic magnetic layer at MgO/CoBFe:** Zhu, J., Katine, J.A., Rowlands, G.E., Chen, Y.-J., Duan, Z., Alzate, J.G., Upadhyaya, P., Langer, J., Khalili Amiri, P., Wang, K.L., and Krivorotov,

I.N., "Voltage-Induced Ferromagnetic Resonance in Magnetic Tunnel Junctions", Physical Review Letters, 108 (19): 197203/1-5. (May 9, 2012) ;

- The use of voltage control of magnetic resonance demonstrates that the anisotropy of magnetic CoBFe layer at the interface of MgO/CoBFe can be switched at the GHz range of ferromagnetic resonance. This result derived from the collaboration between UCLA/UCI and our infrastructure partners at Singular and Hitachi USA. This work lays down the foundation for many different voltage controlled devices. This work also enables the spin wave and nanomagnetic logic devices low energy operation using voltage control.

- **Highlight 2: Demonstration of electric field control of Ge DMS dots at room temperature:** **(citations to Date = 45**) Xiu, F.; Wang, Y.; Kim, J.; Hong, A.; Tang, J.; Jacob, A. P.; Zou, J.; Wang, K. L., Electric-field-controlled ferromagnetism in high-Curie-temperature Mn0. 05Ge0. 95 quantum dots. Nature materials 2010, 9 (4), 337-344;
  - Demonstration of successful synthesis of self-assembled dilute magnetic Mn0.05Ge0.95 quantum dots with ferromagnetic order above room temperature. This achievement showed that the approach to SpinFET Ge is sound if the correct phase of MnGe is employed. This result help catalyze the approach towards nanowire SpinFET. It illustrated the ability to use the gate control to control phase transition at room temperature for spin gain transistor or transpinor.

- **Highlight 3: Low energy spin transfer torque** **(citations to Date = 20)** *Ghao, H.; Lyle, A.; Zhang, Y.; Amiri, P.; Rowlands, G.; Zeng, Z.; Katine, J.; Jiang, H.; Galatsis, K.; Wang, K., Low writing energy and sub nanosecond spin torque transfer switching of in-plane magnetic tunnel junction for spin torque transfer random access memory. Journal of Applied Physics 2011, 109 (7), 07C720-07C720-3.*
  - The emergence of the DARPA STTRAM catalyzed by WIN was important as many new resources were available to the WIN program. The demonstration of very fast switching of STT devices was one such derived benefit. Using in-plane MgO-based magnetic tunnel junctions (MTJs) ultra-fast spin torque transfer (STT) switching was also observed in this sample at 580 ps showing that in-plane MgO MTJs are still a viable candidate as the fast memory cell for STT-RAM. Furthermore, such speed is necessary for spin wave detection and generation.

- **Highlight 4: Coupling of antiferromagnetic and ferroelectric order to achieve a high magneto-electric effect** **(citations to Date = 73)** Wu, S.; Cybart, S. A.; Yu, P.; Rossell, M.; Zhang, J.; Ramesh, R.; Dynes, R., Reversible electric control of exchange bias in a multiferroic field-effect device. Nature materials 2010, 9 (9), 756-761.
  - This achievement showed that instead of using direct coupling between ferroelectric and ferromagnetic order parameters in a single-phase multiferroic material, which only shows a weak magnetoelectric effect, a unique method using indirect coupling through an intermediate antiferromagnetic order parameter can be used. This was an important demonstration towards controlling magnetization with electric fields.

- **Highlight 5: Demonstrating Nano magnetic logic's stability and switching** **(citations to Date = 61)** Carlton, D. B.; Emley, N. C.; Tuchfeld, E.; Bokor, J., Simulation studies of nanomagnet-based logic architecture. Nano Letters 2008, 8 (12), 4173-4178.
  - Our team has been at the forefront of NML. Since this paper, various demonstrations of NML have preceded within WIN including, thermally assisted switching, PEEM analysis, configurational anisotropy "concave" magnet shape, and cascade dynamics.

In addition to these research highlights, we have learned some important technical lessons during Phase 1.5.

- Focus on voltage control of magnetism for low energy operation. Supported by fundamental reasoning, this approach led to the discovery and demonstration of

such mechanisms, critical for enabling new low-dissipation devices. Without the synergistic effort of teams having complementary expertise and infrastructure, the discovery process would have been much delayed or impossible.

- o Complex magnetic material patterning: patterning STT pillars side by side proved to be very difficult. The use of new metal materials, a thin oxide and precision patterning requirements led to an extremely difficult process in demonstrating coupled STT oscillators. Experienced team members were the key for the demonstration of the STT oscillator arrays.
- o Stay focused on the principles leading to room temperature operation. Initially, many single-spin device ideas as well as interconnect concepts were attractive and thus were given the benefit of doubt. Most of these ideas were deemed to be beyond the NRI horizon given the time and resources required to develop materials and structures for room temperature optimization. In some instances, however, new discoveries might emerge, and we need to lookout for them as in the case of the Spin Hall effect discussed above.
- o Program Leverage and Efficiency: In developing new device ideas, much time and funding needed to be directed towards fabrication. Leverageing programs such as DARPA STT and NVL, the WIN program was able to fabricate many test devices and to verify the concepts -- for instance, STO oscillators (Krivorotov and Jiang) and spin wave transport studies (Wang and Khitun).

The WIN Center has been running smoothly in terms of program management, interfacing with sponsors and co-PIs as well as working with NRI. The value of having an experienced team working with Semiconductor Research Corporation has been evident to all stakeholders. Partnering with a Focus Center Research Program (FCRP) center's administration in the same location helped our administrative team be more cost effective in day-to-day operation. During Phase 1, the administrative burden was at its peak due to the natural “start-up” activity along with the increased funding under UC Discovery, particularly the equipment matching portion that required many “checks and balances” in order to fulfil the “cash matching portion”. Human resource assistance from Intel helped alleviate this burden (kudos to Intel employees Y.Botros, A. Jacob, G.Dao and G.Bourianoff, T.Komer). Drs. Youssry Botros and Ajey Jacob were particularly helpful in coordinating the program and integrating different projects. The NRI interface with WIN has also been seamless, much to the credit of NRI staff members such as Allison Hilbert. In administrating the Center, I have been most fortunate in having recruited talented people: Kos Galatsis, Katie Christensen (WIN), Katie Wilson (WIN) and Nevin Gabr (WIN). Monthly operational meetings are well run and very useful in disseminating operational information. Invoicing systems are very manageable thanks to the standard SRC process and experienced administrative team. While the WIN annual review attendance has declined in recent years as the program was reduced form 20 PIs in Phase 1.0 to 9 PIs in Phase 1.5, these events have been well executed. The NRI annual reviews have been effective in disseminating information across the various NRI research initiatives, stimulating cross-center collaborations such as those with Prof. Vincent LaBella (Albany), Mark Rodwell (UCSB), JP Wang (Minnesota), A. Balandin (UC Riverside), Phil Kim (Columbia) and others.

In conclusion, we are grateful to the NRI Directors (Jeff Welser and Tom Theis), the industry sponsors and NIST as well as the hands-on assignees from sponsors that worked hand-in-hand with our principal investigators and students. Last but not least, I thank our academic supporters, principal investigators, researchers and students. Thank you immensely. It has been a pleasure working and collaborating with you all.

Kang L. Wang
Director of WIN

PUBLICATIONS AND PATENTS

Top 5-10 Journal Publications for the Duration of the Center's Operation

Need from Kang

Important Invention Disclosures for the Duration of the Center's Operation

Need from Kang

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History and Accomplishments of the MIND Center

Date: November 30, 2012

A Brief History of MIND

The Midwest Institute for Nanoelectronics Discovery (MIND) was announced on March 26, 2008, at Notre Dame with backing and support of the Semiconductor Research Corporation, the National Institute of Standards and Technology (NIST), the State of Indiana, the City of South Bend, and the University of Notre Dame. The founding universities were Notre Dame, Penn State, Purdue, Illinois, Michigan, and UT Dallas. The total research investment was approximately $20M. As important as this funding was in launching MIND, the center benefited from the collective support of IBM, the University of Notre Dame, bipartisan support in Indianapolis, and leadership in the City of South Bend, which used MIND as an example of a productive university/industry collaboration with the aim of job creation. The economic development leaders in South Bend and Elkhart were consistent supporters of MIND through the five year period of the center.

In 2008 MIND became the fourth center in the Nanoelectronics Research Initiative (NRI), adding tunnel field-effect transistors (TFETs), nanomagnet logic (NML) technology, and explorations in plasmonics, graphene spin FETs, and thermal devices to the widening suite of devices under exploration in the NRI. To better understand and compare the NRI emerging device technologies, MIND proposed and initiated a benchmarking activity, which has been refined in each year to help guide and gauge the relative merits of the devices under development across the NRI. This effort was led by Kerry Bernstein of IBM Research, who was able to win support for the benchmarking effort across all of the centers. MIND also set as a task the exploration of new architectures to utilize NRI device technologies and again, led by Kerry Bernstein, ran architecture workshops in the early years to stimulate researchers to think broadly about the ways to use non-charge-based technologies. MIND held four architecture and benchmarking workshops on the day before the MIND annual review each year to stimulate consideration of new ways to utilize NRI technologies for computation.

MIND benefited significantly from collaborations with NIST, Argonne National Laboratory, and the National High Magnetic Field Laboratory. A MIND postdoc, Qin Zhang, from Notre Dame worked at NIST in Gaithersburg for three years on graphene and III-V TFET metrology. This was a highly productive collaboration with NIST, resulting in 10 journal publications and 15 conference papers. The internal photoemission (IPE) measurement system of Nhan Nguyen, NIST, was utilized extensively in TFET transistor development to determine the flat band voltage and band alignments in graphene and III-V TFETs. NIST has also hosted graduate students from Purdue, Penn State, and Notre Dame for extended stays to utilize the IPE measurement capability and for pulsed current-voltage measurements. MIND students made trips to Argonne to utilize their x-ray photoemission electron microscope for imaging nanomagnets, and to the National High Magnetic Field Laboratory for magnetotransport measurements

Since March of 2008, MIND through October of 2012 MIND researchers generated 496 publications, including journal and conference papers. In 55 months, this is an average of approximately 9 publications per month over the duration of the center or about two publications per week. This is for a research team that averaged about 65 researchers including 21 faculty, plus post docs and graduate students. IBM provided an assignee to the center over most of the duration of the center. MIND researchers filed for four patents relating to nanomagnet logic, TFETs, and teraherz modulators. One patent on nanomagnet logic and one on tunnel FETs issued with two pending.

In 2011, the NRI centers were asked to recompete and focus on one or two devices. In consultation with the industry mentors, MIND focused resources on TFET and NML technologies and dropped work on plasmonics, thermal logic, and graphene spin-based devices. The technologies that were dropped were not been successful in identifying a clear and compelling basis for a logic technology. The primary objective in MIND phase 1.5 has been to systematically explore TFET and NML technologies and produce experimental data to enable a quantitative assessment of the performance of both technologies for scaling beyond the limits of CMOS. For the TFET, the goal was set to demonstrate device technology to meet the theoretical predictions for low subthreshold swing, high on-current, and low off-current, at sub-half-volt supply voltages. For NML, the goal was to demonstrate logic circuits that enable evaluation of the low-power performance potential of the technology. Since NML is well suited to systolic architectures, the focus of the technology development has been toward clocked systems.

Most significant research achievements of the Center over its history

III-V tunnel FETs. Prior to MIND, there were no demonstrations of tunnel FETs in III-V materials, and the results in group IV materials were not clear (the junctions were just not abrupt enough to show negative differential resistance in the forward bias direction). The first demonstration of the III-V TFET

was achieved by Penn State in 2009 using a *p-i-n* InGaAs homojunction utilizing a sidewall gate, with gate field oriented obliquely to the current direction (Mookerjea et al. IEDM 2009). This was followed by a study of the temperature dependence (Mookerjea et al. *EDL* 31 2010) and steady improvements in on-current with the introduction of heterojunctions (Mohata, IEDM 2011, *Appl. Phys. Exp.* 4 2011, Bijesh VLSI Symp. 2012). Purdue proposed a geometry with gate field oriented in-line with the current direction (Klimeck patent filed 2010, Agarwal et al. *EDL* 31 2010), and Notre Dame proposed III-V embodiments (Seabaugh et al. patent filed 2011), which were then demonstrated (Li et al. *EDL* 33 2012, Zhou et al. *EDL* 33 2012, etc.). Record current density in III-V TFETs now stands at 180 µA/µm at 0.5 V (Zhou et al. IEDM 2012), but similar currents are also obtained in the sidewall gate TFET by Penn State. The first *p*-channel TFETs have just recently been demonstrated at Penn State. Scaling has also been pushed in MIND using the nanoassembly process of Penn State (Morrow et al. *Science* 323 2009) and device fabrication approach from the same laboratory (Ho et al. *Nano Lett.* 8, 2008). In collaboration with Bob Wallace, understanding of best practices for gate surface preparation, passivation, and leakage reduction have been steadily advancing. Analytic modeling in MIND now shows that the drive to higher on-current must be traded off against off-current and that there is an optimum bandgap for a given supply voltage, on-current, and off-current (Zhang et al. DRC 2012 late news).

Graphene TFETs and beyond. Several of the most highly cited papers in MIND have been written under this task. *The* most highly cited paper (Fang et al. *PRB* 78 2008) models transport in graphene nanoribbons, comparing the effects of phonon, impurity, and line-edge roughness scattering with application to improving mobility. A paper entitled "Graphene nanoribbon tunnel transistors" is the second most highly cited paper in MIND (Zhang et al. *EDL* 29 2008). This paper shows that graphene nanoribbon TFETs can simultaneously achieve both high speed and low power dissipation. The graphene TFET task also has many experimental highlights, including demonstration of a wafer scale fabrication process for graphene (Tahy et al. DRC 2011), process techniques for forming 10 nm nanoribbons (Hwang et al. *JVST B* 30 2012), demonstration of the opening of a bandgap (Hwang et al. *Appl. Phys. Lett.* 100 2012), and record on-current of 10 mA/µm in nanoribbon FETs (Hwang, ISCS 2012). This year, *p-n* junctions have been demonstrated using side gates and ion doping in nanoribbon TFETs with the observation of negative differential resistance at room temperature. It has also been shown theoretically that the symmetric bandstructure of graphene enables a new kind of switch based on tunneling between graphene bilayers (Feenstra et al. *J. Appl. Phys.* 111 2012). A transistor based on this junction phenomena has been invented which should exhibit both negative resistance and negative transconductance (Zhao et al. DRC 2012). Two-dimensional (2D) crystal materials have also been explored. These materials allow development of TFETs without the need to form nanoribbons to open a bandgap; 2D crystal FETs have also been demonstrated in WS_2 (Hwang et al. *Appl. Phys. Lett.* 101 2012) and $MoTe_2$.

Atomistic device modeling. Modeling insights on TFET leakage paths and experimental realities such as growth capabilities and graphene line-edge roughness drove atomistic device modeling within OMEN/NEMO5 to incorporate new capabilities. These new capabilities were built under funding leveraged from NSF and explored under MIND funding. This led to a new tool set that can analyze complex geometries such as layered lateral devices that suppress leakage and optimize current on/off ratios. The modeling capabilities go far beyond standard commercial TCAD and are foundationally implemented in a new community code NEMO5. This new code is now in use at Intel, GLOBALFOUNDRIES, IBM, Samsung, and Lockheed Martin.

Nanomagnet logic. Following demonstrations of the fundamental building blocks for NML circuits, Notre Dame (ND) has concentrated on the dynamic properties of nanomagnets, ways to read, write, and clock NML structures, and suitable architectures for this technology. Clock designs were devised that enabled the local control of NML ensembles, and still led to "wins" over transistor-based hardware with respect to energy. These designs were then experimentally demonstrated, and used to locally control NML devices (Alam et al. TNANO 2010), Boolean logic gates, and interconnect (Alam et al. TNANO 2012). As the need for clocking impacts dataflow, *i.e.,* it creates inherent pipelines, application-level architectures were identified such that information processing tasks, *e.g.,* pattern matching for "big data," could be accomplished efficiently (Niemier et al, CNNA 2012). State-of-the-art transistor-based equivalents were also designed and benchmarked. Specific outcomes from this effort include (i) revised clock designs, and (ii) proposals for enhanced permeability dielectrics to further minimize clock energy. Notably, this later work seeded experimental work that suggests that clock energy can be reduced by as much as 30x (Li et al. *IEEE Trans. Magnetics* 48, 2012).

Any new technology based on alternative state variables should be able to interface with charge-based devices in an efficient manner. Toward this end, four candidate output structures were

considered to move information from the magnetic domain back to the electrical domain (Liu et al., TNANO 2011). The same clock structures can also be used to properly set the state of an output device. The Notre Dame design targets were fabricated at IBM via a DARPA-funded collaboration. Electrical input structures were also developed and successfully tested at ND.

Finally, ND also: (i) employed micromagnetic simulations to design circuits that enable more complex and efficient computer architectures *e.g.,* reduced area gates (Niemier et al., US Patent No. 8,058,906), fanout, and wire crossings, (ii) considered how clocking could impact nonvolatility (Dingler et al. DAC 2012), (iii) studied how fabrication variations impact logic correctness and clock energy, and (iv) fabricated and successfully tested full adder structures (Varga et al. Intermag/MMM 2013). The Varga accomplishment appears to be the first demonstration of concatenated gates using spin-based devices.

Future directions

Steeper transistors. Steeper transistor slopes and lower voltages should be possible in 2D materials like graphene and dichalcogenide crystals because of self-passivated surfaces and excellent electrostatics. The symmetric band structure enables complementary operation and atomically thin dimensions beyond the limits of scaling of any FET. The III-Nitrides allow the incorporation of piezoelectricity and spontaneous polarization into the design of steep transistors. Complex oxide heterostructures supporting an atomically abrupt and super-high-density 2D electron gas offering a further intriguing platform for low-voltage steep transistors.

Atomistic device modeling. The emergence of new materials to be explored in tunneling transistors such as III-Nitrides, 2D materials, and complex oxides is driving new modeling requirements. The material properties are barely known and need to be explored via experiment and *ab initio* materials models. Subsequently, this foundational data must be mapped into atomistic tight-binding that can scale to realistic device sizes via NEMO5. Ongoing and future NEMO5 endeavors embrace the foundational *ab initio* mapping to tight binding. Furthermore, the relative importance of scattering mechanisms must be examined as well as the interactions between collective phenomena such as piezoelectric responses to local charge densities.

Nanomagnet logic. The research directions for NML should be expanded to include devices with perpendicular magnetic anisotropy (PMA) that are clocked with electric fields. NML devices with PMA (pNML) are especially advantageous when considering system architectures: (1) Provided inputs do not change, the potential for data races associated with different signal arrival times at an in-plane NML gate can be eliminated in pNML circuits. (2) pNML devices always couple antiferromagnetically to neighboring devices, and can be resized such that neighboring devices have different footprints. This reduces the complexity of local signal routing. pNML wire crossings have been realized. (3) With pNML, focused ion beam (FIB) irradiation can define dataflow directionality *without* the multiphase clock schemes that are required for in-plane NML. This also enables fine-grained pipelining and higher throughputs. (4) pNML opens the door to multiple layers of metallic devices that couple in a third dimension. This not only reduces circuit area but can also increase device-to-device coupling (which will reduce error rates), and provides the ability to create circuits with high fan-in. Focus on the design of pNML-based Boolean and non-Boolean logic appears promising. Particular attention should be given to efficient interconnect where propagating domain walls seem promising. Stochastic computing architectures could enable useful information processing hardware using these devices.

Alan Seabaugh
Director of MIND

PUBLICATIONS AND PATENTS

Top 5-10 Journal Publications for the Duration of the Center's Operation

Top 11 journal publications in MIND (according to Web of Science)

1. Mobility in semiconducting graphene nanoribbons: Phonon, impurity, and edge roughness scattering
Author(s): Fang Tian; Konar Aniruddha; Xing Huili; Jena Debdeep
Source: PHYSICAL REVIEW B Volume: **78** Issue: **20** Article Number: **205403** DOI: **10.1103/PhysRevB.78.205403** Published: **NOV 2008** Times Cited: **62** (from All Databases)

2. Graphene Nanoribbon Tunnel Transistors
Author(s): Zhang Qin; Fang Tian; Xing Huili; Seabaugh Alan; Jena Debdeep
Source: IEEE ELECTRON DEVICE LETTERS Volume: **29** Issue: **12** Pages: **1344-1346** DOI: **10.1109/LED.2008.2005650** Published: **DEC 2008** Times Cited: **53** (from All Databases)

3. Programmed Assembly of DNA-Coated Nanowire Devices
Author(s): Morrow Thomas J.; Li Mingwei; Kim Jaekyun; Mayer Theresa; Keating CD
Source: SCIENCE Volume: **323** Issue: **5912** Pages: **352-352** DOI: **10.1126/science.1165921** Published: **JAN 16 2009** Times Cited: **48** (from All Databases)

4. Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors
Author(s): Luisier Mathieu; Klimeck Gerhard
Source: IEEE ELECTRON DEVICE LETTERS Volume: **30** Issue: **6** Pages: **602-604** DOI: **10.1109/LED.2009.2020442** Published: **JUN 2009** Times Cited: **34** (from All Databases)

5. Atomistic Full-Band Simulations of Silicon Nanowire Transistors: Effects of Electron-Phonon Scattering
Author(s): Luisier Mathieu; Klimeck Gerhard
Source: PHYSICAL REVIEW B Volume: **80** Issue: **15** Article Number: **155430** DOI: **10.1103/PhysRevB.80.155430** Published: **OCT 2009** Times Cited: **33** (from All Databases)

6. Ultrafast Transient Absorption Microscopy Studies of Carrier Dynamics in Epitaxial Graphene
Author(s): Huang Libai; Hartland Gregory V.; Chu Li-Qiang; Luxmi; Feenstra R. Lian Chuanxin, Tahy Kristof, Xing Grace
Source: NANO LETTERS Volume: **10** Issue: **4** Pages: **1308-1313** DOI: **10.1021/nl904106t** Published: **APR 2010** Times Cited: **31** (from All Databases)

7. Effect of high-kappa gate dielectrics on charge transport in graphene-based field effect transistors_
Author(s): Konar Aniruddha; Fang Tian; Jena Debdeep
Source: PHYSICAL REVIEW B Volume: **82** Issue: **11** Article Number: **115452** DOI: **10.1103/PhysRevB.82.115452** Published: **SEP 29 2010** Times Cited: **25** (from All Databases)

8. Zener tunneling in semiconducting nanotube and graphene nanoribbon p-n junctions _
Author(s): Jena Debdeep; Fang Tian; Zhang Qin; Xing Huili
Source: APPLIED PHYSICS LETTERS Volume: **93** Issue: **11** Article Number: **112106** DOI: **10.1063/1.2983744** Published: **SEP 15 2008** Times Cited: **24** (from All Databases)

9. Low-Voltage Tunnel Transistors for Beyond CMOS Logic
Author(s): Seabaugh Alan C.; Zhang Qin
Source: PROCEEDINGS OF THE IEEE Volume: **98** Issue: **12** Pages: **2095-2110** DOI: **10.1109/JPROC.2010.2070470** Published: **DEC 2010** Times Cited: **24** (from All Databases)

10. In Situ Axially Doped n-Channel Silicon Nanowire Field-Effect Transistors
Author(s): Ho Tsung-ta; Wang Yanfeng; Eichfeld Sarah; Lew Kok-Keong; Liu Bangzhi; Mohney Suzanne; Redwing Joan; Mayer Theresa Source: NANO LETTERS Volume: **8** Issue: **12** Pages: **4359-4364** DOI: **10.1021/nl8022059** Published: **DEC 2008** Times Cited: **22** (from All Databases)

11. On-Chip Clocking for Nanomagnet Logic Devices_
Author(s): Alam Tanvir; Siddiq Jafar; Bernstein Gary H.; Niemier Michael; Porod Wolfgang; Hu Sharon
Source: IEEE TRANSACTIONS ON NANOTECHNOLOGY Volume: **9** Issue: **3** Pages: **348-351** DOI: **10.1109/TNANO.2010.2041248** Published: **MAY 2010** Times Cited: **20** (from All Databases)

Important Invention Disclosures for the Duration of the Center's Operation

Summary patent filings for MIND

Non-majority MQCA Magnetic Logic Gates and Arrays based on Misaligned Magnetic Islands
Inventors: Mike Niemier, Gary Bernstein, Wolfgang Porod
Patent no. US 8,058,906
Issued November 2011

Tunneling Field-Effect Transistor with Low Leakage Current
Inventors: Mathieu Luisier, Samarth Agarwal, Gerhard Klimeck
Patent no. US 8,309,989 B2
Issued November 2012

Improved Lateral g-FET Design
Inventors: Gerhard Klimeck
Utility patent filed September 2010

Low Voltage Tunnel Field-Effect Transistor (TFET) and Method of Making Same
Inventors: Alan Seabaugh, Patrick Fay, Huili Xing, Yeqing Lu, Guangle Zhou, Mark Wistey, Siyuranga Koswatta
Utility patent filed August 2011

Method and Apparatus for Terahertz Wave Amplitude Modulation
Inventors: Berardi Sensale-Rodriguez, Rusen Yan, Michelle Kelly, Tian Fang, Debdeep Jena, Lei Liu, Huili Xing
Utility patent filed June 2012

Summary invention disclosures pending

Structure and Process for Multiple-Conductor Wrap-Around-Gate Field Effect Transistors with Channel Dimensions Set by Epitaxial Growth
Inventors: Mark Wistey, Mark Rodwell, Yaacov Doron, Cohen Elias, Andrew Carter
Disclosure filed June 2012 – transferred to Nonclassical CMOS Center

Single Transistor Random Access Memory Using Ion Storage In 2D Crystals
Inventors: Alan Seabaugh, Susan Fullerton
Disclosure filed September 2012

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History and Accomplishments of the SWAN Center

Date: November 30, 2012

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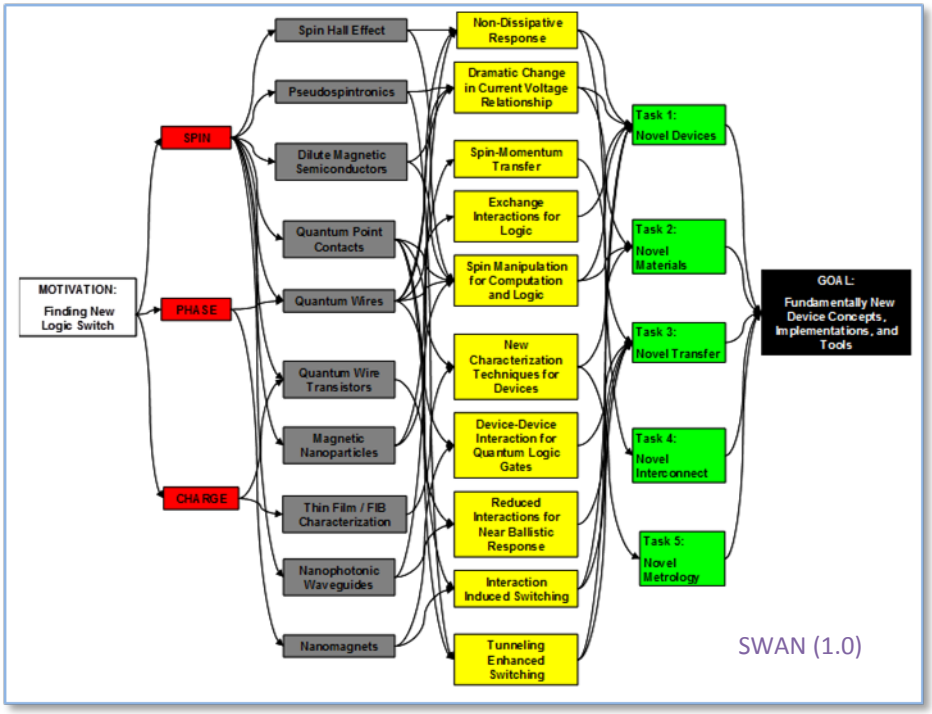
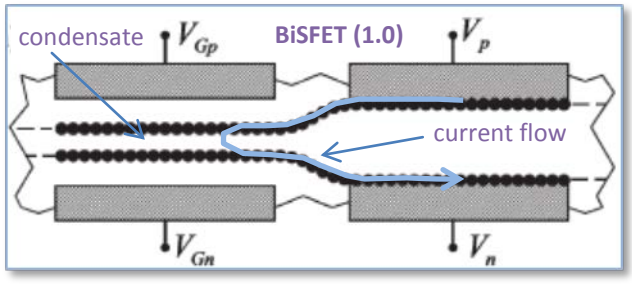
NRI anoelectronics RESEARCH INITIATIVE

A Brief History of SWAN

The South West Academy of Nanoelectronics (SWAN) was founded in 2006 as the third NRI center, headquartered at the University of Texas at Austin, with partner institutions at the University of Texas at Dallas, Texas A&M, Rice, Arizona State, Maryland and Notre Dame. The research was organized into five themes with a heavy emphasis on theory because SWAN wanted to widely explore device opportunities based on novel computational state variables, such as spin and wave-function phase, as well as on novel charge-based switching mechanisms.

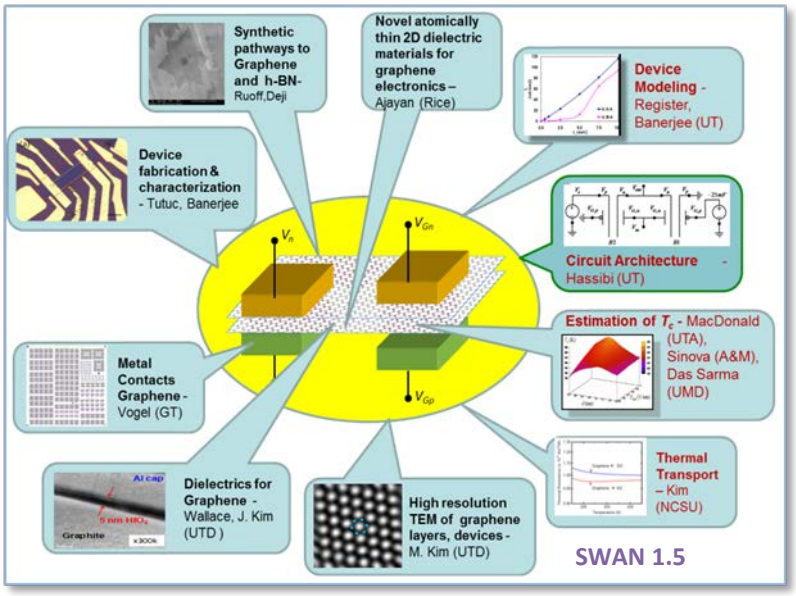


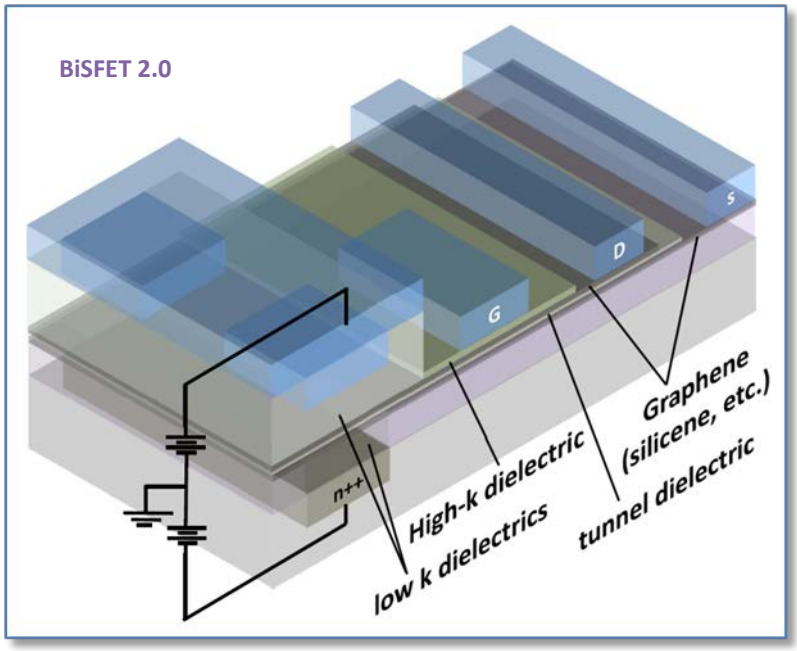
Under Theme 1 which addressed logic devices based on new computational state variables, we explored ideas based on the spin Hall effect, strongly correlated quantum wires, quantum interference, graphene's novel properties, and pseudospintronics, where "pseudospin" refers to the state of two-state quantum systems, analogous to spin up and down. In 2008, many of the concepts came together in the form of the now patented (Banerjee, Register, Tutuc, Reddy and Macdonald, U.S. Patent 8,188,460, 2012), potentially ultra-low power Bilayer Pseudospin Field Effect Transistor (BiSFET) concept based on excitonic-condensate-enhanced charge tunneling (exciton recombination) between two graphene layers. Here, pseudospin refers to the "which layer" of graphene degree of freedom of the many-body wave-function. Prior to the genesis of SWAN, pseudospintronic superfluid exciton condensates had been experimentally reported in III-V GaAs-AlGaAs bilayer systems, but unfortunately only at very low temperatures and high magnetic fields in the quantum Hall regime. However, work by Allan MacDonald's group in SWAN suggested that graphene double layers could be a much more attractive platform for seeing such effects, perhaps allowing condensation at room temperature absent magnetic fields and, thus, making it amenable to NRI goals. The BiSFET concept makes use of a negative-differential resistance (NDR) characteristic, much like that of superconducting Josephson junctions, with an engineerable and gateable low-voltage NDR onset. Initial device and circuit simulations suggested switching energies on the scale of 10 zeptojoules ($10^{\bullet 2}$ attojoules), orders of magnitude below even end of the roadmap CMOS.



The work in Theme 2 had a materials flavor, and focused on studying the magnetic and transport properties of diluted magnetic semiconductors, studies of current-induced magnetization dynamics, new nano-magnet based quantum cellular automata (MQCA) at Notre Dame, including clocking schemes, and Mn doped Si magnetic nanoparticles. In Theme 3 on nanoscale thermal management, the goal was to understand and, where possible, minimize the detrimental effects of phonon scattering in nanoscale devices. When considering "phasetronic" devices where quantum mechanical phase-interference is a principle of operation, the degree of phonon-induced phase-breaking is key. In Theme 4, colleagues at Rice University focused on developing nanoscale plasmonic interconnects with lower loss than optical interconnects, yet much faster than conventional electrical interconnects. Finally, in Theme 5, colleagues at the University of Texas at Dallas established baseline capabilities in nanometrology, including advanced TEM capabilities to support all the device efforts.

SWAN phased out several programs in 2009 because they were not closely aligned with the evolving NRI SWAN mission, even though the PI's had been very productive in terms of publications, and focused our efforts toward the BiSFET. For example, the MQCA effort at Notre Dame was transferred to MIND in its entirety, and the nanoplasmonics work at Rice was phased out due to limited connectivity to other SWAN efforts, while they were encouraged to engage with the MARCO Interconnect Focus Center. The band-to-band tunnel FET work of Register and Banergee's groups was set aside in deference to MIND's efforts in this area, as were spintronic efforts in the Sinova and Tutuc groups, in deference to WIN.





The current SWAN 1.5 program started in 2011 and has 10 Themes focused primarily on the BiSFET and related 2D-to-2D bare tunneling device concepts. We beefed up our experimental efforts toward device demonstration, added circuit design and architecture expertise, and put resources towards a better theoretical understanding of the condensate temperature and dielectric dependencies.

The BiSFET demonstration effort is strongly supported by four experimental themes devoted to key device requirements. Ruoff's group at UT-Austin has improved the process recipes for growth of large domain (~700 micron) high quality graphene and hBN via thermal CVD on copper substrates, and grown clean monolayer graphene using solid precursors. In a strong collaborative effort facilitated by Luigi Colombo, the CVD graphene growth process was transferred from the Ruoff group to the Wallace group at UT-Dallas. Understanding of key factors impacting the CVD graphene quality after the transfer process was obtained by Wallace and Vogel, including the detrimental effects of Polymer residues and moisture. Wallace is now providing clean graphene samples to the UT Austin device groups, and has transferred the graphene cleaning recipe to all NRI centers.

Improvements in our theoretical understanding of screening under SWAN 1.5 has not only further emphasized the need for low-k dielectrics, but indicated that there is a first-order transition in terms of the allowed dielectric constant, beneath which significant condensation at any temperature is unlikely to occur. That evolving understanding has led to both a redirection of the experimental efforts and a basic redesign of the BiSFET itself. Still, device modelling and circuit simulations continue to indicate that switching energies on the scale of 10 of zeptjoules should be possible if the BiSFET can be realized.

Highlights

The overall metrics of SWAN since its inception in 2006 are impressive. It has supported over 90 students supervised by 37 faculty members, and has leveraged the efforts of 7 industrial mentors at 11 universities. 25 of these students have graduated under SWAN, of which 11 work at NRI member companies, 6 in academia and 2 in government research labs including NIST. The work distributed over 15 Research Themes in all has led to 445 publications, including over 200 highly cited papers in

top tier journals such as Science, Nature, Physical Review Letters, Physical Review B, IEEE Electron Device Letters, and IEEE Transactions on Electron Devices. Five patents have been filed through NRI, three of which have already been granted.

***Highlight #1**:* In 2008, S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy and A. Macdonald proposed the now patented (United States Patent 8188460, 2012) Bilayer pseudo-Spin FET (BiSFET), as first reported in IEEE Electron Device Letters, Feb. 2009; (57 citations). Switching energies were predicted• and still are predicted• to be on the scale of 10 zeptojoules ($10^{\bullet 2}$ attojoules) if the BiSFET can be realized. This novel device concept, along with possible derivatives such as 2D-to-2D TFETs, became the focus for a synergistic experimental and theoretical effort. The theoretical effort ranged from advances in basic many body theory led by MacDonald trough device modeling to SPICE level logic circuit design led by Register, the latter beginning prior to the NRI-wide benchmarking effort led by Gary Bernstein. The experimental effort, detailed further below, included advances in relevant materials science of graphene CVD growth, unit process development of compatible gate dielectrics, and metrology involving Coulomb drag measurements in this novel system. Regardless of the ultimate viability of the BiSFET, these collateral benefits alone arguably have made the SWAN effort worthwhile.

Highlight #2: Register and Banerjee developed two other transistor concepts based on tunnelling. One, the "Resonant-injection-enhanced Field-Effect Transistor" (RIEFET) employs quantum interference effects in tandem with conventional gate control to increase subthreshold slope to allow lower voltage operation with still acceptable ON/OFF ratios [United States Patent 8,008,649, 2011]. The other, a novel band-to-band tunnel FET concept dubbed the HetTFET, uses a staggered broken-gap voltage-independent hetero-tunnel-barrier for super-steep subthreshold slopes and low power [IEEE EDL **32**, 743, 2011].

***Highlight #3*:** Atomic layer deposition (ALD) of dielectrics is challenging on graphene because of its inert surface and sp^2 bonding. Luigi Colombo, SWAN mentor from TI, in collaboration with Tutuc and Banerjee, patented and published a novel method for ALD high-k gate dielectric growth on graphene using a sputtered Al or Ti layer that is easily oxidized that can seed ALD. [United States Patent 8,198,707, 2012, "Establishing a uniformly thin dielectric layer on graphene in a semiconductor device without affecting the properties of graphene."] The associated paper in Applied Physics Letters has over 100 citations.

Highlight #4: Ruoff and Colombo successfully led an effort in preparation of large-area, high quality graphene on Cu foils, with Tutuc and Banerjee demonstrating high field effect mobility in these films. This has become the *de facto* standard method of large area CVD graphene. This work was reported in "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," X.Li, Cai, An, Kim, Nah, Yang, Piner, Velamakanni, Jung, Emanuel Tutuc, Sanjay K. Banerjee, Luigi Colombo, Rodney S. Ruoff, Science, 2009, which has garnered **1650 citations**.

Highlight #5: Tutuc led the efforts on the first measurements of Coulomb drag in double layer graphene, as reported in "Coulomb drag of massless fermions in graphene," Kim S, Jo, Nah, Yao, Banerjee, Tutuc, PRB Rapid Comm. **83**, 2011. Condensation is expected to lead to a dramatic increase in Coulomb drag. Although, based on recent theory, we now believe that condensation in the considered system was not possible, the intrinsic value of the work independent of such considerations led the Editors of Physical Review B to choose this work as an **Editor's Choice paper**.

Technical Lessons and Future Directions

Understanding the conditions under which the condensate can form is essential to BiSFET concept and design. There is no quantitatively precise theory of superfluid formation, and of necessity the theory of superfluid condensation in bilayer systems in particular has been substantially advanced by the work of SWAN. Indeed, recent basic experimental work elsewhere on such condensates in III-V systems at ultra-low temperatures [Nandi & Eisenstein, Nature, 2012] have called upon theory developed under SWAN by MacDonald to explain their biasing-scheme-dependent super currents. One consequence of that improving theory has been making a proverbial moving target of the apparent experimental conditions for condensate realization. Experience with CMOS teaches us that high-k dielectrics are preferable. However, we learned that low-k dielectrics were preferable for condensate formation. Even then, however, it was still expected that sub-room temperature condensation might be created in high-quality systems with higher than optimal dielectric constants to test the basic theory, while lower-k dielectrics were brought online. However improvement in our theoretical understanding of screening under SWAN 1.5 has not only further emphasized the need for low-k dielectrics, but indicated that there is a first-order transition in terms of the allowed dielectric constant beyond which significant condensation is unlikely to occur at any temperature.

That evolving understanding, however, has now led to both a re-focusing of our experimental efforts and a basic redesign of the BiSFET itself as illustrated above. Moreover, (hopefully) going forward,

that same theory suggests that the still emerging materials of silicene and germanene• silicon and germanium based counterparts, respectively, of grapheme• may be more favorable still for condensate formation. The above mentioned transition dielectric constant is inversely proportional to the carrier Fermi velocity, and the carrier Fermi velocity in these latter materials is predicted to be smaller than that in grapheme.
This work has also led to a revival of interest in single-particle resonant tunneling in 2D-2D systems; prior work was perforemed in quasi-2D III-V system. While the ideal 2D nature of graphene and the symmetric bandstructure is advantageous, under SWAN we have found that 2D materials with lower carrier veloicities also would be suject to less short-channel indueced resonant broadening.
Moreover, topological insulators (TI), first considered as BiSFET-candidate materials because of reduced free-carrier screening in their gapless surface states, are now being considered for novel electromagnetic devices for the next NRI phase because of the intrinsic spin-polarized surface transport.

Center Management Lessons For Director

Directing the SWAN center has perhaps been the most technically challenging and intellectually stimulating endeavor that I have been involved in in my career. As someone who has had continous involvement with SRC over my entire 25 years in academia, and has been fortunate eonough to have received support continously from all three branches of SRC• GRC, FCRP and NRI• I feel that I can provide some unique perspectives. While all three SRC programs have been tremendously beneficial to my research group, NRI, by design, has perhaps been the most fun intellectually. On one hand, it has forced me and my engineering colleagues to delve into basic many-body quantum physics-concepts, some learned in graduate school but long forgotten. On the other hand, our theorist friends in Physics have been ecstatic for the opportunity to get involved in practical engineering problems. The third leg of this program, embedding very active industrial mentors in the various centers to a perhaps greater degree than in FCRP and GRC, has kept SWAN grounded in reality. I do not believe there is another program within the SRC, NSF or DoD that has achieved this balance between encouraging esoteric device concepts and keeping in mind the practical goal of developing the next, ultra-low power logic switch. SWAN aside, I hope the far forward thinking NRI program continues indefinately. In my opinion, the nation and the semiconductor industry cannot afford otherwise.

Sanjay Banerjee
Director of SWAN

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Top 5-10 Journal Publications for the Duration of the Center's Operation

[1] H. Min, R. Bistritzer, J.-J. Su, and A. H. MacDonald, "Room-temperature superfluidity in graphene bilayers," Physical Review B, vol. 78, no. 12, p. 121401, 2008 Times Cited as of July 2013: 154.

[2] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer PseudoSpin Field-Effect Transistor (BiSFET): A Proposed New Logic Device," Electron Device Letters, IEEE, vol. 30, no. 2, pp. 158–160, 2009 Times Cited as of July 2013: 85.

[3] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," Science, vol. 324, no. 5932, pp. 1312–1314, May 2009 Times Cited as of July 2013: 2,595.

[4] A. Pirkle, R. M. Wallace, and L. Colombo, "In situ studies of Al2O3 and HfO2 dielectrics on graphite," Applied Physics Letters, vol. 95, no. 13, pp. 133106–3, 2009 Times Cited as of July 2013: 36.

[5] D. Reddy, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer Pseudospin Field-Effect Transistor: Applications to Boolean Logic," IEEE Trans. on Electron Devices, vol. 57, no. 4, pp. 755–764, 2010 Times Cited as of July 2013: 16.

[6] D. Basu, L. Register, D. Reddy, A. MacDonald, and S. Banerjee, "Tight-binding study of electron-hole pair condensation in graphene bilayers: Gate control and system-parameter dependence," *Physical Review B*, vol. 82, no. 7, Aug. 2010 Times Cited as of July 2013: 10.

[7] D. Basu, L. Register, A. MacDonald, and S. Banerjee, "Effect of interlayer bare tunneling on electron-hole coherence in graphene bilayers," *Physical Review B*, vol. 84, no. 3, Jul. 2011 Times Cited as of July 2013: 7.

[8] I. Sodemann, D. Pesin, and A. MacDonald, "Interaction-enhanced coherence between two-dimensional Dirac layers," Physical Review B, vol. 85, no. 19, May 2012 Times Cited as of July 2013: 14.

[9] D. Reddy, L. F. Register, and S. K. Banerjee, "Bilayer Graphene Vertical Tunneling Field Effect Transistor", 70th Device Research Conference, State College, Pennsylvania, June (2012) , pp. 73–74 Times Cited as of July 2013: 1

[10] S.Kim; Jo Insun; Nah Junghyo; Z. Yao, Z ; S.Banerjee; E.Tutuc, Coulomb drag of massless fermions in graphene, PHYSICAL REVIEW B Volume: 83 Issue**:** 16 APR 8 2011 (Editor's Choice) Times Cited as of July 2013: 60.

Important Invention Disclosures for the Duration of the Center's Operation

- Sanjay K. Banerjee, Leonard Franklin Register, II, Allan MacDonald, Dharmendar Reddy Palle, Emanuel Tutuc, "Bi-layer pseudo-spin Field Effect Transistor," Application number: 12/624,481, Publication number: US 2010/0127243 A1, Filing date: Nov 24, 2009, Patent US 8,188,460 Issued May 29, 2012.
- L. F. Register and S. K Banerjee, "Incorporating Gate Control over Resonant Tunneling Structure in CMOS To Reduce Off-State Current Leakage, Supply Voltage and Power Consumption." (Otherwise know at the "Resonant Injection Enhanced Field-Effect Transistor" or "RIEFET"), Disclosure, May 2008, Patent application 12/370,844 filed January 13 2009, Patent US 8,008, 649 Issued August 30 2011.
- Sanjay K Banerjee, Allan MacDonald, Leonard Franklin Register and Bhagawan R. Sahu, "BiSFETs and Novel Transistors based on Topological Insulators," Disclosure January 2011.
- L. Colombo, R. M. Wallace, R. S. Ruoff, "Synthesizing Fraphene from Metal-Carbon Solutions Using Ion Implantation," Provisional (2009).
- L. F. Register and S. K. Banerjee, "Hetero-barrier Tunnel Field-Effect Transistor (HetTFET) for low voltage logic," Disclosure, May 2008.

INDEX
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History and Accomplishments of the INDEX Center

Date: November 30, 2012

A Brief History of INDEX

As one of the original NRI centers, the **In**stitute for **N**anoelectronics **D**iscovery and **Ex**ploration (INDEX) has been a leader in developing post-CMOS logic devices and architectures. We have pursued novel devices that are true to NRI's mission, leveraging the multidisciplinary talent in device conception, benchmarking, fabrication, and characterization. INDEX currently supports 14 PIs from Columbia University, Georgia Institute of Technology, MIT, University at Albany-SUNY, University of Virginia, and Purdue University. The culmination of our work over the past five years has resulted in two promising device concepts; they are graphene p-n junction (GPNJ) devices and spin logic devices. Of the two device themes, GPNJ devices have been incubated from the start of the INDEX program, while spin logic devices were brought into the program at a later stage, in part because graphene is a promising material for spin logic devices and INDEX had a growing expertise in graphene materials and devices.
The focus of INDEX, during phase 1.0, was finding new information tokens that could over come the computing limits of the field effect transistor. As such, INDEX operated under a "let a thousand flower bloom" mode with 24 PIs across 11 universities. The PIs were chosen for their diverse background in physics, physical chemistry, electrical engineering, mechanical engineering, and materials science, with expertise in transport physics, modelling, fabrication, and metrology. The participating universities were California Institute of Technology, Columbia University, Georgia Institute of Technology, Harvard University, MIT, University at Albany – SUNY, University of Virginia, North Carolina State University, Purdue University, Rensselaer Polytechnic Institute and Yale University. The materials we examined included organic semiconductors, inorganic nanowires, carbon nanotubes, ferromagnetic materials, magnetic oxides, and graphene. The PIs were distributed over 3 high-level themes: Graphene, Magnetic, and Exciton. Of these, the greatest concentration of faculty members worked on graphene, with 17 PIs. Several of the PIs, including those who worked on fabrication and metrology, crossed multiple device themes to make full utilization of their capabilities. Within each theme, multiple device concepts and projects were being pursued. For example, within the graphene theme, the PIs worked on metrology, modelling, architecture, and devices; and, within graphene devices, the PIs pursued at least 5 different device concepts, including devices based on spin transport, p-n junction, bilayer graphene, and nanoribbons. Similarly, for magnetic devices, multiple devices were being pursued by the PIs, including magnetically coupled ring devices, domain wall logic, and magnetic complex oxides. The most theoretical concepts came from those pursuing excitonic devices. This theme also had the fewest number of PIs as all of them, back then, were relatively new to their universities and were in the process of setting-up their laboratory facilities. Nevertheless, the PIs were encouraged to pursue and realize their device concepts because NRI had identified excitons as one of the truly new logic tokens to emerge from the NRI centers.

The broad set of device concepts and materials that we pursued within INDEX in the beginning was necessary and consistent with the mission of NRI at the time. As the researchers analyzed their state variables, however, it became clear that many of the early information tokens would never implement logic functions efficiently. Specifically, one of the key requirements, that the encoded information token had to maintain its state over many successive logical operations, was violated for several state variables. This included magnetically coupled ring devices, which lacked a viable interconnect scheme, and complex magnetic oxides, which never exhibited FET characteristics. Several device concepts were extensions of conventional FET devices, including graphene nanoribbon devices, which have yet to show the formation of a band gap with reduced ribbon width. It is now believed that transport in ribbons is dominated by Anderson-like localization that precludes the observation of ballistic conductance and chirality-dependent transport, as seen in carbon nanotubes. Some concepts were dropped simply because a deeper physical understanding was missing at the time when we narrowed our device options. This included all the excitonic device concepts. One of the main criteria we had used was when we down selected our device options was demonstration of architectural schemes for performing complex logic functions. Specifically, for phase 1.5 efforts, each information token and the associated device had to not only perform switching, but also communicate through an interconnect scheme to drive the next device. This exercise of winnowing down the device concepts helped to establish a broad-based framework within INDEX for taking fundamental studies to device concepts.

GPNJ is one of the device concepts that transitioned to the Phase 1.5 effort. Although it started with a single investigator during Phase 1, the unique angle-dependent transport properties of GPNJs were

identified as a new information token and motivated strong modelling efforts from the INDEX members. Thus, for Phase 1.5, a team was assembled with expertise in fabrication, modelling and benchmarking to fully capitalize on the promising properties. The culmination of this effort is a device concept with steep subtheshold (SS) slope characteristics and high ON/OFF ratio. The confidence of the team is principally found in the close collaboration between experiment, which demonstrated the most detailed angle-dependent transport study in GPNJs, and modelling, which successfully reproduced the experimental results. Having firmly benchmarked our modelling efforts, we are confident in its prediction of SS slope characteristics. In fact, we anticipate a class of SS slope devices to emerge and have found two devices with such characteristics already.

In parallel, we are also investigating bilayer GPNJ devices, which should show similar angle-dependent transport properties found in monolayer junctions. In a monolayer GPNJ, carriers that are incident normal to the junction transmit with unity probability (known as Klein Tunneling). Therefore, monolayer GPNJ devices are engineered to remove this particular transport mode, either by creating a void or by using a tiled junction after carriers have been collimated. In a bilayer junction, on the other hand, the transmission of the normal mode is forbidden. This anti-Klein tunnelling property of a bilayer GPNJ should result in devices with high on/off properties with reduced design complexity.

The second device to transition to Phase 1.5 was spin logic devices, which by that time had become All-Spin-Logic (ASL). ASL uses nonlocal transport of purely spin currents to torque the magnetic element of the next device. Although we have made considerable progress in device related measurements, including the first demonstration of nonlocal spin transfer torque in graphene, the team has been encouraged by recent developments in other spin torque measurements. Thus, in keeping with our mission to examine the most novel device concepts, a new spin logic device, called the Charged-Couple Spin Logic (CSL), will be investigated. CSL uses the newly demonstrated Giant Spin Hall Effect (GSHE) in metals with strong spin-orbit coupling, which provides a robust room-temperature spin-polarized charge current that can apply spin torque to a magnet. We refer to this process as the ”write” function. Coupled to the GSHE metal are split Magnetic Tunnel Junctions (MTJs), which selects the sense of the spin polarized current and enables the logic “read” function. The “read” and “write” functions in CSL provide the basis for new room-temperature, spin-logic circuits that overcome the interconnect delays of most spin-based logic circuits. Furthermore, since CSL is primarily a metal-based construction, the full implementation of this logic device can be developed in CNSE’s 300mm line. The device integration will leverage CNSE’s new MTJ processing capabilities that are being put in place. Currently, both ASL and CSL devices are being investigated. We will continue to examine both until we can clearly quantify architectural advantages of one over the other.

Lessons Learned: GPNJ devices represent one of the most promising devices to emerge from NRI, and its success is a direct consequence of our strategy in building synergistic, collaborative teams within a multidisciplinary environment. One of the key lessons we have learned in establishing such an environment is the need to encourage those working on fundamental physics to also examine device related parameters. This was achieved by actively engaging them to identify concepts that can be extrapolated into functional devices, for which the angle dependent transport in GPNJ was an example. This transition required not only an interdisciplinary team with the right skill set but also one with sufficient overlap among team members so that the “language” barrier was minimized. In fact, the early days of semiconductor research invited researchers with background in physics, materials and engineering to work together to come-up with a unified device concept. In large part, due to the specialization of academic disciplines that have occurred over the years, it has become increasingly difficult to find researchers with deep expertise and broad knowledge that can thrive in a multidisciplinary environment. On the other hand, we have learned that having a center with researchers from different disciplines encouraged crosscutting learning to occur.

Looking forward: From the vantage point of having deep expertise in novel physics that arise in new materials and benchmarking of new device concepts with architectural schemes, the INDEX team is poised to succeed over the long run by also continuously innovating and modifying our strategy. For instance, our strategy to develop devices at the wafer line of the College of Nanoscale Science and Engineering (CNSE) has been in development for some time. Using IBM’s 0.1WSD donation, we have begun to use the CNSE's facility to demonstrate graphene-based devices and, recently, have actively pursued full process integration. While most studies in graphene are conducted on thermally grown SiO_2, new substrate materials are needed if graphene is to be used in 3D integration. Recently, the INDEX team has developed a deposited film that can provide similar mobility values as those found on thermally grown SiO_2, and provide the necessary adhesion of graphene that was lacking on a deposited SiO_2. This is one example of the steps our team has taken to ensure progress

in graphene integration. In the future, we will not only realize the two device concepts at CNSE's wafer line, but also take these concepts to the next level by developing 3D integration and new architectures that exploit the higher device density.

Ji Ung Lee
Director of INDEX

PUBLICATIONS AND PATENTS

Top 5-10 Journal Publications for the Duration of the Center's Operation

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- Snake States in Graphene, J. R. Williams, C. M. Marcus,Phys. Rev. Lett. 107, 046602 (2011) Times Cited as of July 2013: 28.
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Important Invention Disclosures for the Duration of the Center's Operation

Low Energy Magnetic Domain Wall Logic Device, from MIT, Lead PI: Caroline Ross, October 2011.