Burn-in Reduction: Improving Outlier Screening

"TI has reaped a very large return on investment when compared to the cost of the research contract."
— K Butler, Fellow Texas Instruments

SRC 1197.1 Task Members

W.R. Daasch: Principal Investigator

- Professor, Electrical and Computer Eng.
- Member IEEE, Sigma Xi
- Founder and Director of Integrated Circuits Design and Test Laboratory (ICDT)

L.W. Ning: PhD Candidate

- "Burn-in Reduction using Supervised Learning Analysis of Wafer Sort Test Data," PhD, 2009
- — "*IC binning using residuals of the test response* ", MS Thesis, Portland State University, 2004

N.Amit: Test Engineer, Texas Instruments

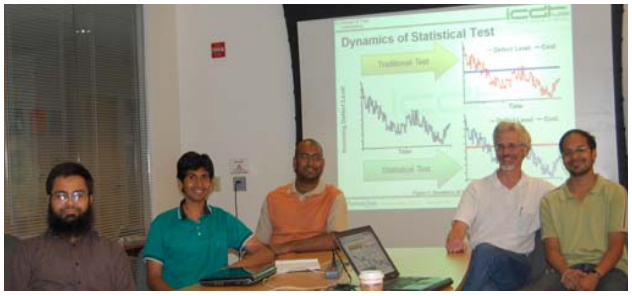
- "*Burn-in reduction using principal component analysis*", MS Thesis, Portland State University, 2006

Integrated Circuits Design and Test Laboratory

ICDT is home to the Advanced Test Methods Group headed by Dr. Daasch. This facility is used to develop and improve methods for all areas in semiconductor design and test .

Accomplishments

- Semiconductor Research Corporation 2008 Technical Excellence Award
- Six patents awarded and 30+ publications since ICDT Laboratory founding in 2000.
- Best Paper awards the International Test Conference 2002 and VLSI Test Symposium 2003
- Over $1.3 million dollars in research grants and contract awards and $3 million in equipment and in-kind donations
- ICDT graduates placed at Credence Systems, IBM, Intel, LSI, Mentor Graphics, Micron, Tektronix, Texas Instruments



Problem Statement

Decrease burn-in cost, maximize yield and retain reliability

Research Objective

Assess early failure risk of statistical outliers in sort data

Sort Test Modeling of Early Failures

The project met the challenge of burn-in reduction and quality retention by assembling meta-variables from sort-test parametric response. **Supervised learning** screened and combined the meta-variables. Classification and Regression Trees (CART), Canonical Correlation Analysis (CCA), and Principal Component Analysis (PCA) were used.

General Approach

Create and evaluate candidate meta-variables in 3 steps

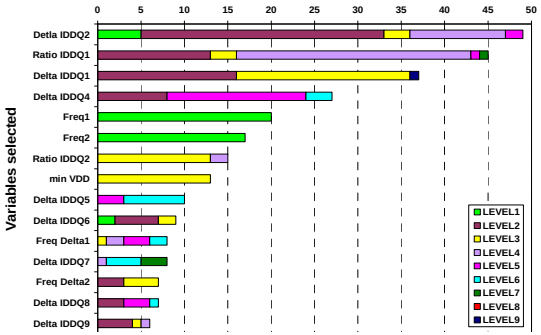
- **Training:** Per chip sort-test and post-burn-in data were combined and analyzed with CART, CCA, or PCA to create meta-variables
- **Optimization:** A second combined dataset is created to improve the new meta-variables accuracy in predicting burn-in failure. Steps 1&2 define supervised learning because the burn-in result is known
- **Generalization:** Per chip sort-test data only is analyzed with Step 2 meta-variables to predict burn-in fails data. With only sort-test data the step assess the viability of a set of meta-variables in production

CART Burn-In Reduction Results

Generalization Results for Original and Improved (pruned) CART

	CART Prediction			
	Original tree		Pruned tree	
Post-Burn-In	Pass	Fail	Pass	Fail
Pass	91%	9%	65%	35%
Fail	67%	33%	20%	80%

- Validation results in table above shows a pruned tree decreases the misclassification rate.
- Pruned trees predict 80% burn-in fails and reduces parts requiring burn-in by 2/3
- Pruned tree has highest ability to predict burn-in fails
- Bar chart below shows 10 out of 15 top burn-in predictors are IDDQ
- Frequency measurements used 4 of 5 times at the tree root
- Trees with both IDDQ and frequency classify early fails with fewer burn-in passes lost through misclassification



Parametric screens as burn-in predictors

Technology Transfer/Industrial Interactions

- Software prototypes
- Evaluation of sort test measurements EFR predictors
- Burn-in Outlier Screens
- Sort Test Burn-in Outlier Screens
- Location Averaging
- Principal Component Variable Reduction
- Canonical Correlation Analysis
- Sort Test Burn-in Risk Classification
- Classification and Regression Trees
- Industrial Interactions – TI, Intel, IBM, AMD
- DOE of sort-test data set collection
- Multiple data sets 90nm and 65nm nodes
- Participation on student thesis committees
- Private communications with Industrial Liaisons

Recent Publications

- "*Burn-in Reduction using Principal Component Analysis*", Nahar (PSU), Daasch (PSU), Subramaniam (TI), ITC 2005
- *"Burn-in Reduction using Robust Canonical Correlation Analysis,"* Ning, Nahar, Daasch (PSU), Butler, Carulli, Subramaniam (TI), SRC Techcon 2005
- "Successful Development and Implementation of Statistical Outlier Techniques on a 65nm Process Driver Device," Nahar, Subramaniam, et. al (TI) and WR Daasch (PSU), IRPS 2006
- "Burn-in Fail Prediction using Classification and Regression Trees," Ning, Daasch (PSU), Subramaniam, Carulli, Butler (TI),in preparation

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